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HD74LV2GT123A

Retriggerable Monostable Multivibrator

REJ03D0004-0200Z
(Previous ADE-205-699A(Z))
Rev.2.00
Apr.18.2003

Description

The HD74LV2GT123A features output pulse duration control by three methods. In the first method, the $\overline{A}$ input is low and the B input goes high. In the second method, the B input is high and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high. The basic pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between Cext and Rext/Cext (positive) and an external resistor connected between Rext/Cext and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between Rext/Cext and V_{CC}. Once triggered, the basic pulse duration can be extended by retriggering the gated low level active ($\overline{A}$) or high level active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. The output pulse equation is simply : $t_{WQ} = Cext \bullet Rext$.

Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- Control input is TTL compatible input level.
  Supply voltage range : 4.5 to 5.5 V
  Operating temperature range : –40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
  All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Output current ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- All the logical inputs have hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV2GT123AUSE	SSOP-8 pin	TTP-8DBV	US	E (3,000 pcs / Reel)

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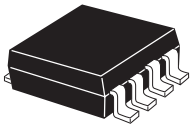
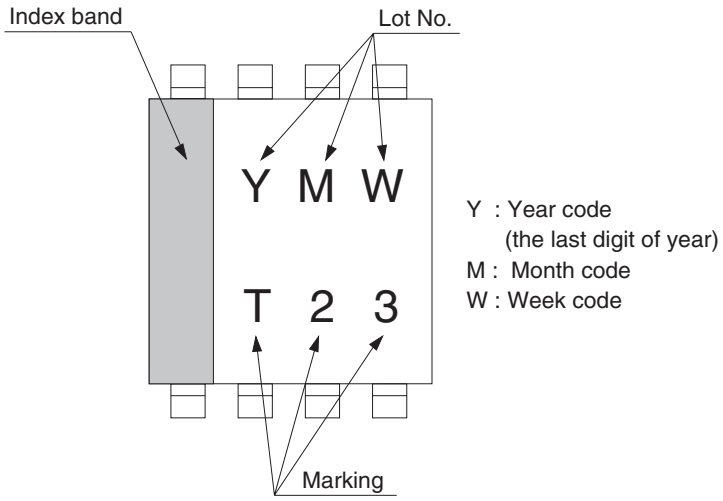
Outline and Article Indication

• HD74LV2GT123A



SSOP–8



Function Table

Inputs			Output Q
$\overline{CLR}$	$\overline{A}$	B	
L	X	X	L
H	H	X	L
H	X	L	L
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

H : High level
L : Low level
X : Immaterial
↑ : Low to high transition
↓ : High to low transition
⎍ : High level pulse

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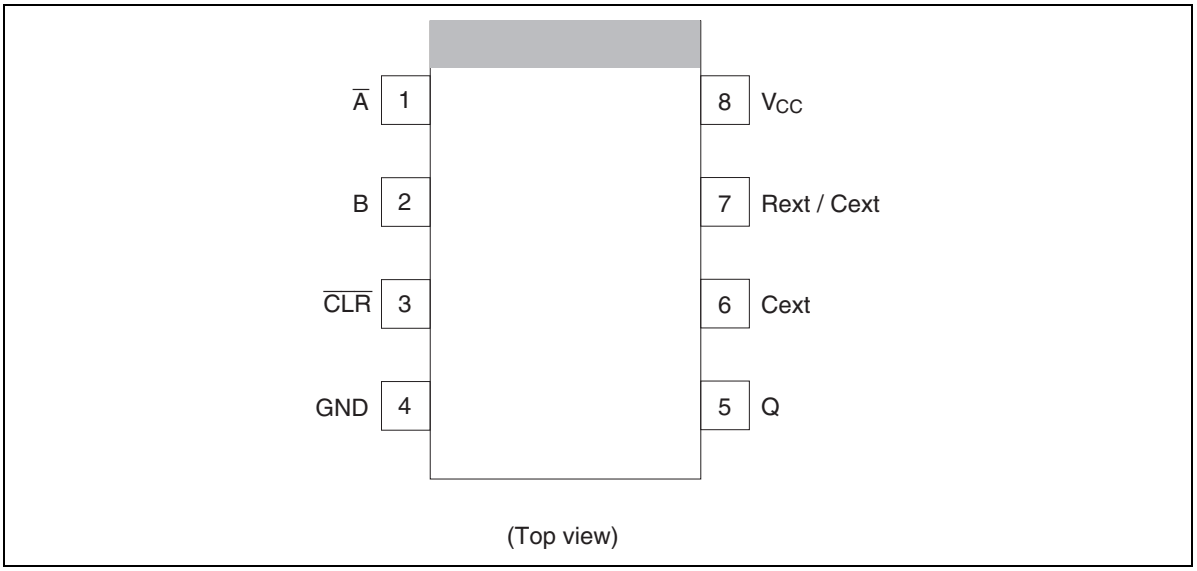
Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range [*1]	V_I	–0.5 to 7.0	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output : H or L
		–0.5 to 7.0		V_{CC} : OFF
Input clamp current	I_{IK}	–20	mA	V_I < 0
Output clamp current	I_{OK}	±50	mA	V_O < 0 or V_O > V_{CC}
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air) [*3]	P_T	200	mW	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

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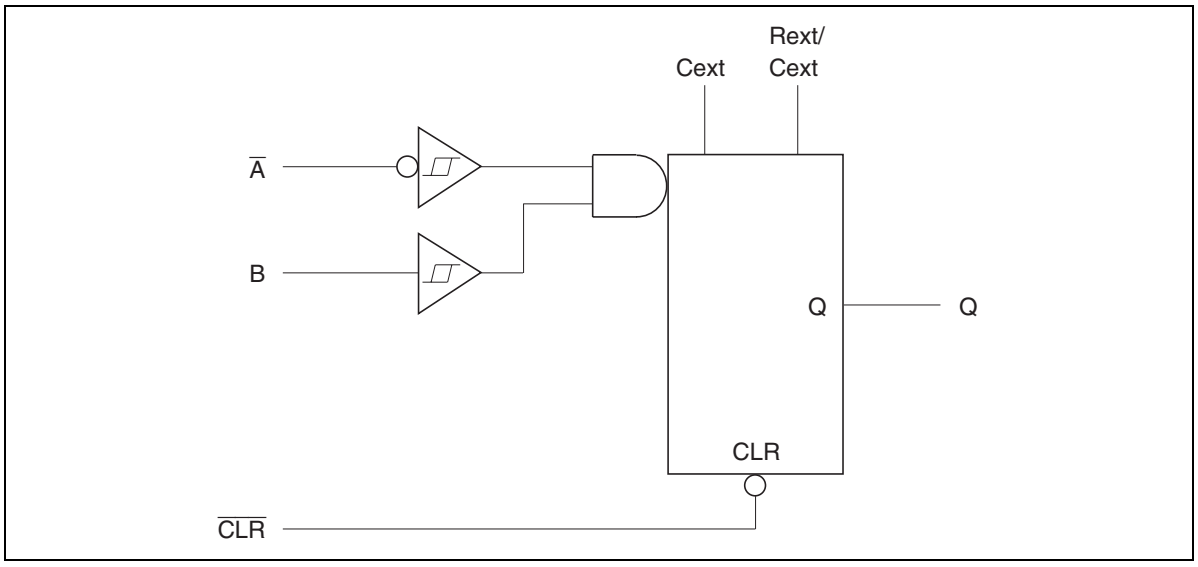
Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.5	—	5.5	V	
Input voltage range	V_I	0	—	5.5	V	
Output voltage range	V_O	0	—	V_{CC}	V	
Output current	I_{OH}	—	—	–12	mA	V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	—	20	ns / V	V_{CC} = 4.5 to 5.5 V
External timing registance	Rext	1	—	—	kΩ	V_{CC} = 4.5 to 5.5 V
External capacitance	Cext	—	Unlimited	—	F	
Supply transition rise rate	$\Delta t / \Delta V_{CC}$	1	—	—	ms / V	
Operating free-air temperature	T_a	–40	—	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



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Electrical Characteristic

- Ta = –40 to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	V	
	V_{IL}	4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	5.0	—	0.15	—	V	$V_T^+ – V_T^-$
Output voltage	V_{OH}	Min to Max	V_{CC}–0.1	—	—	V	I_{OH} = –50 µA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Input current Rext / Cext	I_{IN}	5.5	—	—	±2.5	µA	V_{IN} = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	µA	V_{IN} = V_{CC} or GND, I_O = 0
	I_{CC}–T	5.5	—	—	1.5	mA	One input V_{IN}=3.4V, other input V_{CC} or GND
Active state supply current	ΔI_{CC}	4.5	—	—	650	µA	V_{IN} = V_{CC} or GND Rext / Cext = 0.5V_{CC}
		5.5	—	—	975		
Output leakage current	I_{OFF}	0	—	—	5	µA	V_{IN} or V_O = 0 to 5.5 V
Input capacitance	C_{IN}	5.0	—	3.0	—	pF	V_{IN} = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

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Switching Characteristics

- V_{CC} = 5.0 ± 0.5 V

Item	Symbol	T_a = 25°C			T_a = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	7.3	12.0	1.0	14.0	ns	C_L = 15 pF	$\overline{A}$ or B	Q
		—	8.5	14.0	1.0	16.0		C_L = 50 pF		
	t_{PHL}	—	5.9	9.4	1.0	11.0	ns	C_L = 15 pF	$\overline{CLR}$	Q
		—	7.5	11.4	1.0	13.0		C_L = 50 pF		
	t_{PLH}	—	7.3	12.9	1.0	15.0	ns	C_L = 15 pF	$\overline{CLR}$ (Trigger)	Q
		—	8.7	14.9	1.0	17.0		C_L = 50 pF		
Output pulse width	t_{wQ}	—	140	200	—	240	ns	C_L = 50 pF, Cext = 28 pF, Rext = 2 kΩ		
		90	100	110	90	110	µs	C_L = 50 pF, Cext = 0.01 µF, Rext = 10 kΩ		
		0.9	1.0	1.1	0.9	1.1	ms	C_L = 50 pF, Cext = 0.1 µF, Rext = 10 kΩ		
Pulse width	t_w	5.0	—	—	5.0	—	ns	$\overline{A}$, B or $\overline{CLR}$		
Retrigger time	t_{rr}	—	20	—	—	—	ns	$\overline{A}$ or B (Rext = 1 kΩ, Cext = 100 pF)		
		—	0.95	—	—	—	µs	$\overline{A}$ or B (Rext = 1 kΩ, Cext = 0.01 µF)		

Operating Characteristics

- C_L = 50 pF

Item	Symbol	V_{CC} (V)	T_a = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	5.0	—	31.0	—	pF	f = 10 MHz

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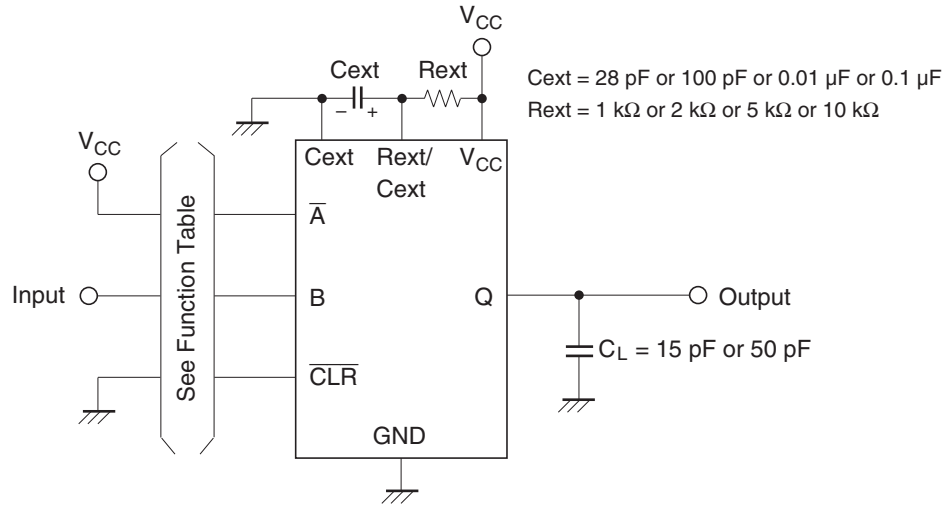
Test Circuit



Note : C_L includes the probe and jig capacitance.

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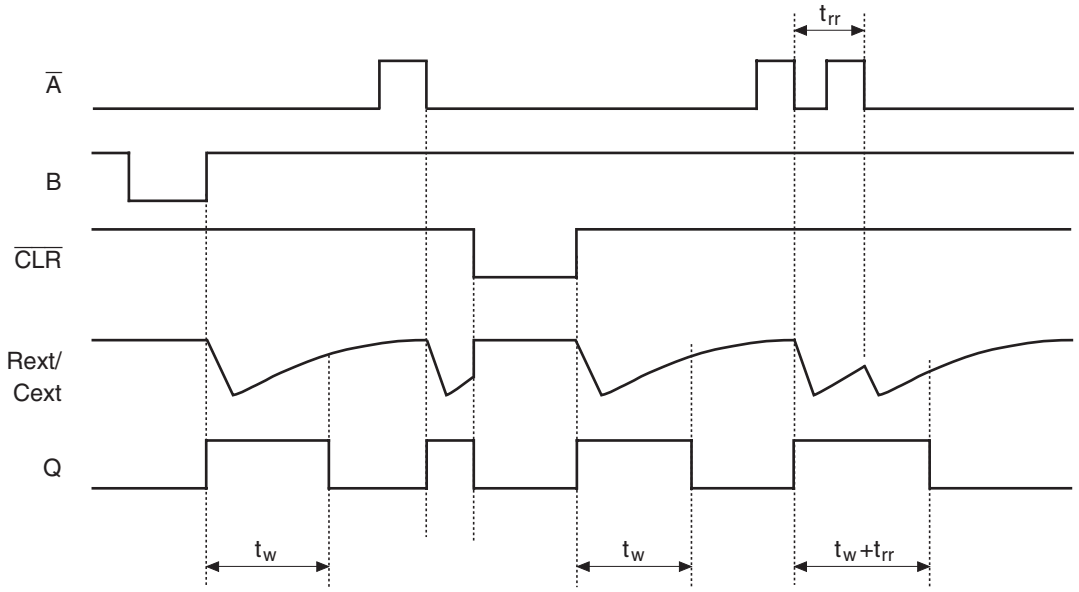
Timing Diagram



Caution in use

In order to prevent any malfunctions due to noise, connect a high frequency performance capacitor between Vcc and GND, and keep the wiring between the External components and Cext, Rext/Cext pins as short as possible.

Large values of Cext may cause problems when powering down the HD74LV2GT123A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from Vcc through the protection diodes at pin 7 pin.
Current through the input protection diodes must be limited to 20 mA; therefore, the turn-off time of the Vcc power supply must not be faster than t = Vcc • Cext/(20 mA). For example, if Vcc = 5 V and Cext = 22 μF, the Vcc supply must turn off no faster than t = (5 V) • (22 μF)/ 20 mA = 5.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.
When a more rapid decrease of Vcc to zero volts occurs, the HD74LV2GT123A may sustain damage.
To avoid this possibility, use an external calmping diode.

The input pins for unused circuit should be used under conditions to fix the outputs to avoid malfunction caused by noises. Also, it's recommended that Rext / Cext terminals are open and external parts are not connected to.

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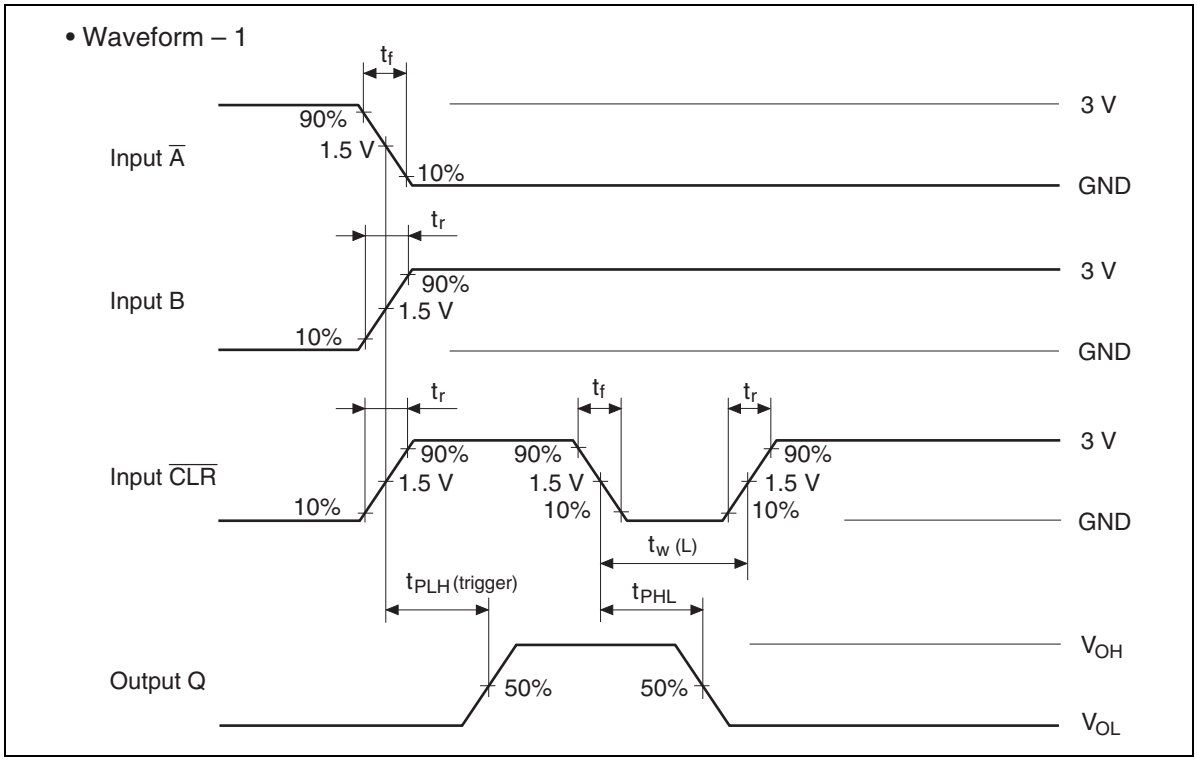
• Waveform – 1



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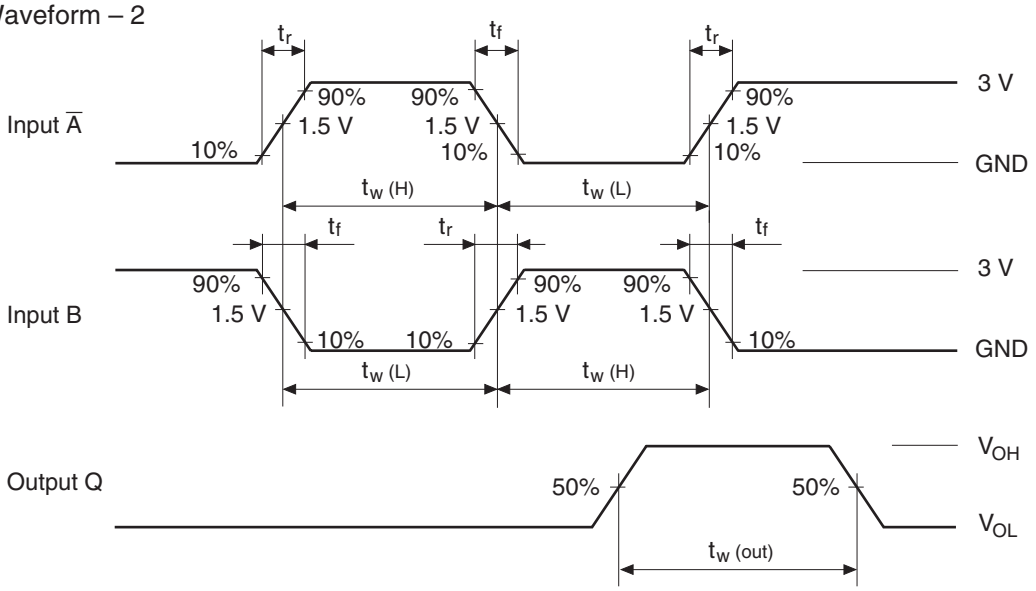
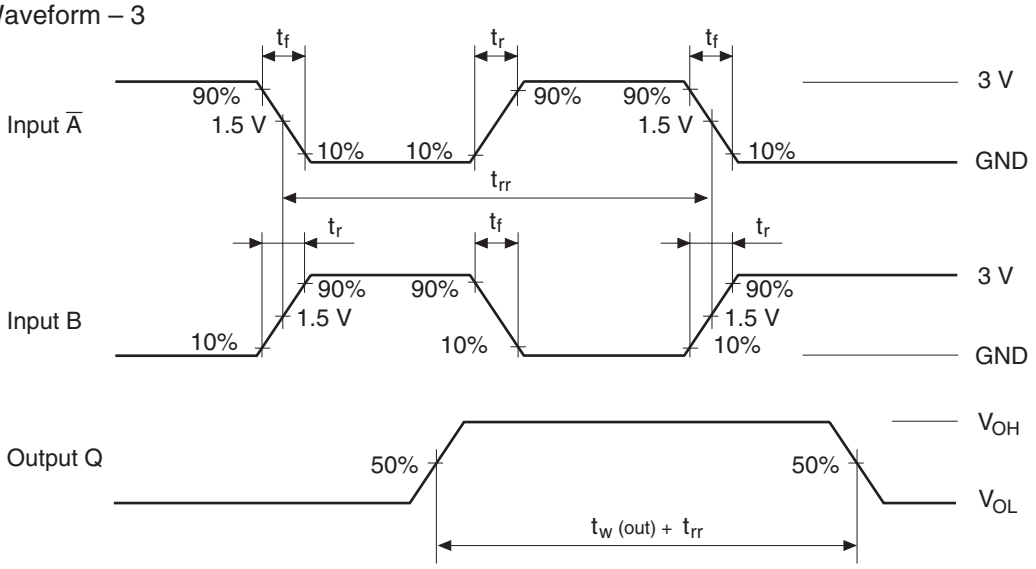
• Waveform – 2



• Waveform – 3



Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns
2. The output are measured one at a time with one transition per measurement.

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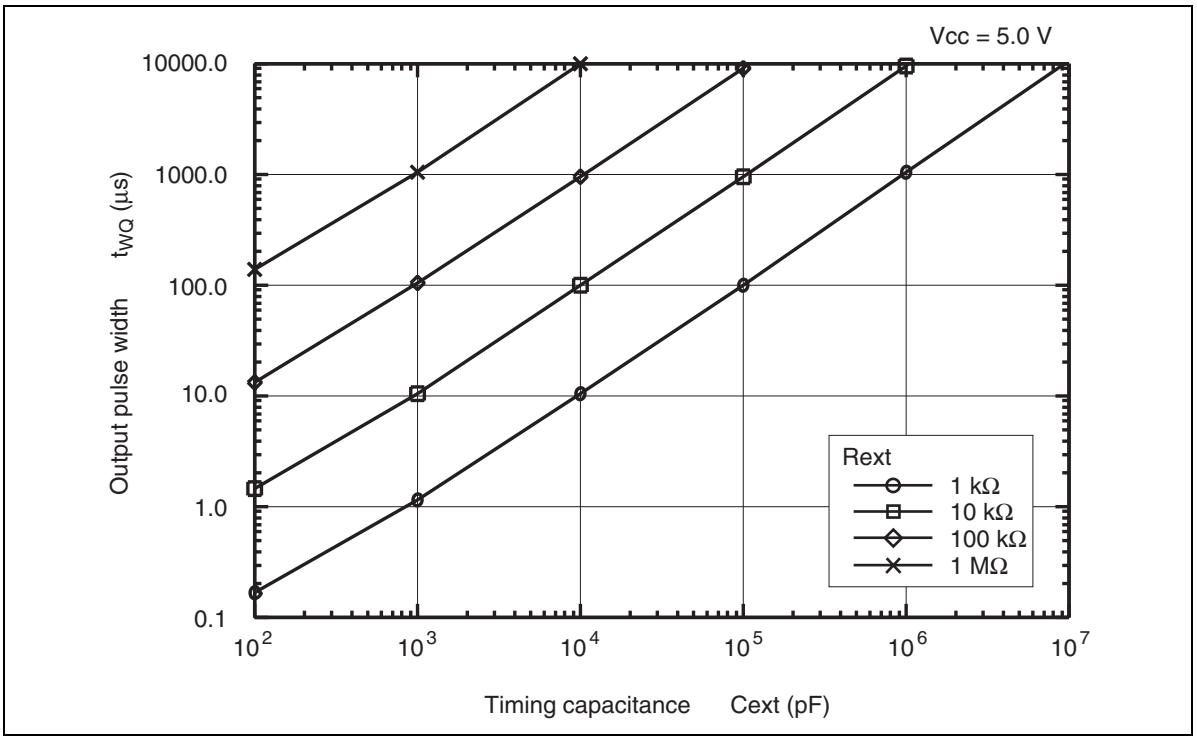
Application Data



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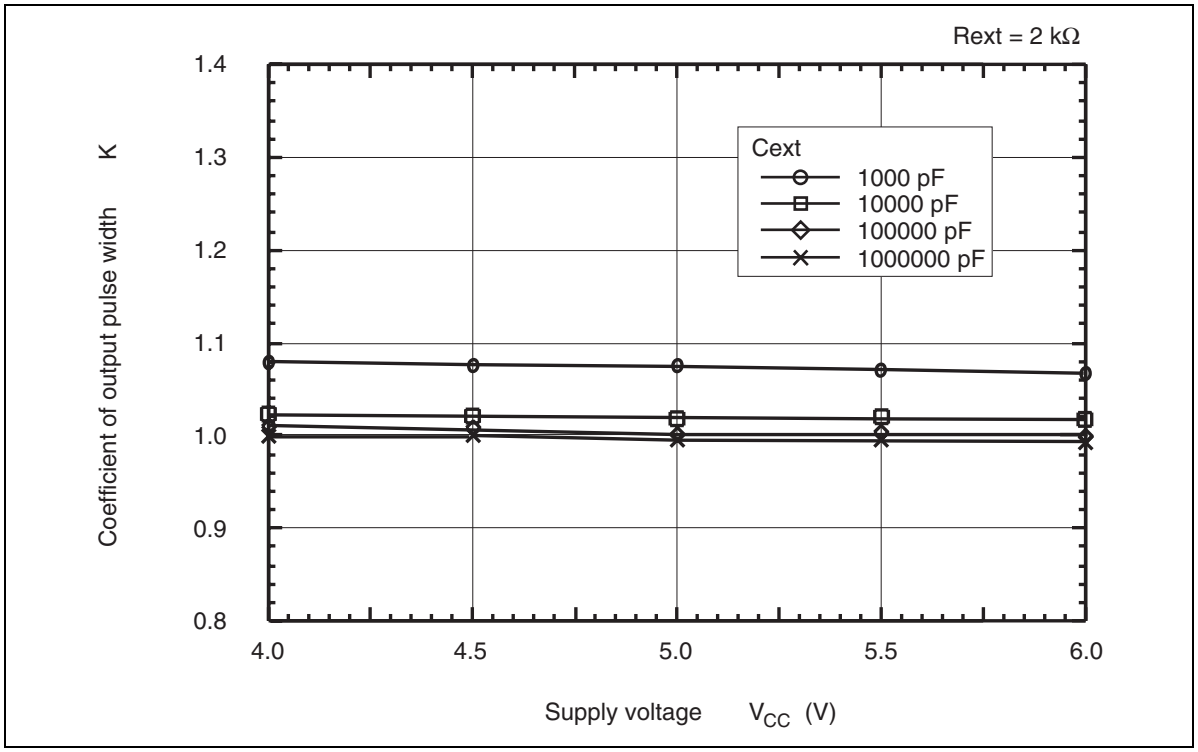

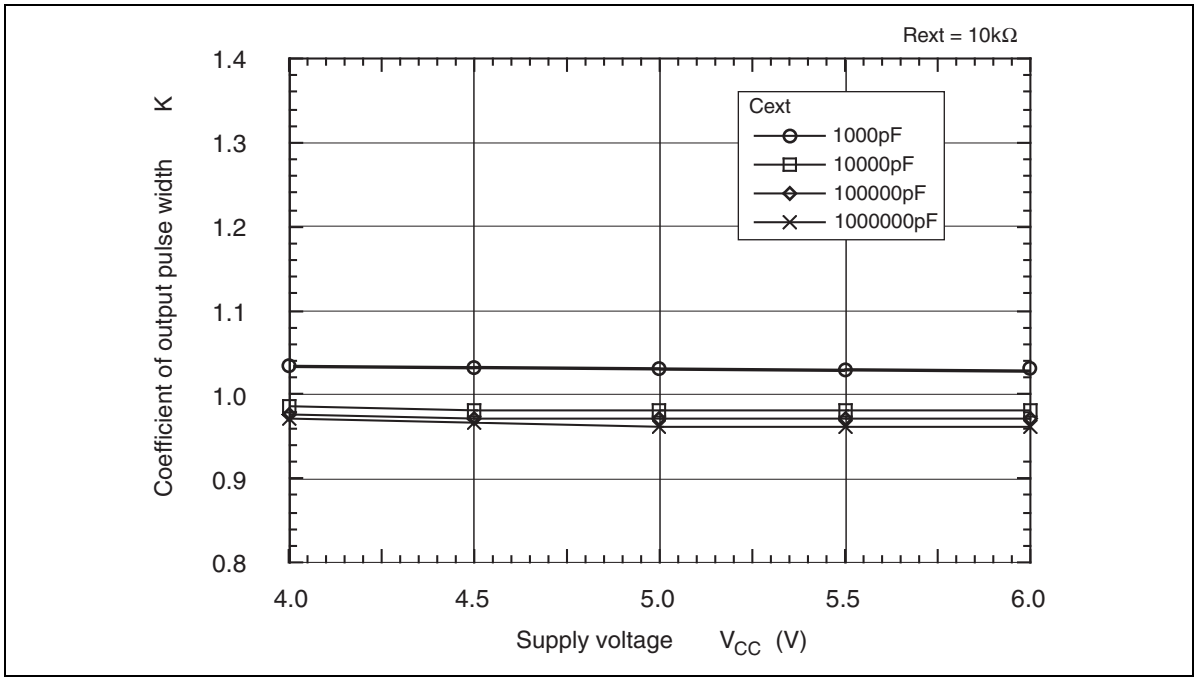

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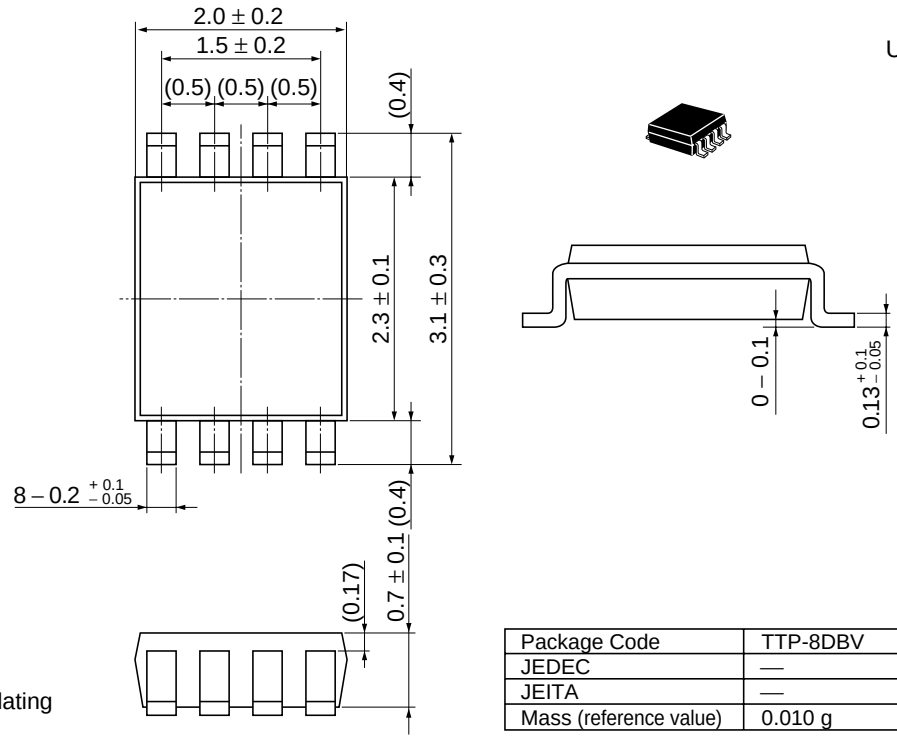
Package Dimensions



Unit: mm

*Sn-Bi plating

Package Code	TTP-8DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.010 g

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