

HD74LVCC4245A

Octal Dual-supply Bus Transceiver with configurable output voltage with 3-state Outputs

REJ03D0380-0101

Rev.1.01

Apr. 13, 2005

Description

The HD74LVCC4245A has eight bus transceivers with three state outputs in a 24 pin package. When (DIR) is high, data flows from the A inputs to the B outputs, and when (DIR) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input (\overline{OE}) high level. This 8-bit non-inverting bus transceiver uses two separate power-supply rails.

And this product has two terminals (V_{CCA} , V_{CCB}), V_{CCA} is connected with control input and a bus side, V_{CCB} is connected with B bus side. V_{CCA} and V_{CCB} are isolated.

The A port, V_{CCA} , is dedicated to accept a 5 V supply level, and the configurable B port, which is designed to track V_{CCB} , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3 V to a 5 V environment and vice versa. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- This product function as level shift transceiver that change V_{CCA} input level to V_{CCB} output level, V_{CCB} input level to V_{CCA} output level by providing different supply voltage to V_{CCA} and V_{CCB} .
- This product is able to the power management: Turn on and off the supply on V_{CCB} side with providing the supply of V_{CCA} . (Enable input (\overline{OE}): High level)
- $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}$, $V_{CCB} = 2.7 \text{ V to } 5.5 \text{ V}$
- All control input V_I (max) = 5.5 V (@ $V_{CCA} = 0 \text{ V to } 5.5 \text{ V}$)
- All A bus side input outputs V_{IO} (max) = 5.5 V (@ $V_{CCA} = 0 \text{ V}$ or output off state)
- All B bus side input outputs V_{IO} (max) = 5.5 V (@ $V_{CCB} = 0 \text{ V}$ or output off state)
- High output current
A bus side: $\pm 24 \text{ mA}$ (@ $V_{CCA} = 4.5 \text{ V}$)
B bus side: $\pm 24 \text{ mA}$ (@ $V_{CCB} = 2.7 \text{ V to } 4.5 \text{ V}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Package)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVCC4245ATEL	TSSOP-24 pin	PTSP0024JB-A (TTP-24DBV)	T	EL (1,000 pcs/reel)

Function Table

Inputs		Operation
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

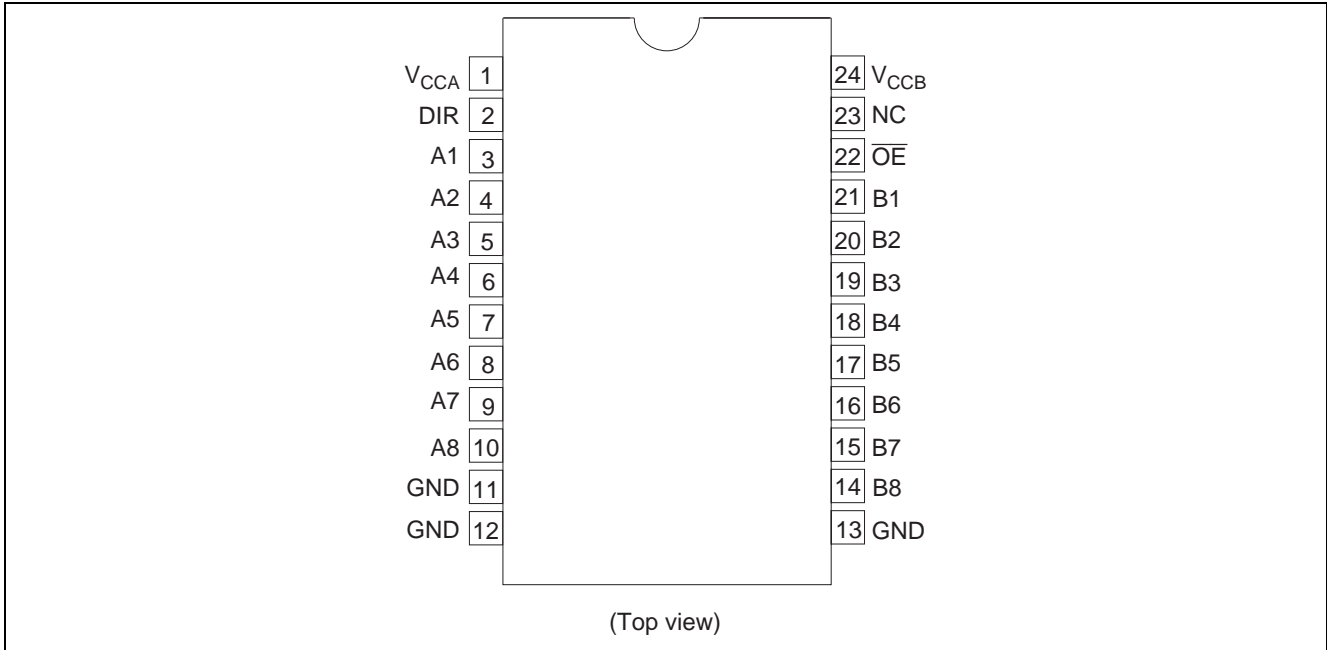
H: High level

L: Low level

X: Immaterial

Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CCA}, V_{CCB}	-0.5 to 6.0	V	
Input voltage ¹	V_I	-0.5 to 6.0	V	DIR, \overline{OE}
Input / output voltage	V_{IO}	-0.5 to $V_{CCA}+0.5$	V	A port output "H" or "L"
		-0.5 to 6.0		A port output "Z" or V_{CCA} : OFF
		-0.5 to $V_{CCB}+0.5$		B port output "H" or "L"
		-0.5 to 6.0		B port output "Z" or V_{CCB} : OFF
Input diode current	I_{IK}	-50	mA	$V_I < 0$
Output diode current	I_{OK}	-50	mA	$V_O < 0$
		50		$V_O > V_{CC}+0.5$
Output current	I_O	± 50	mA	
V_{CCA}, V_{CCB}, GND current	$I_{CCA}, I_{CCB}, I_{GND}$	100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ²	P_T	862	mW	TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

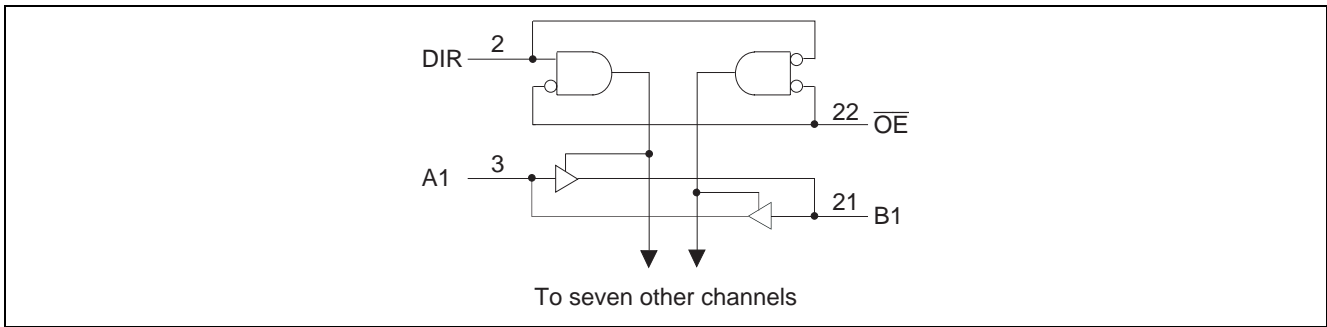
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of 150 $^\circ\text{C}$.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CCA}	4.5 to 5.5	V	
	V_{CCB}	2.7 to 5.5		
Input / output voltage	V_I	0 to 5.5	V	DIR, \overline{OE}
	$V_{I/O}$	0 to V_{CCA}		A port output "H" or "L"
		0 to 5.5		A port output "Z" or V_{CCA} : OFF
		0 to V_{CCB}		B port output "H" or "L"
	0 to 5.5	B port output "Z" or V_{CCB} : OFF		
output current	I_{OH}	-24	mA	
	I_{OL}	24		
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operating temperature	T_a	-40 to 85	°C	

Note: Unused or floating inputs must be held high or low.

Block Diagram



Electrical Characteristics

($T_a = -40$ to 85°C)

Item	Symbol	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit	Test Conditions	
Input voltage	V_{IHA}	4.5 to 5.5	2.7 to 5.5	2	—	V	A port	
	V_{IHB}	4.5 to 5.5	2.7 to 3.6	2	—		B port	
		4.5 to 5.5	4.5 to 5.5	$V_{CCB} \times 0.7$	—			
	V_{IH}	4.5 to 5.5	2.7 to 5.5	2	—		Control input	
	V_{ILA}	4.5 to 5.5	2.7 to 5.5	—	0.8		A port	
	V_{ILB}	4.5 to 5.5	2.7 to 3.6	—	0.8		B port	
		4.5 to 5.5	4.5 to 5.5	—	$V_{CCB} \times 0.3$			
V_{IL}	4.5 to 5.5	2.7 to 5.5	—	0.8	Control input			
Output voltage	V_{OHA}	4.5	3.0	4.4	—	V	$I_{OH} = -100 \mu\text{A}$	
				3.76	—		$I_{OH} = -24 \text{ mA}$	
	V_{OHB}	4.5	3.0	2.9	—		$I_{OH} = -100 \mu\text{A}$	
				2.7	2.2		—	$I_{OH} = -12 \text{ mA}$
					3.0		2.46	—
				2.7	2.1		—	$I_{OH} = -24 \text{ mA}$
					3.0		2.25	—
				4.5	3.76		—	
	V_{OLA}	4.5	3.0	—	0.1		$I_{OL} = 100 \mu\text{A}$	
				—	0.44		$I_{OL} = 24 \text{ mA}$	
	V_{OLB}	4.5	3.0	—	0.1		$I_{OL} = 100 \mu\text{A}$	
				2.7	—		0.44	$I_{OL} = 12 \text{ mA}$
					3.0		—	0.44
				2.7	—		0.5	
4.5					—	0.44	$I_{OL} = 24 \text{ mA}$	

Electrical Characteristics (cont)

(Ta = -40 to 85°C)

Item	Symbol	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit	Test Conditions
Input current	I _{IN}	5.5	3.6 5.5	—	±1	μA	Control input V _I = V _{CCA} or GND
Off state output current	I _{OZ}	5.5	3.6 5.5	—	±5	μA	V _{I (CONT)} = V _{IH} or V _{IL} , V _O = V _{CCA} , V _{CCB} or GND
Output leak current	I _{OFF}	0	0	—	20	μA	A port, V _{I/O} = 5.5 V, B port, V _{I/O} = 3.6 V
Quiescent supply current	I _{CCA}	5.5	OPEN	—	80	μA	A _n = V _{CCA} or GND, Control input = V _{CCA}
		5.5	3.6	—	80		B to A, Control input = V _{CCA} or GND
	I _{CCB}		5.5	3.6	—	50	μA
		5.5		—	80		
Increase in I _{CC} per input ^{*1}	ΔI _{CCA}	5.5	5.5	—	1.5	mA	A port or Control input, One input at V _{CCA} -2.1 V, Other input at V _{CCA} at GND
	ΔI _{CCB}	5.5	3.6	—	0.5		B port, One input at V _{CCB} -0.6 V, Other input at V _{CCB} or GND Control input at GND

Notes: For condition shown as Min or Max, use the appropriate values under recommended operating conditions.

1. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

(Ta = 25°C)

Item	Symbol	V _{CCA} (V)	V _{CCB} (V)	Min	Typ	Max	Unit	Test Conditions
Control Input, capacitance	C _{IN}	5	3.3	—	5	—	pF	V _I = V _{CCA} or GND
Input / output capacitance	C _{I/O}	5	3.3	—	11	—	pF	A port, V _I = V _{CCA} or GND, B port, V _I = V _{CCB} or GND

Switching Characteristics

($T_a = -40$ to 85°C , $V_{CCA} = 5.0 \pm 0.5$ V, $V_{CCB} = 2.7$ to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	From (Input)	To (Output)
Propagation delay time	t_{PLH}	1	—	7	ns	$C_L = 50$ pF $R_L = 500$ Ω	A	B
	t_{PHL}	1	—	7				
	t_{PLH}	1	—	5.3			B	A
	t_{PHL}	1	—	6.2				
Output enable time	t_{ZH}	1	—	8	ns	$C_L = 50$ pF $R_L = 500$ Ω	\overline{OE}	A
	t_{ZL}	1	—	9				
	t_{ZH}	1	—	10.2			\overline{OE}	B
	t_{ZL}	1	—	10				
Output disable time	t_{HZ}	1	—	5.2	ns	$C_L = 50$ pF $R_L = 500$ Ω	\overline{OE}	A
	t_{LZ}	1	—	5.2				
	t_{HZ}	1	—	7.4			\overline{OE}	B
	t_{LZ}	1	—	5.4				

($T_a = -40$ to 85°C , $V_{CCA} = 5.0 \pm 0.5$ V, $V_{CCB} = 5.0 \pm 0.5$ V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	From (Input)	To (Output)
Propagation delay time	t_{PLH}	1	—	6	ns	$C_L = 50$ pF $R_L = 500$ Ω	A	B
	t_{PHL}	1	—	7.1				
	t_{PLH}	1	—	6.1			B	A
	t_{PHL}	1	—	6.8				
Output enable time	t_{ZH}	1	—	8.3	ns	$C_L = 50$ pF $R_L = 500$ Ω	\overline{OE}	A
	t_{ZL}	1	—	9				
	t_{ZH}	1	—	8.1			\overline{OE}	B
	t_{ZL}	1	—	8.2				
Output disable time	t_{HZ}	1	—	4.9	ns	$C_L = 50$ pF $R_L = 500$ Ω	\overline{OE}	A
	t_{LZ}	1	—	4.7				
	t_{HZ}	1	—	6.3			\overline{OE}	B
	t_{LZ}	1	—	5.4				

Operating Characteristics

Item	Symbol	V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	5.0	3.0	—	20	—	pF	$f = 10$ MHz, $C_L = 0$

Power-up considerations

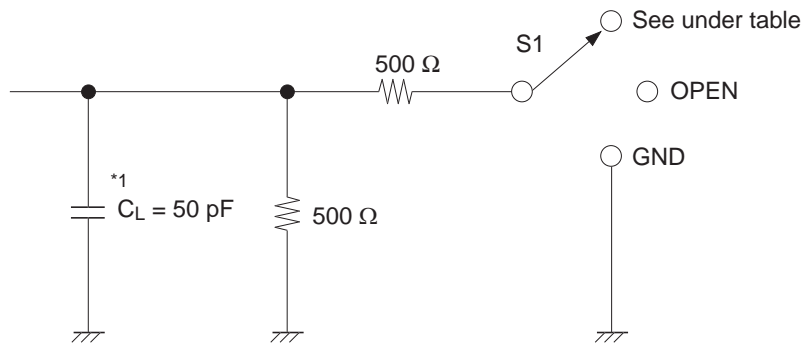
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device.
(Power up of V_{CCA} is first. Next power up is V_{CCB} .)
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low.
If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

Test Circuit

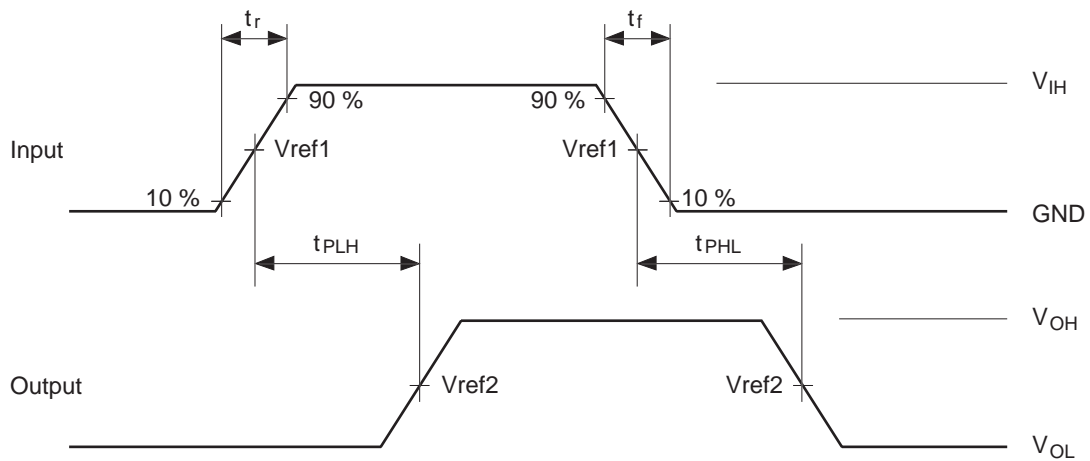


Load circuit for outputs

Symbol	S1			
	$V_{CCA} = 5 \pm 0.5 \text{ V}$ $V_{CCB} = 2.7 \text{ to } 3.6 \text{ V}$		$V_{CCA} = 5 \pm 0.5 \text{ V}$ $V_{CCB} = 5 \pm 0.5 \text{ V}$	
	A/ $\overline{\text{OE}}$ to B	B/ $\overline{\text{OE}}$ to A	A/ $\overline{\text{OE}}$ to B	B/ $\overline{\text{OE}}$ to A
t_{PLH} / t_{PHL}	OPEN	OPEN	OPEN	OPEN
t_{ZH} / t_{HZ}	GND	GND	GND	GND
t_{ZL} / t_{LZ}	6 V	$2 \times V_{CCA}$	$2 \times V_{CCB}$	$2 \times V_{CCA}$

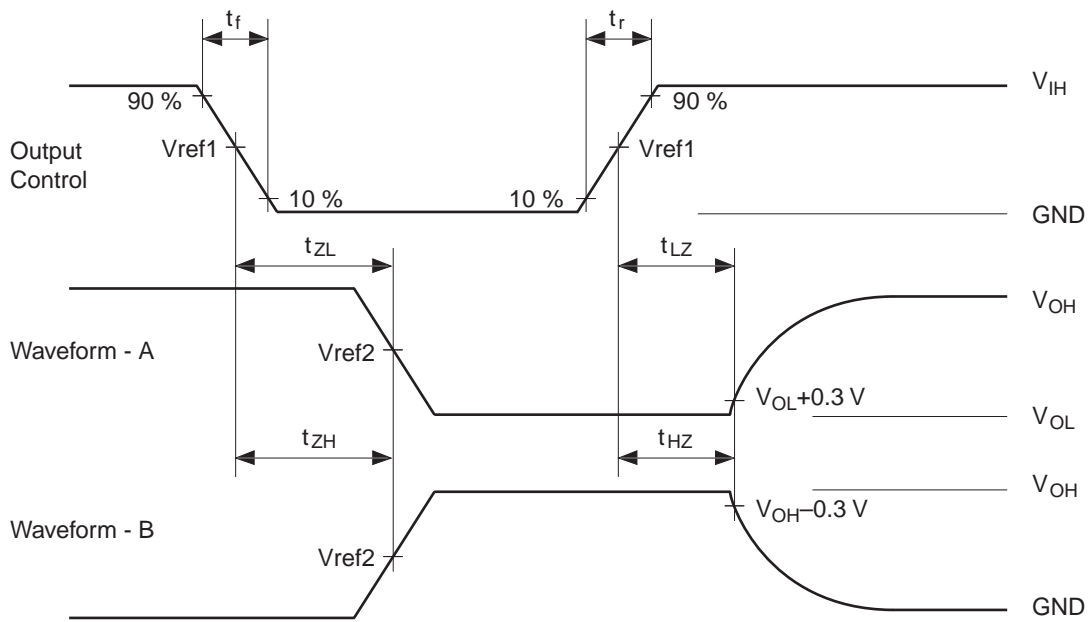
Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1



Symbol	$V_{CCA} = 5 \pm 0.5 \text{ V}$ $V_{CCB} = 2.7 \text{ to } 3.6 \text{ V}$		$V_{CCA} = 5 \pm 1.5 \text{ V}$ $V_{CCB} = 5 \pm 0.5 \text{ V}$	
	A to B	B to A	A to B	B to A
V_{IH}	3.0 V	2.7 V	3.0 V	V_{CCB}
Vref1	1.5 V	1.5 V	1.5 V	$1/2 V_{CCB}$
Vref2	1.5 V	$1/2 V_{CCA}$	$1/2 V_{CCB}$	$1/2 V_{CCA}$

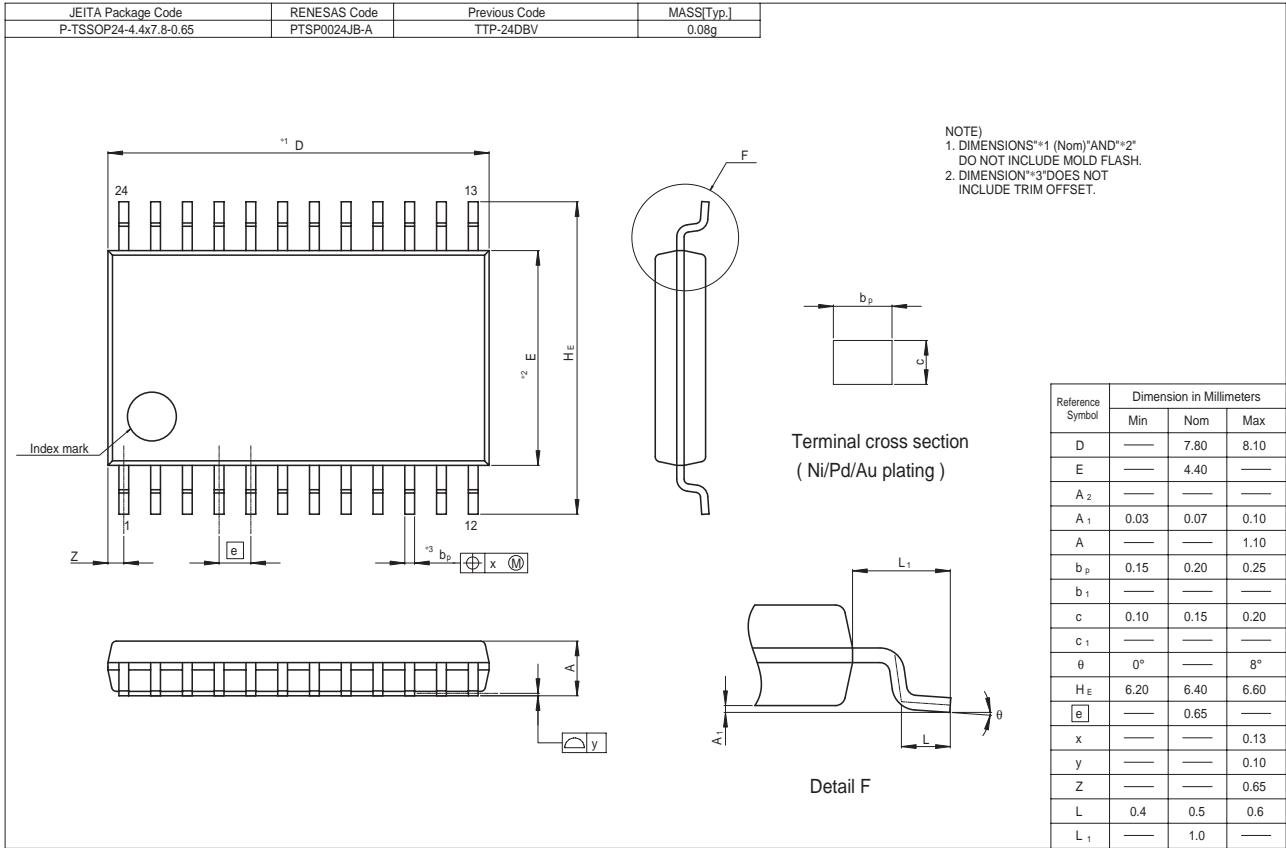
Waveforms – 2



Symbol	$V_{CCA} = 5 \pm 0.5 V$ $V_{CCB} = 2.7 \text{ to } 3.6 V$		$V_{CCA} = 5 \pm 0.5 V$ $V_{CCB} = 5 \pm 0.5 V$	
	\overline{OE} to B	\overline{OE} to A	\overline{OE} to B	\overline{OE} to A
V_{IH}	3.0 V	3.0 V	3.0 V	3.0 V
V_{ref1}	1.5 V	1.5 V	1.5 V	1.5 V
V_{ref2}	1.5 V	$1/2 V_{CCA}$	$1/2 V_{CCB}$	$1/2 V_{CCA}$

- Notes:
1. All input pulses are supplied by generators having the following characteristics :
 $PRR \leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001