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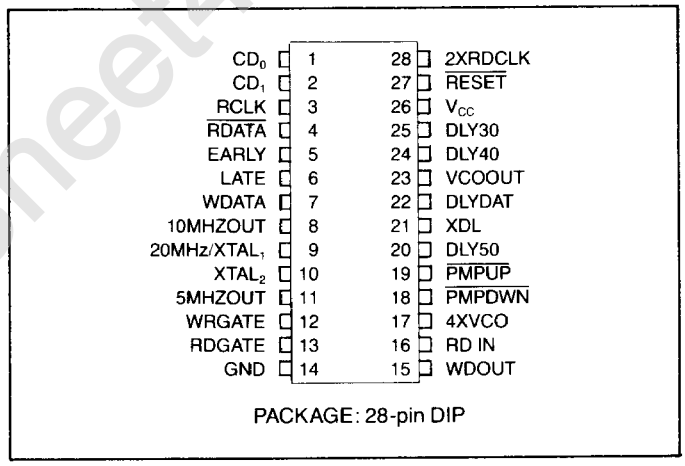
HDC 9227
PRELIMINARY

High Performance Dual (Hard/Floppy Disk) Data Separator DDS

FEATURES

- ☐ Single chip combines high performance analog hard disk data separator and high resolution digital floppy disk data separator
- ☐ Significantly reduces component count in hard disk and floppy systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Eliminates all tuning and tweaking normally required by analog data separators
- ☐ Built-in hard disk write precompensation logic
- ☐ Fabricated in CMOS technology
- ☐ Single +5V supply
- ☐ TTL Compatible

PIN CONFIGURATION



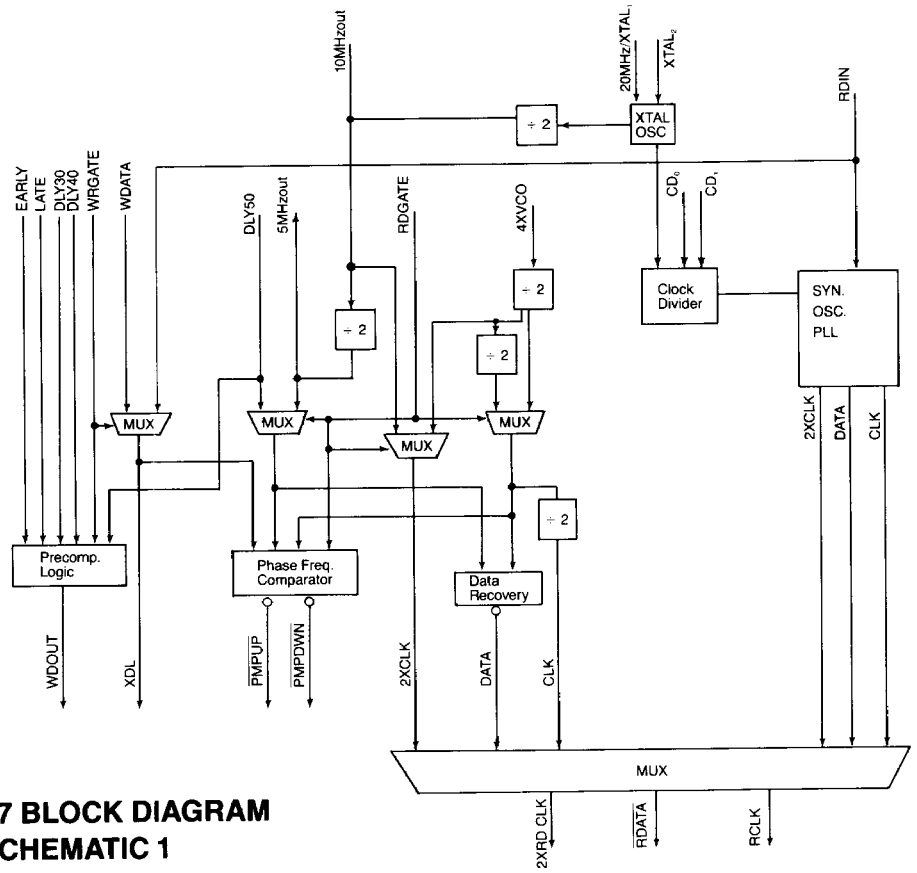
PACKAGE: 28-pin DIP

GENERAL DESCRIPTION

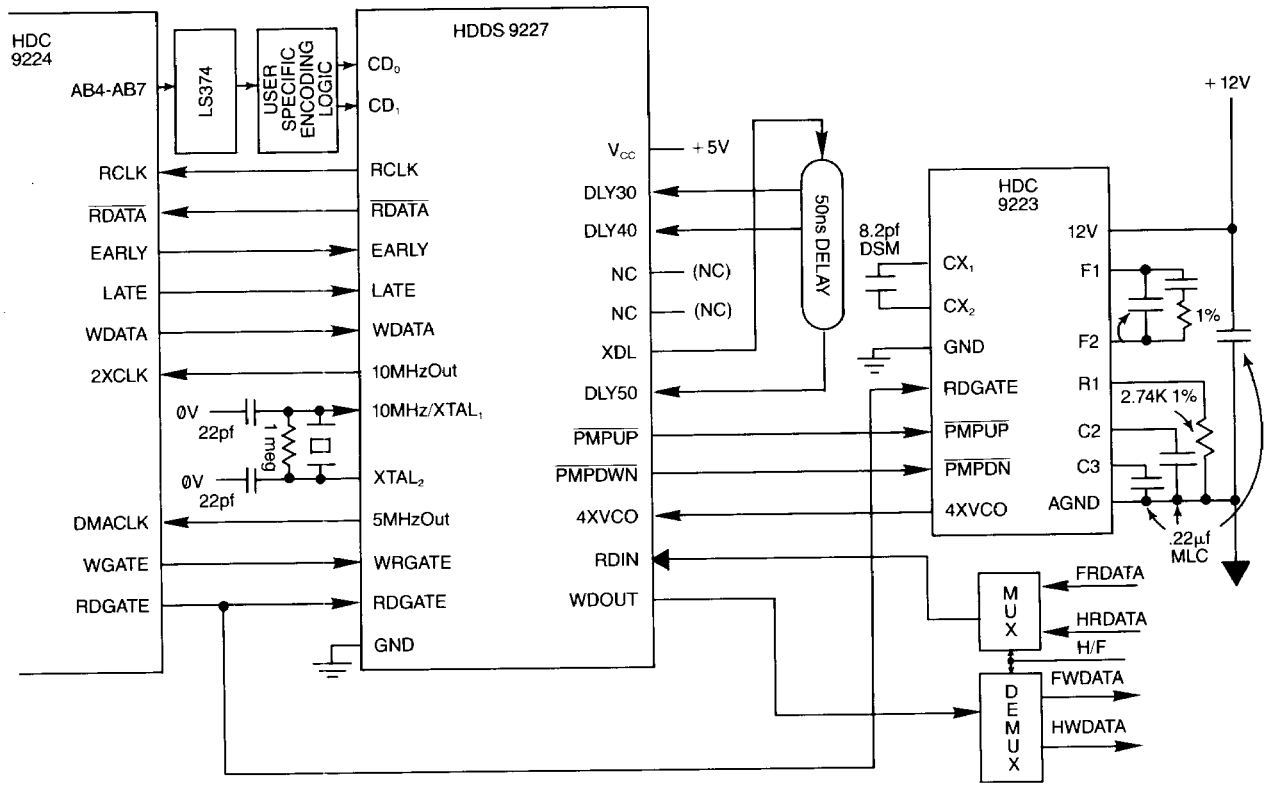
The HDC 9227 Universal Disk Data Separator (UDDS) is a 28 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of the hard disk/floppy disk sub-system.

Internally, a precision floppy disk digital data separator is combined with the digital portion of a high performance, self tuning analog hard disk data separator.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9227 simplifies the task of the system designer.



HDC 9227 BLOCK DIAGRAM
SCHEMATIC 1



TYPICAL CIRCUIT CONFIGURATION
SCHEMATIC 2

DESCRIPTION OF PIN FUNCTIONS

PIN #	NAME	SYMBOL	DESCRIPTION
1, 2	CLOCK DIVISOR 0 AND 1	CD_0, CD_1	CD_0 and CD_1 control the internal clock divider circuit and hard/floppy mode. See table 1.
3	READ CLOCK	RCLK	For hard disks this clock has a nominal frequency of 5 MHz and defines the half bit boundaries of the RDATA output. For floppy disks it is the clock derived from the floppy disk drive serial bit stream.
4	READ DATA	$\overline{\text{RDATA}}$	This output is a regenerated version of the raw read data from the drive, either hard or floppy, which satisfies the timing of the HDC 9224.
5	EARLY	EARLY	This input is generated by the Hard Disk Controller. In the hard disk mode it causes the data separator to output WDOUT early with respect to WDATA. In the floppy mode this input has no effect, as floppy precompensation is provided by the HDC 9224.
6	LATE	LATE	This input is generated by the Hard Disk Controller. In the hard disk mode it causes the data separator to output WDOUT late with respect to WDATA. In the floppy mode this input has no effect, as floppy precompensation is provided by the HDC 9224.
7	WRITE DATA	WDATA	This input is the write waveform generated by the Hard Disk Controller. In the hard disk mode this waveform is passed through the data separator and is delayed according to the write precompensation inputs EARLY and LATE. When in the floppy mode precompensation is handled by the HDC 9224.
8	10 MHz OUTPUT	10MHzOUT	This output is a 10 MHz signal derived from $XTAL_1$ and $XTAL_2$. It is typically used as a 10 MHz clock for the HDC 9224.
9, 10	CRYSTAL 1, 2	20MHz/$XTAL_1$ $XTAL_2$	A 20 MHz crystal may be connected between these two pins. If a TTL signal is used in place of a crystal, the TTL signal should be connected to the 20 MHz/$XTAL_1$ input and the $XTAL_2$ output should be disconnected.
11	5 MHz OUTPUT	5MHzOUT	This output is the 10 MHz output divided by two. It is normally connected to the HDC 9224 DMACLK input when the HDC 9225 chip is not being used.
12	WRITE GATE	WRGATE	This is the WRITE GATE input generated by the Hard Disk Controller. When low, the signal at the RDIN input is selected and output to the delay line via the XDL pin. When high (write mode), the signal at the WDATA input is selected and output to the delay line via the XDL pin for precompensation purposes (hard disk mode).
13	READ GATE	RDGATE	In hard disk mode, this active-high input signal, upon assertion, will permit the VCO to begin locking on the incoming data from the drive. When RDGATE is low, the VCO will lock on to a 5 MHz signal (20 MHz/4).
14	GROUND	GND	This is the ground pin for the device.
15	WRITE DATA OUT	WDOUT	This output is the precompensated WDATA signal. This output is the write data signal connected to the hard or floppy drive.
16	READ DATA IN	RDIN	This input receives data from the drive.
17	4XVCO	4XVCO	This signal is the output of the external VCO and runs at a frequency equal to four times the hard disk data rate. This signal is divided by two and then feeds the phase comparator to generate the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ signal. It is also divided by four and output as the RCLK signal when in the hard disk mode.
18	PUMP DOWN	$\overline{\text{PMPDWN}}$	When asserted low, this output will decrease the frequency of the VCO.
19	PUMP UP	$\overline{\text{PMPUP}}$	When asserted low, this output will increase the frequency of the VCO.
20	DELAY50	DLY50	This input is a 50ns delay of the XDL signal. The 50ns tap is used to arm the phase detector and to create a reclocked version of the raw read data from the hard disk drive. This input is also used (in conjunction with DLY40 and DLY30) to generate the hard disk precompensation delays.

DESCRIPTION OF PIN FUNCTIONS

PIN #	NAME	SYMBOL	DESCRIPTION
21	XDL	XDL	During write operations when WGATE is asserted, this output is identical to WDATA. XDL is output to the delay line thus creating precise delays which are used during write precompensation. When WGATE is not asserted, this output is the raw read data on the RDIN input. XDL is output to the delay line and is used to provide proper arming for the phase comparator and clocking for the reclocking circuitry.
22	TEST OUTPUT	DLYDAT	Leave disconnected.
23	TEST OUTPUT	VCOOUT	Leave disconnected.
24, 25	DELAY40 DELAY30	DLY 40, DLY 30	These inputs are delays of 40 and 30ns of the XDL signal. The 40, 50 and 30ns delays are used respectively for nominal, late and early positioning of the bits respectively in the WDOUT signal when in the hard disk mode.
26	5 VOLTS	+5V	This pin is the +5V power pin for the device.
27	RESET	$\overline{\text{RESET}}$	For test only. Connect to +5V or leave disconnected.
28	2XRDCLK	2XRDCLK	When in the HARD DISK mode this output is nominally 10 MHz. When in the FLOPPY mode this output is nominally 250KHz, 500KHz or 1 MHz depending on the selected transfer rate. NOTE: This output is undefined when switching between data rates, modes and during "LOCK TIME" associated with the switching of RDGATE.

DESCRIPTION OF OPERATION

The HDC 9227 contains a complete, high performance, digital data separator for floppy disk use as well as the digital portion of an analog data separator for hard disk use.

HARD DISK MODE

(Selected when BOTH CD_0 and $CD_1 = 0$)

When in the hard disk mode, the HDC 9227, in conjunction with the HDC 9223, an external tapped delay line and filter (shown in Schematic 2) allows a system designer to implement a phase locked loop to perform phase and frequency locking onto MFM encoded data from a Winchester hard disk.

In MFM format a pulse on RDIN corresponds not to a 1 or a 0 but to a flux transition on the media. These flux transitions can be spaced at T, 1.5T, or 2T, time intervals where the data transfer bit rate is T = 1/Freq. For the ST 506 drive, Freq. = 5MHz and the flux transitions may be spaced at 200, 300 or 400 nanoseconds.

Due to the phenomena of magnetic storage, the bit spacing is not constant but instead will vary due to magnetic effects and drive rotational speed variation. To compensate for this, the HDC 9227 takes the Read Data from the drive and generates two signals, $\overline{\text{RDATA}}$ and RCLK. The RCLK signal, derived from the VCO, changes period as a function of the variations in the disk data, permitting the data from the drive to be correctly clocked into the HDC 9224 independent of bit spacing variations on the media.

The VCO runs nominally at 20 MHz since the bit spacing can change in 100 ns increments and the oscillator must have the ability to adjust its frequency at this interval. The HDC 9227 divides 4XVCO by 2 and compares the phase of this signal to the incoming data. The positive edge of RDIN arms the phase detector for sampling the phase of the two signals. The positive edge of 4XVCO/2 asserts $\overline{\text{PMPDN}}$. The positive edge of DLY50 asserts $\overline{\text{PMPUP}}$. Sampling is terminated when $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDN}}$ are both asserted. The signal RCLK is generated by dividing 4XVCO by four.

When the HDC 9224 wants to read data from the disk, it asserts RGATE. This signal tells the phase locked loop to acquire bit synchronization. If Read Gate is inactive, the VCO will be locked to a crystal controlled signal of 5 MHz.

The HDC 9227 also performs hard disk write precompensation. Certain bit patterns, when written and then read back, are shifted either late or early depending on the bit pattern. Since this "bit" or "peak shift" is predictable, intentionally writing these bits late or early will compensate for the shift during read back.

The HDC 9224 recognizes these patterns, and in addition to producing the write data waveform, will generate the signals EARLY or LATE to allow the HDC 9227 to write the bits at the appropriate time. Typically, bits are written early or late by 10 ns. The last 3 taps of the delay line allow the HDC 9227 to implement the precompensation as a function of the EARLY and LATE signals. The final output write waveform is presented to the drive on the WDOUT pin.

FLOPPY DISK MODE

(Selected when either CD_0 or $CD_1 = 1$)

When in the floppy mode the high performance digital data separator will accept data from the drive at 125K, 250K, or 500K data rates and output the appropriate regenerated clock and data signals.

The heart of the digital floppy disk data separator section is a synthetic oscillator phase locked loop. One half-bit cell of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of 20 phase slices. The circuit therefore needs a phase slice clock with a frequency of 20 times the half-bit cell time.

Detection of an input pulse away from the center "slot" of the half-bit cell causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit cell closer to the pulse.

A short history of input pulse detections (which induce phase corrections by the HDC 9227) is kept. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency, and helps compensate for drive speed variations.

Since the HDC 9227 provides a precompensated WDOUT (write data output) for floppy disks, this signal can be tied directly to the floppy drive and contains the precompensated write data required by the drive.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec) ..... +300 C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} +0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, V_{CC} = 5.0V, ±5%)

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT				
I_{CC}			mA	
OUTPUT VOLTAGE				
V_{OH}	2.4		V	I_{OH} = 400uA (All outputs except 10MHzOUT and 5MHzOUT)
V_{OH}	4.3		V	I_{OH} = 400 uA (10MHzOUT and 5MHzOUT)
V_{OL}		0.4	V	I_{OL} = 2.0 mA
INPUT VOLTAGE				
V_{IH}	2.0		V	(For all inputs except $XTAL_1$ and 4XVCO)
V_{IL}		0.8	V	(For all inputs except $XTAL_1$ and 4XVCO)
V_{IH}	3.5		V	(For $XTAL_1$ and 4XVCO)
V_{IL}		1.5	V	(For $XTAL_1$ and 4XVCO)
INPUT CURRENT				
I_{IH}		10	µA	V_{IH} = 2.0V
I_{IL}		10	µA	V_{IL} = 0.4V

PRELIMINARY
Notice: This is not a final specification.
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AC ELECTRICAL CHARACTERISTICS (TA = 0C to +70C, V_{CC} = 5.0V, ±5%)

Symbol	Min.	Typ.	Max.	Unit	Comments
T_1			70	ns	figure 1
T_2			80	ns	figure 1
T_3			65	ns	figure 3
T_4			70	ns	figure 3
T_5			100	ns	figure 5
T_6			100	ns	figure 5
T_{11}			65	ns	figure 2
T_{12}			65	ns	figure 2
T_{13}			65	ns	figure 2
T_{14}			65	ns	figure 2
T_{15}			45	ns	figure 4
T_{16}			45	ns	figure 6
T_{17}			45	ns	figure 8
T_{18}	45	50	55	ns	figure 9
T_{19}	25			ns	figure 10
T_{20}	25			ns	figure 11
T_{21}	6			ns	figure 12
T_{22}	50			ns	figure 12
T_{23}	25		100	ns	figure 12
T_{24}				ns	figure 7
T_{25}				ns	figure 7
T_{26}				ns	figure 7
T_{27}				ns	figure 7
T_{28}				ns	figure 7
T_{29}				ns	figure 7

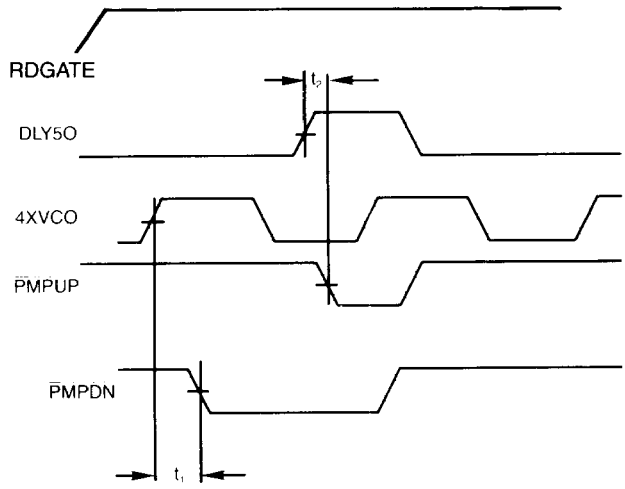


FIGURE 1

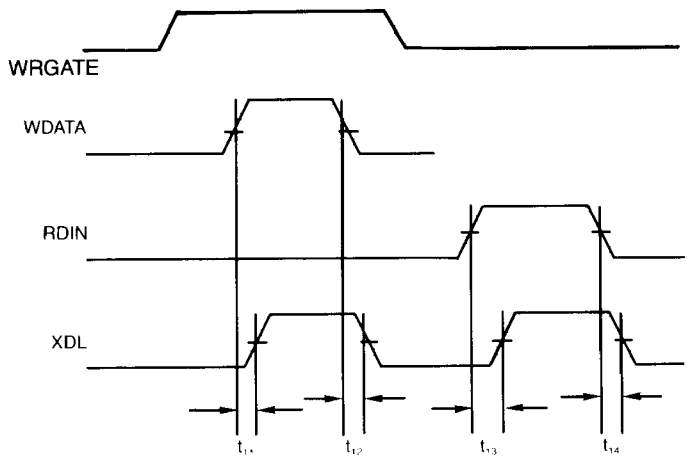


FIGURE 2

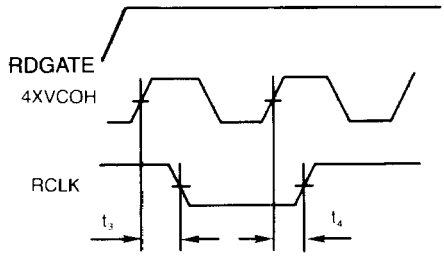


FIGURE 3

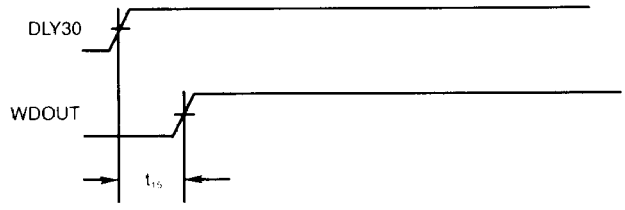


FIGURE 4

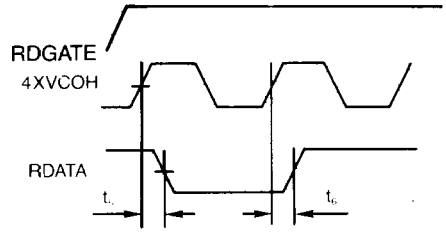


FIGURE 5

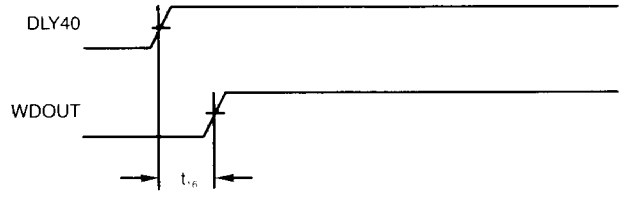


FIGURE 6

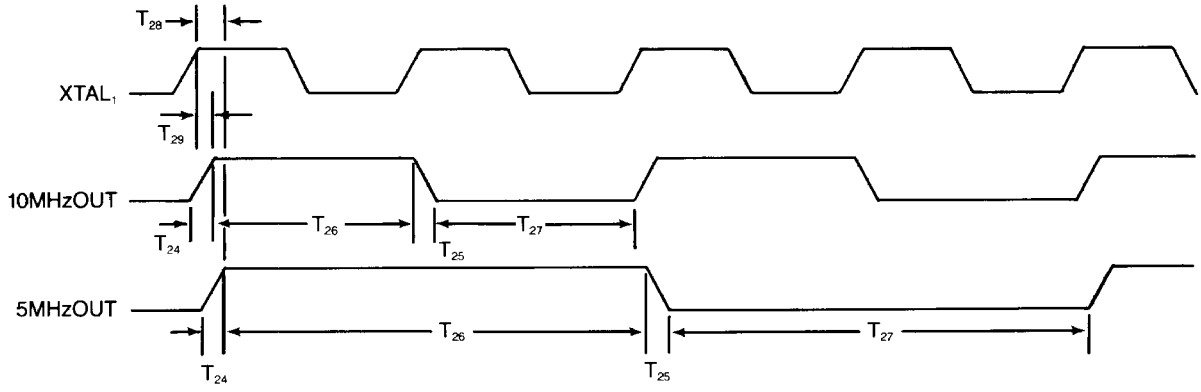


FIGURE 7

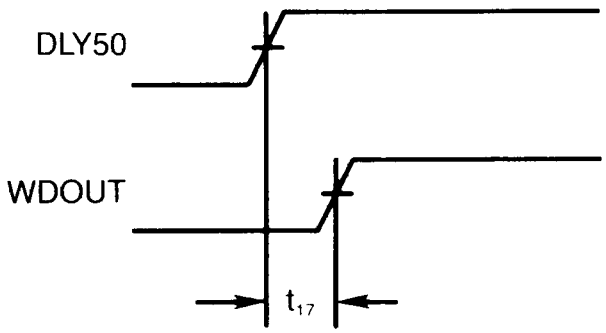
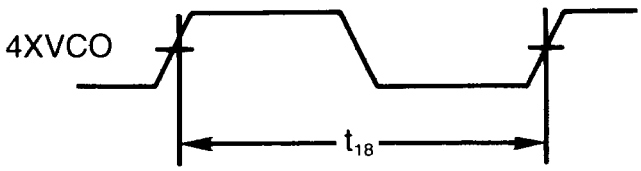


FIGURE 8



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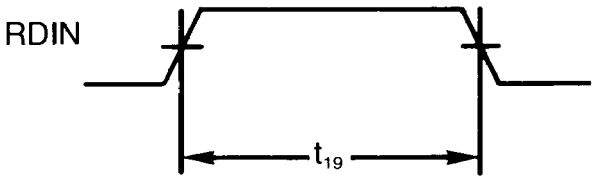

FIGURE 10

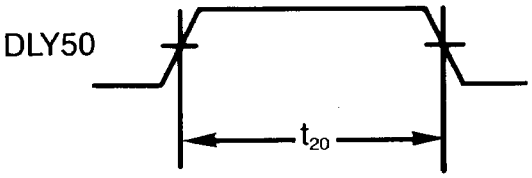

FIGURE 11

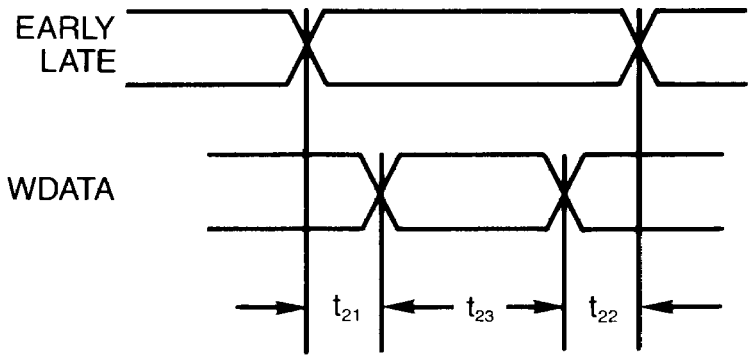

FIGURE 12

CD_1	CD_0	Clock Rate	Data Rate	Drive Type and Mode
0	0	10 MHz	5 Mbs	Hard Disk, MFM
0	1	20 MHz	500 Kbs	Floppy, MFM
1	0	10 MHz	250 Kbs	Floppy, FM or MFM
1	1	5 MHz	125 Kbs	Floppy, FM

TABLE 1.