The HP HDCS Family of CMOS Image Sensors

HP Part Number HDCS-2000/2100/1000/1100
Product Technical Specification
Revision 3.0

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1. Sensor Overview

1.1 Description

HDCS-2000/2100(VGA) and HDCS-1000/1100(CIF) are CMOS active pixel image sensors with integrated A/D conversion and full timing control. They provide random access of sensor pixels which allows windowing and panning capabilities. The sensor is designed for video conferencing applications and still image capabilities. The HDCS family achieves excellent image quality with very low dark current, high sensitivity, and superior anti-blooming characteristics. The devices operate from a single DC bias voltage, are easy to configure and control, and feature low power consumption.

1.2 Features

- Available in two image array sizes: VGA (640 x 480) and CIF (352 x 288)
- RGB Bayer color filter arrays for the HDCS-2000 and HDCS-1000.
- HDCS-2100 and HDCS-1100 are monochrome versions
- Random access and windowing capability to zoom to any sized window on 4 x 4 pixel boundaries.
- Panning capability to any location within the sensor array.
- Independent X and Y sub-sampling modes (2:1 each) providing a 4X frame rate increase.
- Full frame video rates at 8 bit resolution: 44.5 fps CIF and 15.3 fps VGA at 25 MHz.
- Full frame video rates at 10 bit resolution: 40.8 fps CIF and 14.0 VGA at 25 MHz.
- Still image capability.
- Mechanical shutter and external flash trigger.
- Accumulation mode to aid in determining proper exposure time.
- Low power/standby modes.
- Machine solderable, high temperature tolerant color filter array
- Two 10 bit internal successive approximation analog to digital converters.
- Two integrated differential 8 bit programmable gain amplifiers with independent gain control for each color (R,G,B).
- Integrated voltage references.
- Automatic subtraction of column fixed pattern noise.
- Internal register set programmable via either the UART or Synchronous Serial interface.
- Integrated timing controller with rolling electronic shutter, row/column addressing, and operating mode selection with programmable exposure control, frame rate, and data rate.
- Digital data output via selectable 8/10 bit synchronous parallel interface.
- Programmable horizontal, vertical, and shutter synchronization signals.
- Maskable multi-source level sensitive microcontroller compatible interrupt request signal.
- Single 3.3 volt power supply.

1.3 Applications

- Digital still camera.
- Video conferencing camera.
- Surveillance and security video cameras.
- Automotive
- Machine vision systems.
- Biometric security systems (e.e., fingerprint recognition).
- Toys

1.4 Specifications

Electrical Specifications	
Pixel Size	9 x 9 µ m
Maximum Clock Rate	25 MHz from externally supplied clock source
A/D Dynamic Range	60 db
Pixel Signal-to-Noise Ratio (SNR)	66 db
Noise (Equivalent Electrons) kTC	40 electrons
Dark Current [1]	0.1nA/cm2 at 22 C ambient
Sensitivity [2]	1.1 V/(Lux-S)
Peak Quantum Efficiency [1, 2]	21%
Saturation	1.3V
Full Well Capacity	81,000 electrons
Conversion Gain [2]	16µ V/electron
Programmable Gain Range	1 - 40 (255 increments)
Fill Factor	42%
Exposure Control	0.5 µ sec - 4 sec in 0.5 µ sec steps
Package	44 pin gull wing optical PQFP
Supply Voltage	3.3v, -5/+10%
Power Consumption	200 mW max operating, 3.3 mW max standby
Operating Temperature	-5 to 65 degrees C.

Table 1. Electrical Specifications

Notes: (1) Specified over complete pixel area (2) Measured at unity gain

1.5 HDCS Sensor Top Level Block Diagram

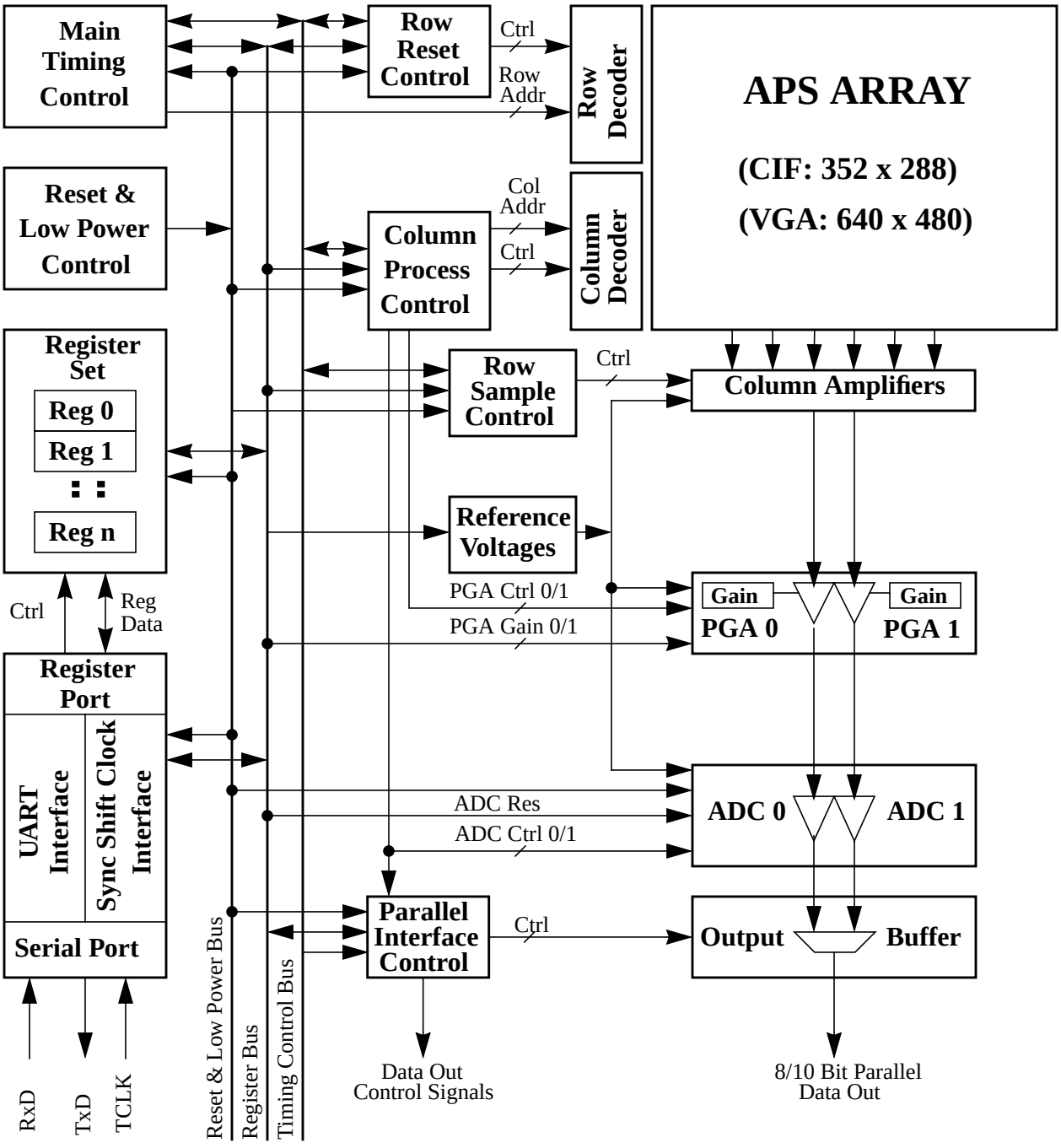


Figure 1. Top Level Architectural Block Diagram

1.6 High Level Description of Operation

HDCS Sensors are controlled through a serial interface. The serial interface may be configured as a half-duplex UART slave, or as a Synchronous Serial slave.The serial interface is used to write the system registers to set up the viewing window coordinates, integration/exposure time, frame rate, PGA gain, interrupt masks, status pins functions, output pin switching speed, output data format, and output data timing.

A system reset must be performed by asserting the nRST pin before operation may begin.

The CONFIG register selects one of the three operating modes: 1) normal, 2) accumulation, 3) mechanical shutter.The CONFIG register also allows the selection of subsampling mode, and either single frame capture mode, or continuous run mode. Operation begins when the RUN bit in the CONTROL register is set.

The following discussion pertains to operation in normal mode.

When operation begins the timing generator resets the top pixel row of the viewing window. After a pixel row is reset it begins integration. After one Row Process time elapses the next row is reset. This continues until the bottom row of the viewing window is reached. In continuous run mode this process repeats by wrapping to the top row of the viewing window. In single frame capture mode the process ends when the bottom row of the viewing window is reached. In continuous run mode if the integration time is less than the time to cycle through a frame there is no overhead time between frames. If the integration time is greater than the time to cycle through a frame there is an overhead delay between frames equal to integration time minus the time to cycle through a frame.

Row Processing has 2 parts: 1) Row Sample followed by 2) Column Processing. Row Sampling consists of selecting a row and reading it into the analog row buffer. Column processing consists of reading pixel data out of the analog row buffer, converting it to digital data, then outputting the digital value from the chip. Column Processing time depends on the input clock (CLK) speed, and the TCTRL system register. See the Register Set chapter and Programmer reference for more details.

The output portion of Column Processing is suppressed until the first row finishes integration. Therefore if the integration time equals 8 Row Process times, data for Row (N) is begin read out, while Row (N+8) is being reset. After the initial overhead of waiting for the first row to integrate, during each Row Process time one row is being reset, and a different row is being read out.

When the a row has finished integration it is transferred to the analog row buffer using double correlated sampling and reference column subtraction, then Column Processing begins.

Column Processing reads data out of the analog row buffer in pixel pairs. The pixel pairs are processed by 2 parallel channels. The first row is an even row. Even rows are green-red rows from the bayer filter pattern. The first pixel of a green-red row is a green pixel. Odd rows are blue-green rows of the bayer filter pattern. The first pixel of a blue-green row is a blue pixel. Each pixel is transmitted through a PGA (programmable gain amplifier). Pixels are amplified by different values corresponding to the pixel position in the 2 by 2 block of the RGB bayer color filter pattern. In other words each color (R/G/B) is amplified by a different number. Each ADC (analog to digital converter) channel converts the analog PGA output to a 10 bit digital value. The ADC values for both channels are output in sequential order on the parallel DATA pins along with the assertion of the DRDY pin. The timing of the DATA and DRDY pins is programmable. Column Processing con-

tinues until all the pixels for the viewing window have been output on the DATA pins. The nROW status signal is asserted when the data for the last pixel of the row has been output.

When nROW is asserted for the bottom row of the viewing window, nFRAME is also asserted.

If the CFC bit of the CONFIG register equals ‘0’, then the Sensor is in single frame mode. In single frame mode if the nIRQ_nCC (interrupt/capture complete) status pin is enabled as capture complete, then nIRQ_nCC is asserted at the same time as nFRAME. The RF (run flag) is turned off in the STATUS register and the sensor idles until it is told to run another frame.

If the CFC bit of the CONFIG register equals ‘1’, then HDCS Sensor is in continuous run mode. In continuous run mode after the assertion of nFRAME, the sensor immediately begins the next frame which has already started integrating. If integration time is less than the time to cycle through 1 frame, then there is no delay between the processing of the bottom row of frame X and the top row of frame X+1. If integration time is greater than the time to cycle through 1 frame, then there is a delay between the bottom row of frame X and the top row of frame X+1. They delay equals integration time minus the time to cycle through one frame.

Continuous Run mode is terminated by resetting the RUN bit of the CONTROL register. Single Frame mode may also be terminated by de-asserting the RUN bit. If the SFC (stop when frame complete) bit of the CONFIG register is set when the RUN bit is de-asserted HDCS Sensor will process until nFRAME is asserted at the normal time, then return to idle. If the SFC (stop when frame complete) bit of the CONFIG register is not set when the RUN bit is de-asserted EYRIS/PUPIL will immediately assert nFRAME, nROW, and nIRQ_nCC and return to the idle state. If enabled for the capture complete function, the nIRQ_nCC (interrupt/capture complete) status flag is asserted at the same time as nFRAME for the last frame.

TIME = 1

Row 0	**RESET(0)**
Row 1	
Row 2	
Row 3	
Row 4	
Row 5	

TIME = 2

Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	
Row 3	
Row 4	
Row 5	

TIME = 3

Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	

TIME = 4

Row 0	**READ(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

TIME = 5

Row 0	
Row 1	**READ(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

TIME = 6

Row 0	
Row 1	
Row 2	**READ(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

TIME = 7

Row 0	**RESET(0)**
Row 1	
Row 2	
Row 3	**READ(3)**
Row 4	**INTEGRATE(2)**
Row 5	**INTEGRATE(1)**

TIME = 8

Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	
Row 3	
Row 4	**READ(3)**
Row 5	**INTEGRATE(2)**

TIME = 9

Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	**READ(3)**

TIME = 10

Row 0	**READ(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

TIME = 11

Row 0	
Row 1	**READ(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

TIME = 12, goto time=7

Row 0	
Row 1	
Row 2	**READ(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Figure 2. Example of 6 row view window with integration time = 2 rows.

TIME = 1

Row 0	**RESET(0)**
Row 1	
Row 2	
Row 3	
Row 4	
Row 5	

TIME = 2

Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	
Row 3	
Row 4	
Row 5	

TIME = 3

Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	

TIME = 4

Row 0	**INTEGRATE(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

TIME = 5

Row 0	**INTEGRATE(4)**
Row 1	**INTEGRATE(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

TIME = 6

Row 0	**INTEGRATE(5)**
Row 1	**INTEGRATE(4)**
Row 2	**INTEGRATE(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

TIME = 7

Row 0	**INTEGRATE(6)**
Row 1	**INTEGRATE(5)**
Row 2	**INTEGRATE(4)**
Row 3	**INTEGRATE(3)**
Row 4	**INTEGRATE(2)**
Row 5	**INTEGRATE(1)**

TIME = 8

Row 0	**INTEGRATE(7)**
Row 1	**INTEGRATE(6)**
Row 2	**INTEGRATE(5)**
Row 3	**INTEGRATE(4)**
Row 4	**INTEGRATE(3)**
Row 5	**INTEGRATE(2)**

TIME = 9

Row 0	**READ(8)**
Row 1	**INTEGRATE(7)**
Row 2	**INTEGRATE(6)**
Row 3	**INTEGRATE(5)**
Row 4	**INTEGRATE(4)**
Row 5	**INTEGRATE(3)**

TIME = 10

Row 0	**RESET(0)**
Row 1	**READ(8)**
Row 2	**INTEGRATE(7)**
Row 3	**INTEGRATE(6)**
Row 4	**INTEGRATE(5)**
Row 5	**INTEGRATE(4)**

TIME = 11

Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	**READ(8)**
Row 3	**INTEGRATE(7)**
Row 4	**INTEGRATE(6)**
Row 5	**INTEGRATE(5)**

TIME = 12

Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	**READ(8)**
Row 4	**INTEGRATE(7)**
Row 5	**INTEGRATE(6)**

TIME = 13

Row 0	**INTEGRATE(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	**READ(8)**
Row 5	**INTEGRATE(7)**

TIME = 14

Row 0	**INTEGRATE(4)**
Row 1	**INTEGRATE(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	**READ(8)**

TIME = 15, goto time=7

Row 0	**INTEGRATE(5)**
Row 1	**INTEGRATE(4)**
Row 2	**INTEGRATE(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Figure 3. Example of 6 row view window with integration time = 7 rows

2. Register Set

2.1 Register List and Address Map

The registers used to configure and control the HDCS sensor are organized as a sequential array of 8 bit registers. The register names, mnemonics, size, and offset from the chip base address are listed here:

Register Name	Mnemonic	Address (hex)
Identifications Register	IDENT	0x00
Status Register	STATUS	0x01
Interrupt Mask Register	IMASK	0x02
Pad Control Register	PCTRL	0x03
Pad Drive Control Register	PDRV	0x04
Interface Control Register	ICTRL	0x05
Interface Timing Register	ITMG	0x06
Baud Fraction Register	BFRAC	0x07
Baud Rate Register	BRATE	0x08
ADC Control Register	ADCCTRL	0x09
First Window Row Register	FWROW	0x0A
First Window Column Register	FWCOL	0x0B
Last Window Row Register	LWROW	0x0C
Last Window Column Register	LWCOL	0x0D
Timing Control Register	TCTRL	0x0E
PGA Gain Register: Even Row, Even Column	ERECPGA	0x0F
PGA Gain Register: Even Row, Odd Column	EROCPGA	0x10
PGA Gain Register: Odd Row, Even Column	ORECPGA	0x11
PGA Gain Register: Odd Row, Odd Column	OROCPGA	0x12
Row Exposure Low Register	ROWEXPL	0x13
Row Exposure High Register	ROWEXPH	0x14
Sub-Row Exposure Low Register	SROWEXPL	0x15
Sub-Row Exposure High Register	SROWEXPH	0x16
Configuration Register	CONFIG	0x17
Control Register	CONTROL	0x18

Table 2. Register Set Declaration

2.2 Register Descriptions

2.2.1 IDENT: Identification Register

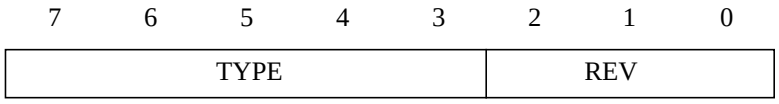


Figure 4. Identification Register Format

Mnemonic	Read/Write Control	Description
REV	R	Revision. **REV** 000 : Revision A. 0001 - 111 : Reserved.
TYPE	R	Chip Type. **TYPE** 00000 : HDCS - 2000/2100 00001 : HDCS - 1000/1100 00010 - 11111 : Reserved
RSV	N/A	Reserved

Table 3. Identification Register bit descriptions

2.2.2 STATUS: Status Register

	7	6	5	4	3	2	1	0
	RSV	SSF	IEF	EEF	CC	FC	RC	RF
Reset Value	X	0	0	0	0	0	0	0

Figure 5. Status Register Format

Mnemonic	Read/Write Control	Description
RF	R	Run flag. When 1, indicates an image capture process is executing. When 0, indicates no image capture process is executing.
RC	R/W	Row Complete flag. When 1, indicates a row has been completed since RC flag last cleared. When 0, indicates a row has not been completed since RC flag last cleared. Clear by writing a 1 to the RC flag.
FC	R/W	Frame Complete flag. When 1, indicates a frame has been completed since FC was last cleared. When 0, indicates a frame has not been completed since FC flag was last cleared. Clear by writing a 1 to the FC flag.
CC	R/W	Image Capture Complete flag. When 1, indicates an image capture process has been completed since CC flag last cleared. When 0, indicates an image capture process has not been completed since the CC flag was last cleared. Clear by writing a 1 to the CC flag.
EEF	R	Exposure Error Flag. When 1, indicates an exposure error was detected since the flag was last cleared. When 0, indicates no exposure error has been detected. Clear iby writing a 1to EEF flag and correcting the exposure settings.
IEF	R/W	Interface error Flag. When 1, indicates an error was detected by the interface controller since the flag was last cleared. When 0, indicates no serial interface error has been detected since the flag was last cleared. Clear by writing a 1 to IEF.
SSF	R/W	Shutter Sync Flag. When 1, indicates that all rows in the selected image window have been reset while running in the “shutter mode” and that the timing controller has started a delay period to allow the host system to activate either a mechanical shutter or strobe light since the flag was last cleared. When 0, indicates no shutter synchronization event has been detected since the flag was last cleared. Clear by writing a 1 to SSF.
RSV	N/A	Reserved

Table 4. Status Register bit descriptions

2.2.3 IMASK: Interrupt MaskRegister

	7	6	5	4	3	2	1	0
	RSV	ISS	IIE	IEE	ICC	IFC	IRC	IEN
Reset Value	X	0	0	0	0	0	0	0

Figure 6. Interrupt Mask Register format

Mnemonic	Read/Write Control	Description
IEN	R/W	Interrupt Enable. When 1, active and enabled interrupt sources will generate an interrupt. When 0, all interrupts are disabled.
IRC	R/W	Interrupt when Row Complete. When 1, an interrupt will be asserted after completion of each row. When 0, no row complete interrupt will be asserted.
IFC	R/W	Interrupt when Frame Complete. When 1, an interrupt will be asserted after completion of each frame. When 0, no frame complete interrupt will be asserted.
ICC	R/W	Interrupt when Capture Complete. When 1, an interrupt will be asserted after completion of each image capture process. When 0, no image capture complete interrupt will be asserted.
IEE	R/W	Interrupt when Exposure Error occurs. When 1, an interrupt will be asserted when an exposure setting error is detected. When 0, no interrupt will be asserted when an exposure setting error is detected.
IIE	R/W	Interrupt when interface error occurs. When 1, an interrupt will be asserted when an error is detected on the serial interface channel. When 0, no interrupt will be asserted when an interface error is detected.
ISS	R/W	Interrupt when shutter sync flag set. When 1, an interrupt will be asserted when the shutter synchornization flag of the STATUS register is set. When 0, no interrupt will be asserted when the shutter synchronization flag is set.
RSV	N/A	Reserved

Table 5. Interrupt Mask Register bit descriptions

2.2.4 PCTRL: Pad Control Register

	7	6	5	4	3	2	1	0
	LVC	LVF	LVR	IPD	ICE	FSS	FSE	RCE
Reset Value	0	0	0	0	0	0	0	0

Figure 7. Pad Control Register Format

Mnemonic	Read/Write Control	Description
RCE	R/W	Row Complete Enable. When 1, enables the row complete status output signal (TCLK). When 0, disables the row complete status signal.
FSE	R/W	Frame Complete/Shutter Sync Enable. When 1, enables the multifunction frame complete/shutter sync status output signal (nFRAME_nSYNC). When 0, disables the multifunction frame complete/ shutter sync status signal.
FSS	R/W	Multifunction pin mode select. When 1, the multifunction nFRAME_nSYNC signal is configured to operate as the shutter sync signal. When 0, the multifunction nFRAME_nSYNC signal is configured to operate as the frame complete signal.
ICE	R/W	Image capture complete enable. When 1, the multifunction nIRQ_nCC pin functions as the image capture complete status output. When 0, the multifunctions nIRQ_nCC pin functions as the active low interrupt request output.
IPD	R/W	Interrupt pin internal pull-up disable. When 1, internal circuitry does not drive the nIRQ_nCC output high. When 0, a weak internal pull-up driver is enabled for the nIRQ_nCC output pin. Only applies when the ICE bit is configured for the interrupt request mode.
LVR	R/W	Level row status signal select. When 1, the nROW status signal is asserted for the entire row processing time when it is enabled. When 0, the nROW status signal is asserted for 4 clock cycles at the end of row processing time when it is enabled.
LVF	R/W	Level frame status signal select. When 1, the nFRAME_nSYNC status signal is asserted for the entire frame processing time when it is enabled and configured as the frame complete signal. When 0, the nFRAME_nSYNC status signal is asserted for 4 clock cycles at the end of frame processing time when it is enabled.
LVC	R/W	Level capture complete status signal select. When 1, the nIRQ_nCC status signal is asserted for the entire duration an image capture process is running when the signal is enabled and configured as the capture complete signal. When 0, the nIRQ_nCC status signal is asserted for 4 clock cycles at the end of a completed image capture process time when it is enabled.

Table 6. Pad Control Register Bit Descriptions

2.2.5 PDRV: Pad Drive Control Register

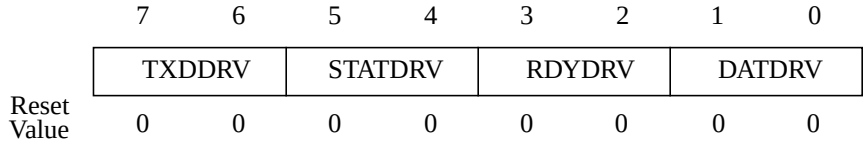


Figure 8. Pad Drive Control Register Format

Mnemonic	Read/Write Control	Description
DATDRV	R/W	Parallel data port drive level select. **DATDRV** 00 : High drive (5 ns) 01 : Medium high drive (10 ns) 10 : Medium low drive (15 ns) 11 : Low drive (20 ns)
RDYDRV	R/W	DRDY signal drive level select. **RDYDRV** 00 : High drive (5 ns) 01 : Medium high drive (10 ns) 10 : Medium low drive (15 ns) 11 : Low drive (20 ns)
STATDRV	R/W	nRow, tclk_nFrame, nIRQ_nCC, status signal output pin drive level select. **STATDRV** 00 : High drive (5 ns) 01 : Medium high drive (10 ns) 10 : Medium low drive (15 ns) 11 : Low drive (20 ns)
TXDDRV	R/W	Serial transmit data signal drive level select. **TXDDRV** 00 : High drive (5 ns) 01 : Medium high drive (10 ns) 10 : Medium low drive (15 ns) 11 : Low drive (20 ns)

Table 7. Pad Drive Control Register Bit Descriptions

2.2.6 ICTRL: Interface Control Register

	7	6	5	4	3	2	1	0
	HAVG	DSC		DDO	DOD		DAD	AAD
Reset Value	0	0	0	0	0	0	0	0

Figure 9. Interface Control Register Format

Mnemonic	Read/Write Control	Description
AAD	R/W	Auto Address Disable. When 0, register addresses are automatically incremented after each register write. When 1, the desired register address must be set prior to each register write.
DAD	R/W	Device Address Disable. When 0, the device address must be included in each serial message packet. When 1, the device address is not included in the serial message packets.
DOD	R/W	Data Output Disable. **DOD** 00 : DATA[9:0] is driven with ADC_data[9:0]. 01 : DATA[1:0] outputs are driven to zero. DATA[9:2] is driven with ADC_data[9:0] rounded up to 8 significant bits. 10 : DATA[1:0] are driven to zero. If ADC_data[9] or ADC_data[8] is one, DATA[9:2] is forced to be xFF, otherwise DATA[9:2] is driven with ADC_data[7:0]. This is called saturation mode 2. 11 : DATA[1:0] are driven to zero. If ADC_data[9] is one, DATA[9:2] is forced to be xFF, otherwise DATA[9:2] is driven with ADC_data[8:1]. This is called saturation mode 1.
DDO	R/W	Delay Data Output. When 0, parallel data outputs switch relative to the rising edge of the system clock. When 1, parallel data outputs switch relative to the falling edge of the system clock.
DSC	R/W	Data Setup cycle count before DRDY is asserted. 00 : 0 clock, 01 : 1 clocks, 10 : 2 clocks, 11 : 3 clocks
HAVG	R/W	Horizontal average enable. When 1, horizontal averaging of RGB outputs is enabled. When 0, horizontal averaging is disabled.

Table 8. Interface Control Register Bit Descriptions

2.2.7 ITMG: Interface Timing Control Register

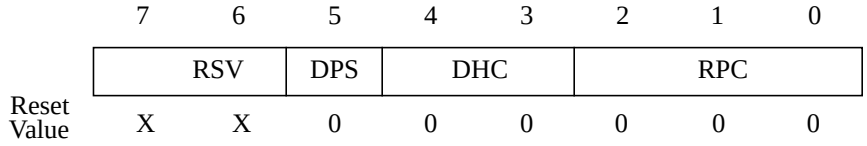


Figure 10. Interface Timing Register Format

Mnemonic	Read/Write Control	Description
RPC	R/W	Data Ready Pulse Count: The number of cycles that the DRDY signal is asserted for. **RPC** **Number of Clock Cycles DRDY Signal Asserted** 000 : 1 clock 001 : 2 clocks 010 : 3 clocks 011 : 4 clocks 100 : 5 clocks 101 : 6 clocks 110 : 7 clocks 111: 8 clocks
DHC	R/W	Data Hold cycle count after de-assertion of DRDY. 00 : 0 clock, 01 : 1 clocks, 10 : 2 clocks, 11 : 3 clocks
DPS	R/W	DRDY signal Polarity Select. When 0, DRDY is active high. When 1, DRDY is active low.
RSV	N/A	Reserved.

Table 9. Interface Timing Register Bit Descriptions

2.2.8 BFRAC: Baud Fraction Register

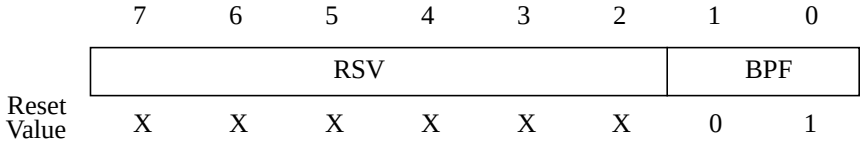


Figure 11. Baud Fraction Register Format

Mnemonic	Read/Write Control	Description
BPF	R/W	Baud Rate Fraction. Fractional portion of the baud period. **BPF** **BAUD Rate Fraction** 00 : Zero fractional portion. 01 : 1/4 10 : 1/2 11 : 3/4
RSV	N/A	Reserved

Table 10. Baud Fraction Register bit descriptions.

2.2.9 BRATE: Baud Rate Register

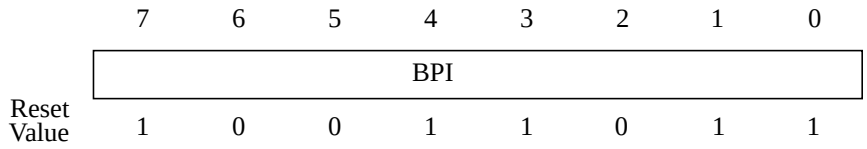


Figure 12. Baud Rate Register Format

Mnemonic	Read/Write Control	Description
BPI	R/W	Baud Rate Integer. Integer portion of baud rate. BAUD_PERIOD = 1 / (BAUD_RATE) BAUD_RATE = CLK_FREQ * [16 * (BPI + 1) + (4 * BPF)]
RSV	N/A	Reserved

Table 11. Baud Rate Register bit descriptions.

2.2.10 ADCCTRL: ADC Control Register

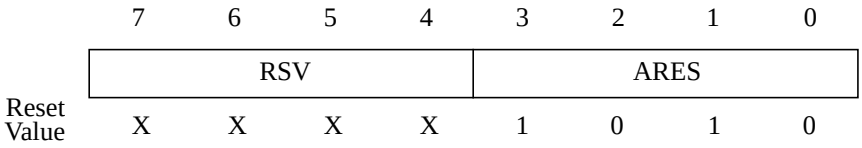


Figure 13. ADC Control Register Format

Mnemonic	Read/Write Control	Description
ARES	R/W	ADC Conversion Resolution. **ARES** 0000 : Reserved. 0001 - 1010 : Number corresponds to bits of ADC output resolution. 1011 - 1111 : Reserved. Note: Legal settings in normal operation are 1000 - 1010. The ADC resolution impacts the minimum allowable column timing. See “Column Timing Related Equations” on page 56 for more information.
RSV	N/A	Reserved

Table 12. ADC Control Register bit descriptions

2.2.11 FWROW: First Window Row Register

This register is used to define the row address of the first row of the image window. When using the full array for image capture, the value should be zero.

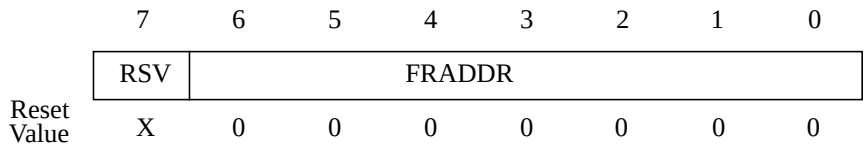


Figure 14. First Window Row Register

Mnemonic	Read/Write Control	Description
FRADDR[8:2]	R/W	First Row Address. Represents bits [8:2] of the address of first row of the image window. Bits [1:0] of the first row address are hard wired as “00” to force the window to begin on an even row boundary that is a multiple of four. The legal range is from zero to the last row address minus three. 0 <= FRADDR[8:0] <= LRADDR[8:0] - 3.
RSV	N/A	Reserved

Table 13. First Window Row Register Bit Descriptions

2.2.12 FWCOL: First Window Column Register

This register is used to define the address of the first column of the image window. When using the full array for image capture, the value should be zero.

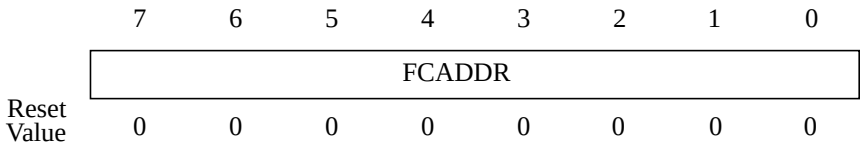


Figure 15. First Window Column Register Format

Mnemonic	Read/Write Control	Description
FCADDR	R/W	First Column Address. Represents bits [9:2] of the address of the first column of the image window. Bits [1:0] of the first column address are hard wired as “00” to force the window to begin on an even row boundary that is a multiple of four. The legal range of the first column address is from zero to the last column address minus the minimum number of columns in the image windows: 0 <= FCADDR[9:0] <= LCADDR[9:0] - MINC +1 where MINC represents the minimum number of columns in the image windows for the given operating mode and column timing. See “Column Timing Related Equations” on page 56 for the equation for MINC.

Table 14. First Window Column Register Bit Descriptions

2.2.13 LWROW: Last Window ROW Register

This register is used to define the address of the last row of the image window. When using the full array for image capture, the value should be the number of rows - 1.

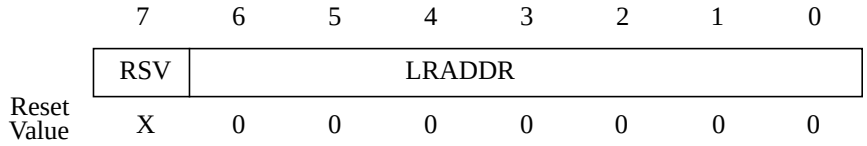


Figure 16. Last Window Row Register Format

Mnemonic	Read/Write Control	Description
LRADDR	R/W	Last Row Address. Represents bits [8:2] of the address of the last row of the image window. Bits [1:0] of the last row address are hard wired as “11” to force the window to end on an odd row boundary that is a multiple of four minus one. The legal range is from the address of the first row plus three to the number of rows minus one. FRADDR[8:0] + 3 <= LRADDR[8:0] <= number of rows in array - 1
RSV	N/A	Reserved

Table 15. Last Window Row Register Bit Descriptions

2.2.14 LWCOL: Last Window Column Register

This register is used to define the address of the last column of the image window. When using the full array for image capture, the value should be the number of columns - 1.

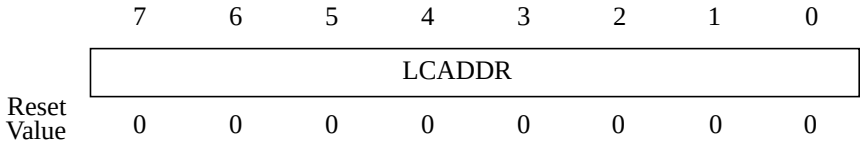


Figure 17. Last Window Column Register Format

Mnemonic	Read/Write Control	Description
LCADDR	R/W	Last Column Address. Represents bits [9:2] of the address of last column of the image window. Bits [1:0] of the last column address are hard wired as “11” to force the window to end on an odd column boundary that is a multiple of four minus one. The legal range of the last column address is from the the first column address plus the minimum number of columns, to the number of columns in the array minus one. FCADDR[9:0] + MINC - 1 <= LCADDR[9:0] <= number of columns in array - 1 where MINC represents the minimum number of columns in the image windows for the given operating mode and column timing. See “Column Timing Related Equations” for the equation for MINC.

Table 16. Last Window Column Register Bit Descriptions

2.2.15 TCTRL: Timing Control Register

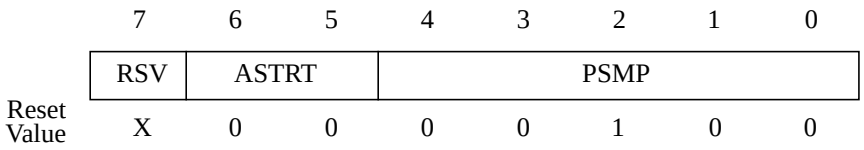


Figure 18. Timing Control Register Format

Mnemonic	Read/Write Control	Description
PSMP	R/W	PGA Sample duration. The number represents the number of clock cycles that the PGA sample signal is asserted. Valid numbers range from 4 to 31 where PSMP + CTO + 1 >= ARES. See “Column Timing Related Equations” on page 56 for more information.
ASTRT	R/W	ADC Start Signal Duration. **ASTRT** — **adcStart Signal Duration** — **ADC Sample Duration** 00 : 2 clock cycles 1 clock cycle 01 : 3 clock cycles 2 clock cycles 10 : 4 clock cycles 3 clock cycles 11 : 5 clock cycles 4 clock cycles
RSV	N/A	Reserved

Table 17. Timing Control Register bit descriptions

2.2.16 ERECPGA: Even Row, Even Column PGA Gain Register

This register is used to set the PGA gain for pixels on even rows and even columns.

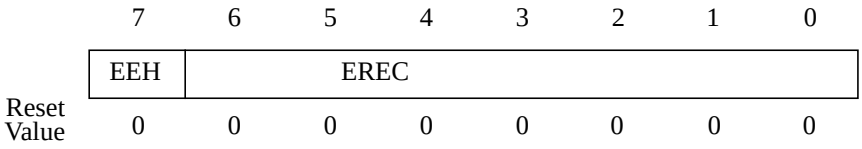


Figure 19. Even Row, Even Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
EREC	R/W	PGA gain for pixels on Even Rows and Even Columns. Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(EEH+1) where n=binary to decimal conversion of EREC
EEH	R/W	PGA Even row Even column High gain enable. When 1, the PGA gain value programmed in the EREC bit field is doubled. When 0, PGA gain value programmed in EREC bit field is used.

Table 18. Even Row, Even Column PGA Gain Register Bit Description

2.2.17 EROCPGA: Even Row, Odd Column PGA Gain Register

This register is used to set the PGA gain for pixels on even rows and odd columns.

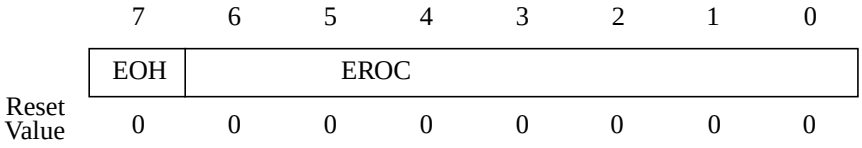


Figure 20. Even Row, Odd Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
EROC	R/W	PGA gain for pixels on Even Rows and Odd Columns: Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(EOH+1) where n=decimal conversion of EROC
EOH	R/W	PGA Even row Odd column High gain enable: When 1, PGA gain value programmed in EROC bit field is doubled. When 0, PGA gain value programmed in EROC bit field is used.

Table 19. Even Row, Odd Column PGA Gain Register Bit Description

2.2.18 ORECPGA: Odd Row, Even Column PGA Gain Register

This register is used to set the PGA gain for pixels on odd rows and even columns.

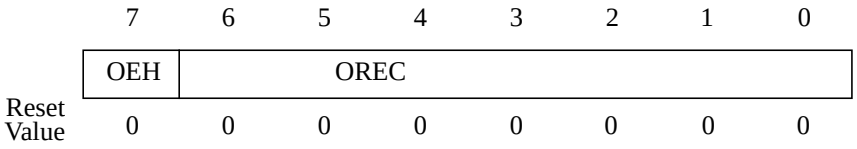


Figure 21. Odd Row, Even Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
OREC	R/W	PGA gain for pixels on Odd Rows and Even Columns: Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(OEH+1) where n=decimal conversion of OREC
OEH	R/W	PGA Odd row Even column High gain enable: When 1, the PGA gain value programmed in the OREC bit field is doubled. When 0, PGA gain value programmed in OREC bit field is used.

Table 20. Odd Row, Even Column PGA Gain Register Bit Description

2.2.19 OROCPGA: Odd Row, Odd Column PGA Gain Register

This register is used to set the PGA gain for pixels on odd rows and oddcolumns.

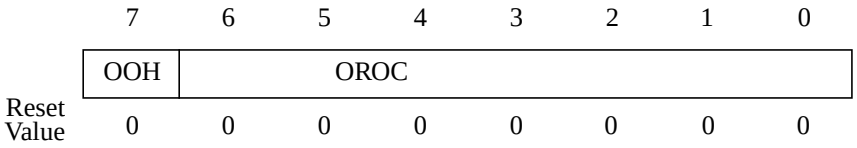


Figure 22. Odd Row, Odd Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
OROC	R/W	PGA gain for pixels on Odd Rows and Odd Columns: Legal values from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(OOH+1) where n=decimal conversion of OROC
OOH	R/W	PGA Odd row Odd column High gain enable: When 1, PGA gain value programmed in OROC bit field is doubled. When 0, PGA gain value programmed in OROC bit field is used.

Table 21. Odd Row, Odd Column PGA Gain Register Bit Description

2.2.20 ROWEXPL: Row Exposure Low Register

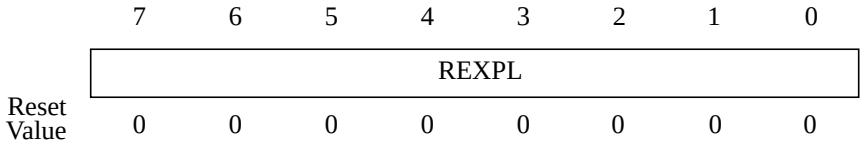


Figure 23. Row Exposure Low Register Format

Mnemonic	Read/Write Control	Description
REXPL	R/W	Row Exposure Low Register. Least significent bits of the row exposure register (REXP[7:0]) formed by the concatenation of the ROWEXPH[6:0] and ROWEXPL[7:0] registers (i.e., REXP[14:0] = {ROWEXPH[6:0], ROWEXPL[7:0]}). In the “Normal” mode and the “Shutter” mode, the row exposure register defines the number of row processing periods (see “Diagram of the Row Processing Period”) that the image is exposed for. This register has no effect when operating in the “Accumulation” mode. The legal range of values for the row exposure register is: 0 <= ROWEXP[15:0] <= 32,767. For more information, refer to the “Exposure Control”, Section 3.4.5 on page 58.
RSV	N/A	Reserved

Table 22. Row Exposure Low Register Bit Descriptions

2.2.21 ROWEXPH: Row Exposure High Register

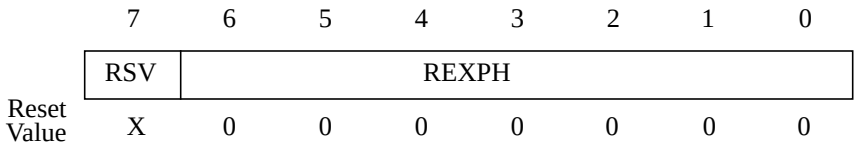


Figure 24. Row Exposure High Register Format

Mnemonic	Read/Write Control	Description
REXPH	R/W	Row Exposure High Register. Most significent bits of the row exposure register (ROWEXP[14:8]) formed by the concatenation of the ROWEXPH[6:0] and ROWEXPL[7:0] registers (i.e., REXP[14:0] = {ROWEXPH[6:0], ROWEXPL[7:0]}). In the “Normal” mode and the “Shutter” mode, the row exposure register defines the number of row processing periods (see “Diagram of the Row Processing Period” on page 51) that the image is exposed for. This register has no effect when operating in the “Accumulation” mode. The legal range of values for the row exposure register is: 0 <= ROWEXP[15:0] <= 32,767. For more information, refer to the “Exposure Control”, Section 3.4.5 on page 58.
RSV	N/A	Reserved

Table 23. Row Exposure High Register Bit Descriptions

2.2.22 SROWEXPL: Sub-Row Exposure Low Register

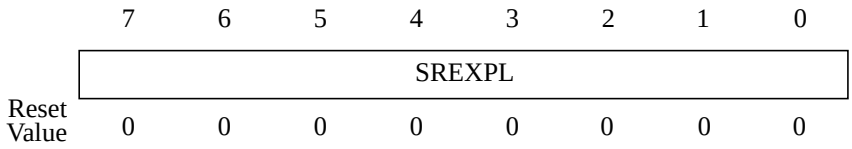


Figure 25. Sub-row Exposure Low Register Format

Mnemonic	Read/Write Control	Description
SREXPL	R/W	Sub-row exposure low register. Least significent bits of the sub-row exposure register (SROWEXP[7:0]) formed by the concatenation of the SROWEXPH and SROWEXPL registers (i.e., SROWEXP[14:0] = {SROWEXPH[6:0], SROWEXPL[7:0]}). This register has no effect when operating in the “Accumulation” and the “Shutter” modes and applies only to the “Normal” mode of operation (see “Major Image Capture Modes” on page 42). This register is used to specify the sub-row duration of time that each pixel is exposed before being sampled. The unit of measurement is one clock cycle. The legal range of values is: 0 <= SROWEXP[15:0] <= CP - (MNCT * CT) - 1 For more information, see “Exposure Control”, Section 3.4.5 on page 58, and “Timing Equations” on page 54.

Table 24. Sub-row Exposure Low Register Format

2.2.23 SROWEXPH: Sub-Row Exposure High Register

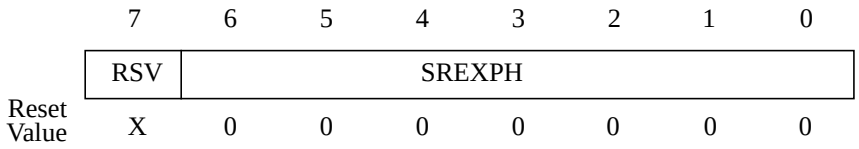


Figure 26. Sub-row Exposure High Register Format

Mnemonic	Read/Write Control	Description
SREXPH	R/W	Sub-Row Exposure High Register. Most significent bits of the Sub-row Exposure Register (SROWEXP[14:8]) formed by the concatenation of the SROWEXPH and SROWEXPL registers. This register has no effect when operating in the “Accumulation” and the “Shutter” modes and applies only to the “Normal” mode of operation (see “Major Image Capture Modes”). This register is used to specify the sub-row duration of time that each pixel is exposed before being sampled. The unit of measurement is one clock cycle. The legal range of values is: 0 <= SROWEXP[15:0] <= CP - (MNCT * CT) - 1 For more information, see the “Exposure Control”, and “Timing Equations” sections.
RSV	N/A	Reserved

Table 25. Sub-row Exposure High Register Format

2.2.24 CONFIG: Configuration Register

The configuration register is used to select the method of image capture to be used.

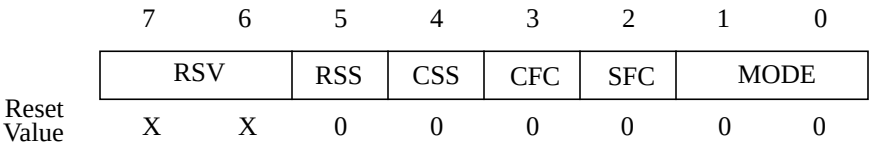


Figure 27. Configuration Register Format

Mnemonic	Read/Write Control	Description
MODE	R/W	Operating mode select. **MODE** 00: Normal operation mode. 01: Shutter mode. 10: Accumulation mode. 11: Reserved.
SFC	R/W	Stop when Frame Complete. When 1, the internal timing controller will complete processing the current frame before stopping following de-assertion of the RUN control bit. When 0, the internal timing controller will stop execution immediately upon de-assertion of the RUN control bit. Data currently in the image pipe will be output.
CFC	R/W	Continuous Frame Capture: 1 forces continuous multiple frame capture when RUN flag asserted. 0 forces single frame image capture when RUN flag asserted.
CSS	R/W	Column Sub-Sample enable. When 1, one half of the columns in the image window are processed. When 0, all columns in the image window are processed.
RSS	R/W	Row Sub-Sample enable. When 1, one half of the rows in the image window are processed. When 0, all rows in the image window are processed.
RSV	N/A	Reserved

Table 26. Configuration Register Bit Descriptions

2.2.25 CONTROL: Control Register

The configuration register is used to initiate and monitor an image capture process, and control the reset and power up state of the chip.

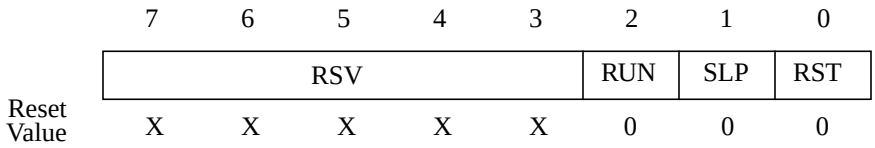


Figure 28. Control Register Format

Mnemonic	Read/Write Control	Description
RST	R/W	Hardware Reset. When 1, an internal hardware reset is asserted. When 0, does not assert an internal hardware reset.
SLP	R/W	Sleep mode enable. When 1, internal sleep mode is asserted, the internal timing controller clocks and state machines are disabled, and power to the analog sections blocks is disabled. When 0, internal sleep mode is not asserted.
RUN	R/W	Run enable. Transition from 0 to 1 initiates the configured image capture process which may be single or multiple frames depending on the state of the CFC control bit. Normal termination of a single frame image capture process automatically drives RUN to a 0. When 1, writing a 0 to RUN posts a request to the internal timing controller to stop the current image capture process. Depending on the state of the SFC bit, the stop request will be executed immediately or at the next frame boundary.
RSV	N/A	Reserved

Table 27. Control Register Bit Descriptions

3. Programming Reference

3.1 Programming Reference Overview

The HDCS sensor supports a wide variety of operating modes, window sizes and locations, exposure control settings, timing control settings, analog to digital conversion settings, and data output format settings. Operation of the system is primarily controlled by a set of internal registers that must be initialized to the desired settings prior to use. All register reads and writes occur via one of two user selectable serial communication interfaces, both of which support multiple user configurable data rates and operating modes. When an image capture process is running, image data is output from the HDCS Sensor via the parallel interface. Depending on the programmed operating mode and exposure settings, data may be output in bursts or a steady stream.

3.2 Windowing and Panning

The HDCS sensor supports a very flexible windowing and panning scheme in that numerous windows sizes, aspect ratios, and positions are supported. The image window can be placed virtually anywhere within the boundaries of the array.

The primary restriction on the image window size is that all windows are forced to be a multiple of four rows and four columns, regardless of the mode. When operating in the “Normal Mode”, there is a further restriction on the minimum window size to ensure that the column processing portion of the row processing time is of sufficient duration to perform the required exposure reset (see “Diagram of the Row Processing Period” on page 51 and “Sub-row Exposure Control” on page 60). The only restriction on the window location is that the first row and first column are aligned to a number that is a multiple of four. Likewise, the last row and last column to are aligned to an odd number that is one less than a multiple of four.

3.3 Programmable Gain Settings

The material used to create color filter patterns such as the RGB Bayer pattern combined with the frequency response of the photo diodes combine to produce different degrees of sensitivity to red, green, and blue light. The HDCS sensor allows the host system to compensate for these differences, if necessary, by allowing four different gain settings independantly programmed via the four PGA gain registers . The gain values are applied as even row even column, even row odd column, odd row even column, and odd row odd column. Since the programmable gain settings modify the resulting signal levels driving the on-chip ADC/S, the gain settings should be factored into the exposure control algorithm.

The voltage gain settings are given by:

Gain = [1 + (19 * n / 127)] * [m + 1]

where “n” is the number defined by the the seven least significent bits of the corresponding gain register (i.e., n = ERECPGA[6:0], EROCPGA[6:0], ORECPGA[6:0], or OROCPGA[6:0]) and “m” is the most significent bit of the same register (i.e., i.e., M= ERECPGA[7], EROCPGA[7], ORECPGA[7], or OROCPGA[7]).

For gain settings lower than 20 (decimal), the best results will be obtained by setting “m” equal to zero. Also, for PGA gain settings higher than 10, it is recommended that the “PSMP” and “ASTRT” portions of the column timing period be increased over the minimum values (see “Column Timing Period” on page 53, and “TCTRL: Timing Control Register” on page 30).

3.4 Internal Timing Controller Operation

Once initiated, the internal timing controller generates all of the control signals and executes all of the sequences required to capture one or more frames of image data with minimal host system intervention. To initiate an image capture process, the host controller must first configure the register set and then assert the “RUN” bit of the “CONTROL” register. If the system is configured to capture a single frame, the timing controller will execute a finite sequence of operations and stop execution after outputting a single frame of data. If the system is configured to capture multiple frames, the timing controller will continue to sequence and output data until forced to stop by the host system. The host system can stop the HDCS sensorby deasserting the “RUN” bit of the “CONTROL” register, asserting an internal or external reset, or asserting an internal or external low power mode condition.

The HDCS sensor supports multiple image capture modes classified as either a major or minor mode. Major modes define the general operation of an image capture process and are mutually exclusive in that only one mode can be applied at a time. Minor modes further refine the behavior of the major mode, can be applied to every major mode, affect the major mode operation in a similar manner, and are not mutually exclusive.

3.4.1 Major Image Capture Modes

The major operating mode is selected by programming the “MODE” field of the “CONFIG” register. The three major image capture modes include the “Normal Mode”, the “Shutter Mode”, and the “Accumulation Mode”.

All image capture processes are initiated by the host system first configuring the register set (image window size and location, operating modes, exposure duration, gain settings, etc.) and then asserting the “RUN” bit of the “CONTROL” register. Internal circuitry generates all of the control signals necessary to address, sample, convert, and output one or more frames of image data with minimal host system interaction.

3.4.1.1 Normal Image Capture Mode

The “Normal” image capture mode is the default mode and is intended to be used for capturing high quality still or video images. The exposure duration is internally controlled by implementing a rolling electronic shutter that does not require use of an external mechanical shutter or external flash. Following assertion of the “RUN” bit, the internal timing controller begins sequentially resetting rows in the selected image window to individually start the integration period of each row. To ensure that the integration period of all rows are equivalent, the rows are reset at a rate equal to the rate at which they will subsequently be sampled. All row operations occur in ascending order and wrap back to the first row in the image window after operating on the last row. When the first row in the image window has been exposed for the programmed duration, the system samples, converts, and outputs data for each row in ascending order. If the system is configured to capture one frame, this process automatically terminates upon completion of the first frame. If it is configured to capture multiple frames, the process continues terminated by host interaction.

If the exposure duration is greater than the time required to process one frame and multiple frames are captured, a delay equal to the row exposure count minus the number of rows will be inserted between each frame. As such, the image data will be output in single frame bursts with a delay between each burst. If enabled and configured as the shutter sync signal, the nFRAME_nSYNC signal will be asserted at the start of the inter-frame delay to facilitate operation of an external shutter or flash. If the exposure duration is not greater than the time required to process one frame, data will be output in a steady stream with no inter-frame delay, and the shutter sync signal will not be asserted.

The sample reset occurs during the row sample portion of the row processing time and occurs immediately after the row is sampled (i.e., the end of the integration time for that row). Similarly, the exposure reset essentially marks the start of the integration time for the row that is reset. During a Normal mode image capture process, the exposure reset of each row must occur during the column processing portion of the row processing time. As such, the duration of the required reset pulse defines the minimum duration of the column processing time. The column processing time is a function of the number of columns in the image window, the programmed column timing, and the column sub-sampling mode

The following diagram depicts the sequence of operations for a Normal mode image capture process with an exposure duration greater than the time required to process one frame such that an inter-frame delay is created. The diagram columns “Exposure Reset Row” and “Sample Reset Row” are referring to the row number that is being reset to start the exposure, and the row number that is being sampled. In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively, and the row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumptions that n = 0, m = 7, and R = 2.

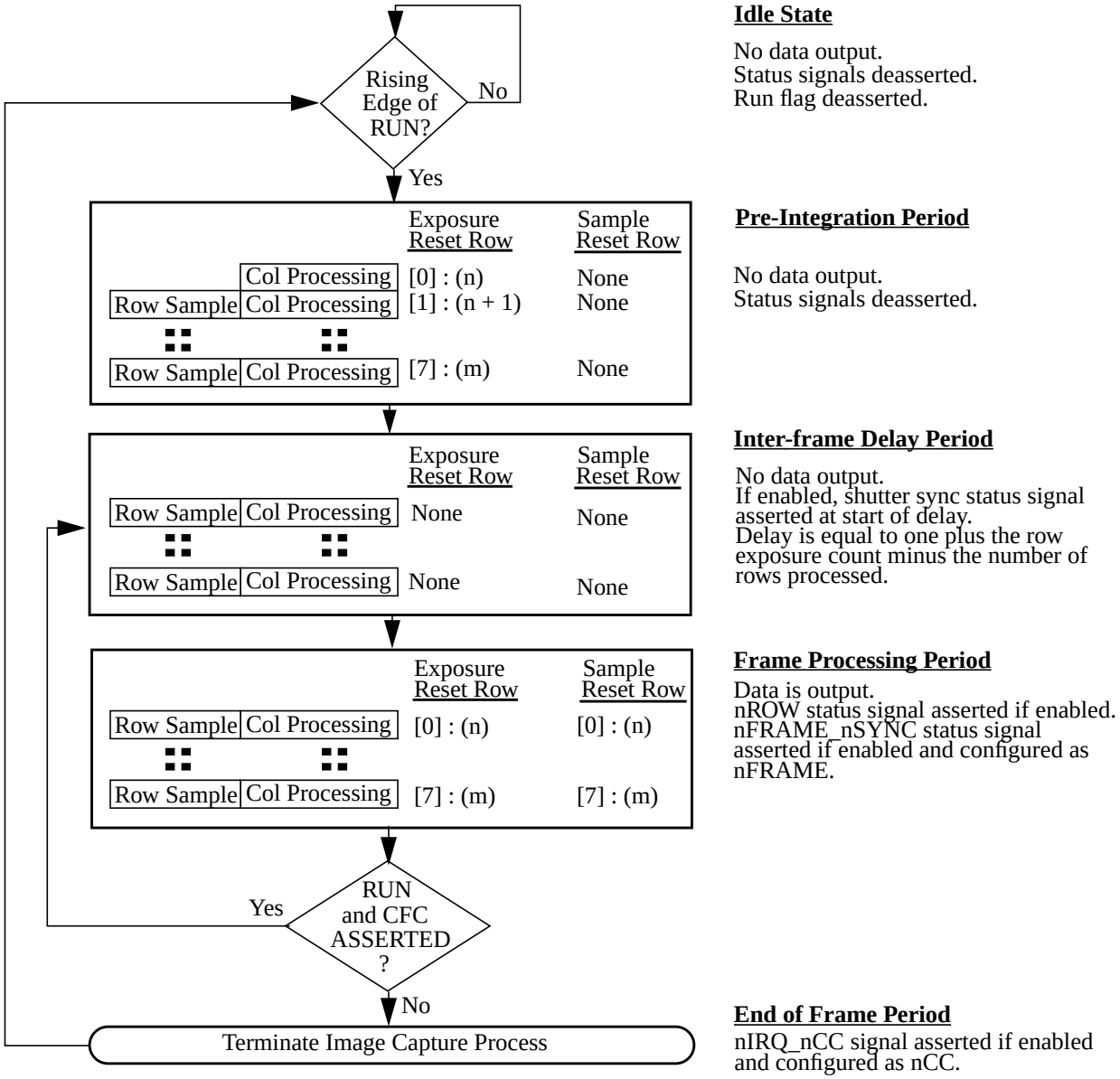


Figure 29. Normal Mode Image Capture Process with an Inter-frame Delay

The following diagram depicts the sequence of operations for a Normal mode image capture process with an exposure duration less than the time required to process one frame such that there is no inter-frame delay. The diagram columns “Exposure Reset Row” and “Sample Reset Row” are referring to the row number that is being reset to start the exposure, and the row number that is being sampled. In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively, and the row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumption that n = 0, m = 7, and R = 2.

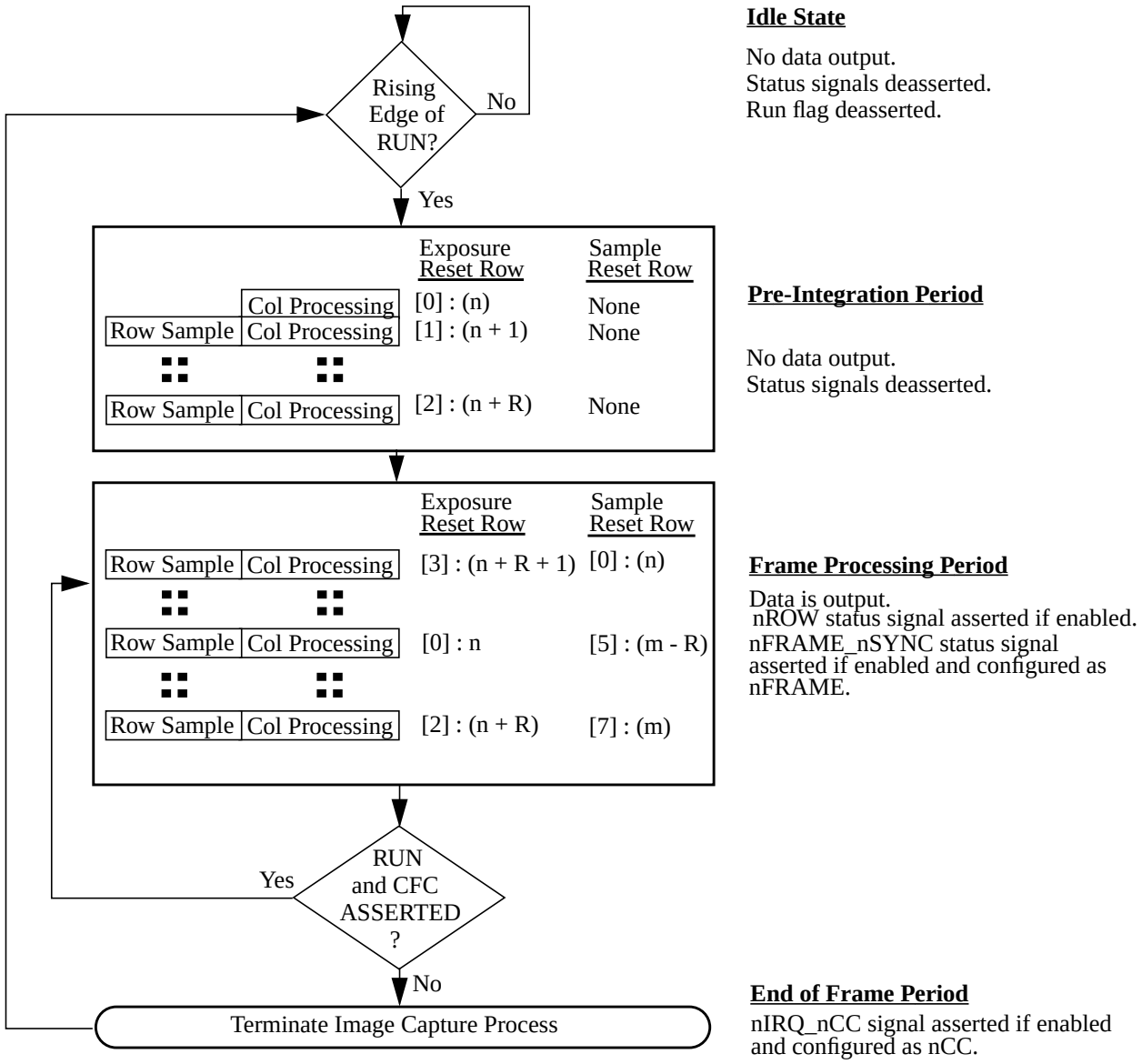


Figure 30. Normal Mode Image Capture Process with no Inter-frame Delay

3.4.1.2 Shutter Mode Image Capture Process

The “Shutter Mode” image capture mode is intended to be used for capturing high quality still or video images in conjunction with an external shutter or flash. The basic sequence of operations is to execute a “fast rolling reset” on all rows in the image window, assert the shutter sync signal, delay a time duration programmed via the row exposure control registers (ROWEXPH and ROWEXPL), then sample, convert, and output the frame of data.

The objective of using the “fast rolling reset” is to minimize the pre-integration period and hence the latency between initiating the image capture process and when the shutter or flash can be opened. Due to the difference in duration of the row processing time and the time required to simply reset one row, the duration of time that each row is allowed to integrate is not equal. Rather, it increases from row to row in ascending order. As such, the dark current contribution is greater for the last row in the image window than the first. Obtaining high quality results in this mode requires that the dark current contribution be negligible relative to the light intensity when the shutter is opened or the flash is strobed. Also, if using a flash without a shutter, the ambient light level contribution must be negligible relative to the flash intensity.

Since the fast rolling reset is used to start integration of each row in this mode, there is no requirement to execute an exposure reset during the column processing time. As such, the minimum window size in this mode is reduced to the minimum window addressable via the register set.

In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively, and the row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumption that n = 0, m = 7, and R = 2.

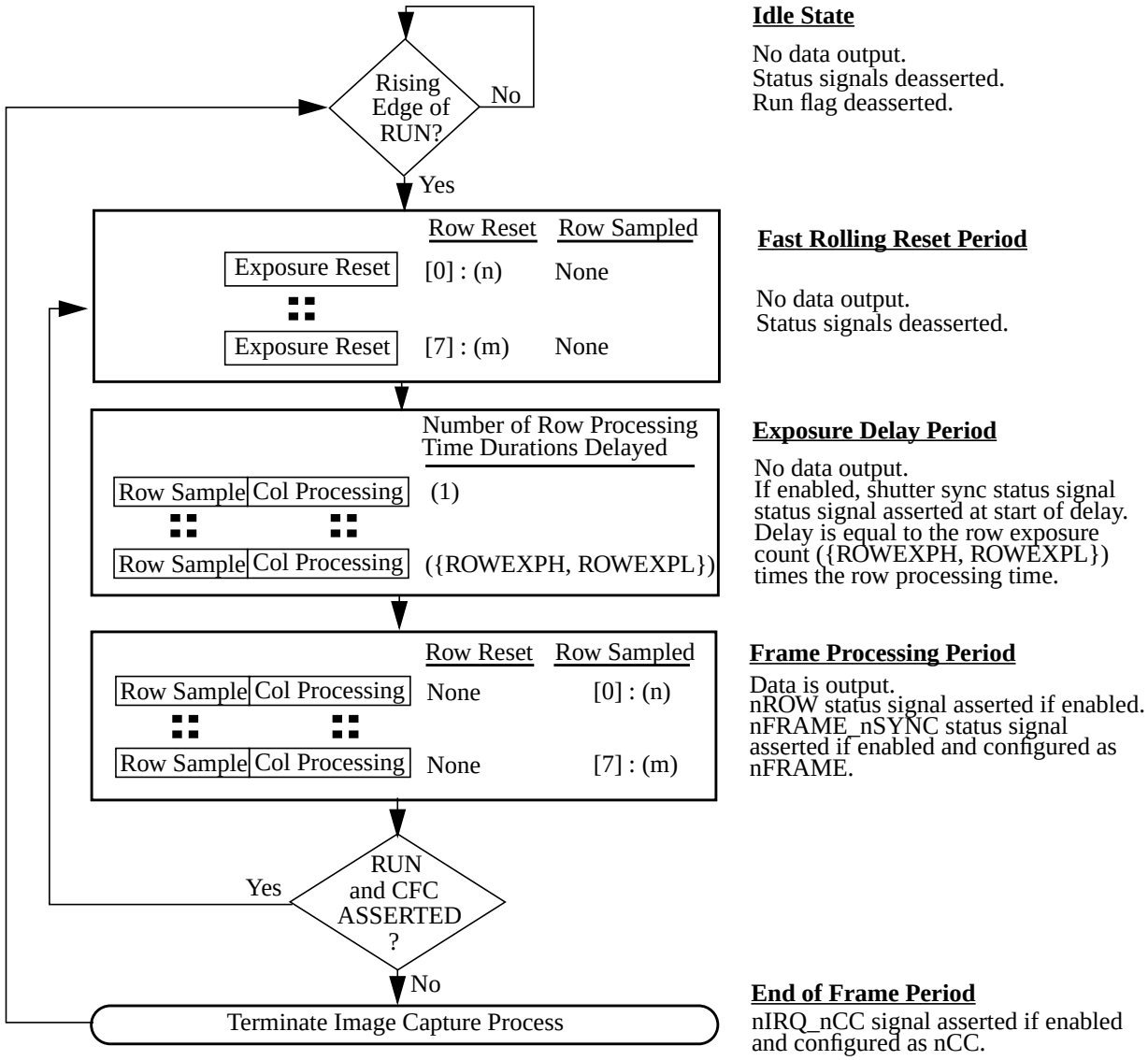


Figure 31. Graphical Depiction of the Shutter Mode Image Capture Process

3.4.1.3 Accumulation Mode Image Capture Process

The “Accumulation Mode” image capture process is designed to facilitate exposure control by providing a mechanism to determine the time required for one or more pixels in the image window to become saturated. In this mode, assertion of the “RUN” bit of the “CONTROL” register causes each pixel in the array to be reset simultaneously and then allowed to integrate. After the global reset, rows in the image windows are continuously double sampled and data is output. None of the pixels within the usable portion of the image array are reset after the initial global reset. As such, the pixels can be sampled multiple times while they continue to integrate. The time required for a user defined percentage of the pixels to become saturated can be used to determine the required exposure duration for the current light level.

Since the doubling sampling that occurs during the row sample time period uses pixel reset levels derived from a reference row, the resulting image quality may not be as high as can be achieved in the Normal or Shutter modes of operation.

In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively, and the row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumption that n = 0, m = 7, and R = 2.

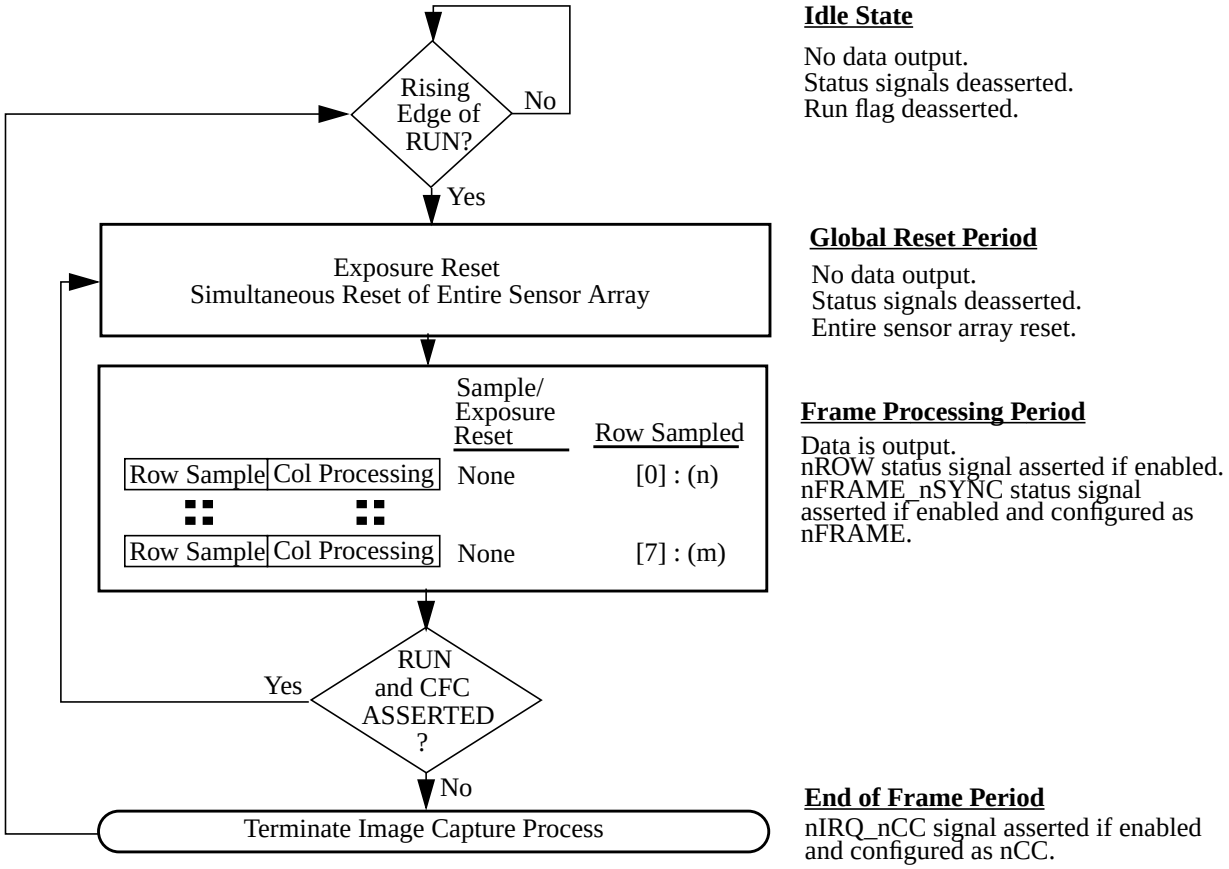


Figure 32. Graphical Depiction of the Accumulation Mode Image Capture Process

3.4.2 Minor Image Capture Modes

Every minor operating modes can be applied to every major operating mode and have a similar affect on every major mode. Every each minor mode can be enabled or disabled regardless of the state of other minor modes. Supported minor modes include row sub-sampling, column sub-sampling, single frame versus video mode, and single channel mode. With the exception of single channel mode, the state of each minor mode is controlled by fields in the CONFIG" register.

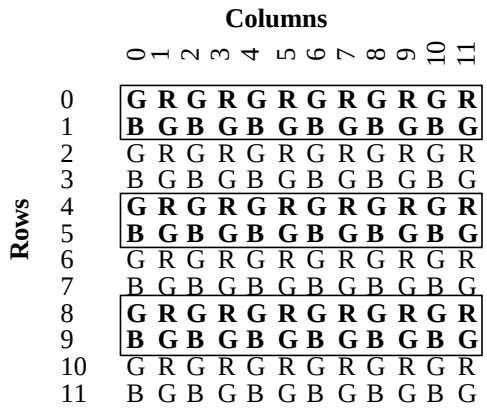
3.4.2.1 Single Frame Versus Video Mode

The state of the "CFC" field of the "CONFIG" register determines whether the system operates in single frame or video mode. Initiation of an image capture process when in single frame mode causes one frame of data to be output, after which the timing controller automatically terminates the image capture process. When in the video mode, the initiated image capture process will continue indefinitely until the host system intervenes by deasserting the "RUN" bit in the "CONTROL" register, asserting a sleep condition, or asserting a reset condition.

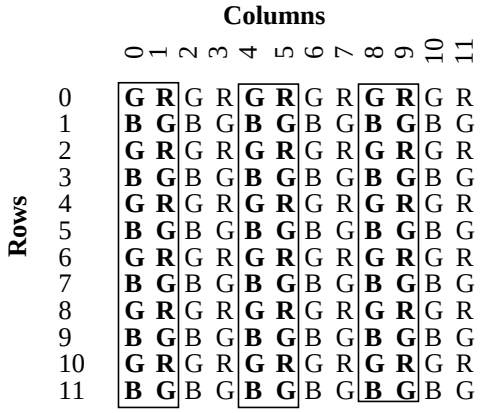
3.4.2.2 Row and Column Sub-Sampling Modes

The row and column sub-sampling modes can be used to implement a zoom feature and are controlled by the “RSS” and “CSS” fields of the “CONFIG” register respectively (“CONFIG: Configuration Register” on page 37).

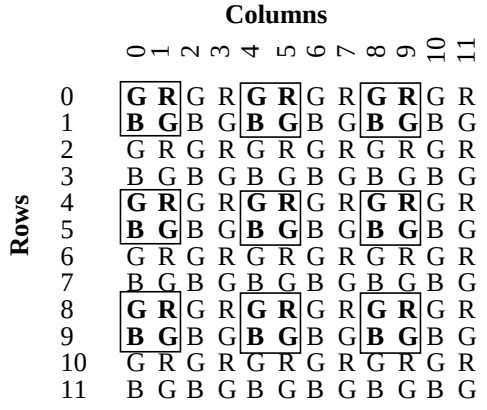
When both the row and column sub-sampling modes are disabled, every pixel within the defined image window is sampled during an image capture process. Enabling sub-sampling reduces the number of pixels sampled per frame by a factor of either two or four depending on whether just one or both modes are enabled. However, the impact on the actual frame rate and data rate depends on the major operating mode, the exposure register settings, the size of the image window, and the selected column timing.



Row Sub-sampling Pattern



Column Sub-sampling Pattern



Combined Row and Column Sub-sampling Pattern

Notes:

1) Sampled pixels shown in bold type within rectangles.
2) Assuming image window coordinates are (0,0) to (11,11).

Figure 33. Sub-sampling Patterns

3.4.3 Basic Timing Controller Operations

The internal operation of the timing controller and hence the rate and timing of data output is deterministic and can be calculated using an understanding of the operating mode in effect and the basic sequences of operations it executes, an understanding of the timing of those basic sequences, and pertinent register settings. The basic sequence of operations executed in each major mode is described in the section “Major Image Capture Modes” on page 42. The objective of this section is to describe the timing of the basic sequences and the registers that affect them.

3.4.3.1 Row Processing Period

The period of time required to process one row is a fundamental piece of information required to correctly program the exposure duration and to understand the rate and timing at which data is output from the chip. Rows are processed sequentially in ascending order and the data output rate and overall timing controller sequencing corresponds to the rate at which individual rows are processed. The rate at which rows are processed is highly programmable and depends on the image window size, whether column sub-sampling is enabled, and the selected timing control parameters.

As shown below, row processing is comprised of two major portions called the “Row Sample Period” and the “Column Processing Period”. When operating in the “Normal Mode” (refer to “Major Image Capture Modes” on page 42), an “Exposure Reset Period” occurs during the same time slot as the “Column Processing Period”. The sub-row exposure registers ({SROWEXPH, SROWEXPL}) define the time delay from the start of the column processing period to the start of the exposure reset period and hence the sub-row component of the overall integration time.

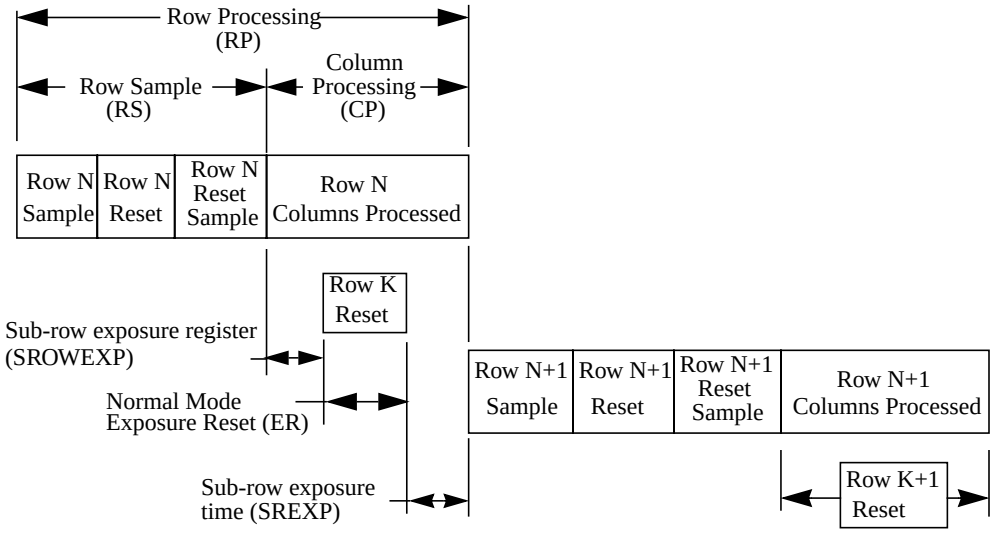


Figure 34. Diagram of the Row Processing Period

3.4.3.2 Row Sample Period

The row sample period is a constant duration regardless of the selected operating mode, image window size, and the programmed column timing. If current row has been fully exposed, it is sampled, reset, and sampled again to implement the double sampling feature. The reset that occurs in this time slot is referred to as the “sample reset”. If current row has not been fully exposed, the system does not actually sample or reset any rows, but simply delays an amount of time equivalent to what it would take to sample, reset, and sample again. Refer to “Row Timing Related Equations” on page 55 to determine the duration of the row sample period.

3.4.3.3 Column Processing Period

The analog to digital conversion of a row of sampled pixel data occurs during the column processing period. Data is also output from the chip during this period. The duration of time required to perform the column processing period of the row processing is highly programmable and depends on the number of columns in the image window, whether column sub-sampling is enabled, whether the single channel mode is enabled, and the selected column timing.

The column processing period begins with a constant duration overhead period following by some number of programmable duration column timing periods. The number of column timing periods ranges between two and the number of columns in the array and is user programmable based on the image window size and the operating mode. If the single channel mode is enabled, one column is processed at a time, otherwise pairs of columns are processed in parallel. Regardless of the selected operating mode, columns are always processed and the data is always output in ascending order.

Refer to “Column Timing Related Equations” on page 56 for information on how to calculate the duration of the column processing period.

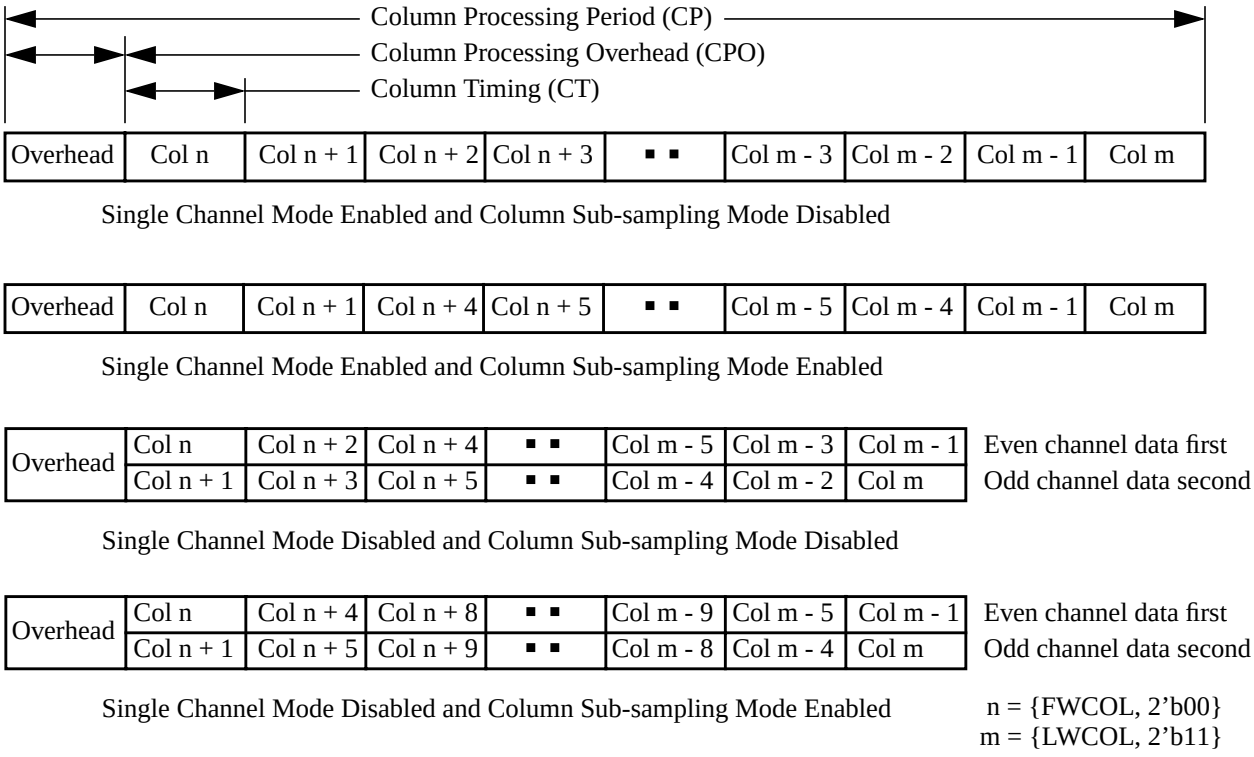


Figure 35. Column Processing Sequencing For Applicable Operating Modes

3.4.3.4 Column Timing Period

The column timing period is a basic unit of the column processing time and is comprised of a fixed duration overhead period and two independently programmable periods that can be used to vary the duration of each data conversion and output process. For any operating mode and image window size, increasing the column timing from the minimum will increase the row processing time, decrease the average data output rate, and decrease the frame rate. As such, the column timing can be used to scale the frame and data rates to match artificial lighting frequencies and host system bandwidth requirements.

The PGA Sample signal and ADC Start signal durations are programmed via the “PSMP” and “ASTRT” fields of the timing control register (“TCTRL”, see page 30). Note that the column timing period must be a minimum of 11 cycles when performing 10-bit A/D conversions.

Refer to “Column Timing Related Equations” on page 56, “TCTRL: Timing Control Register” on page 30 for more information on calculating the duration of the column timing period.

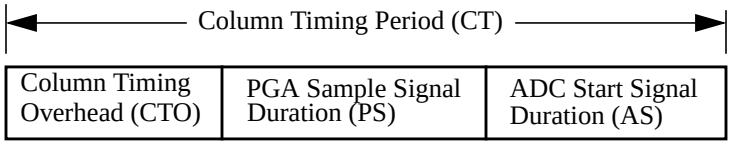


Figure 36. Column Timing Period

3.4.3.5 Frame Processing Period

The frame processing period is the period of time during which one frame of fully exposed data is sampled and output. The frame processing period is highly programmable and depends on the size of the image window, the selected timing parameters, and whether row sub-sampling is enabled. For more information, refer to “Major Image Capture Modes” on page 42, and “Operating Mode Timing Related Equations” on page 55.

3.4.3.6 Pre-Integration Period

The pre-integration period occurs only when operating in the “Normal Mode” and occurs only once prior to capturing the first frame of data. The absolute time duration is highly programmable and depends primarily on the row processing time and the row exposure register settings. For more information, refer to “Operating Mode Timing Related Equations” on page 55, and “Normal Image Capture Mode” on page 42.

3.4.3.7 Inter-frame Delay Period

The inter-frame delay period occurs only when operating in the “Normal Mode” and the row exposure count is greater than the number of rows processed in the image window. There is no data output during this time period and no rows are being sampled or reset. The inter-frame delay period will be executed multiple times when operating in video mode.

The host system can override the internal rolling electronic shutter by opening an external shutter or asserting a flash during this time slot. To facilitate timing the opening of a shutter or assertion of a flash, a synchronization signal can be configured to be asserted at the beginning of the exposure delay period. This is accomplished by enabling the

nFRAME_nSYNC output signal and configuring it for the nSYNC mode. For more information, refer to “Operating Mode Timing Related Equations” on page 55, and “Normal Image Capture Mode” on page 42.

3.4.3.8 Fast Rolling Reset Period

The fast rolling reset period occurs only in the “Shutter Mode”. The duration of the fast rolling reset period is determined by the exposure reset duration, a fixed overhead per exposure reset, and the number of rows in the image window that will be processed. During this period each row in the image window that will be processed is reset, starting with the first and continuing in ascending order. For more information, refer to “Shutter Mode Image Capture Process” on page 46, and “Operating Mode Timing Related Equations” on page 55.

3.4.3.9 Exposure Delay Period

The exposure delay period occurs only in the “Shutter Mode” (Figure 31 on page 47) and the duration is determined by the row processing time and the row exposure register settings. To ensure that the shutter or flash do not conflict with the internal electronic shutter, the exposure delay should be configured to be the minimum setting that is greater than the time shutter will be opened or the flash asserted. To facilitate timing the opening of a shutter or assertion of a flash, a synchronization signal can be configured to be asserted at the beginning of the exposure delay period. This is accomplished by enabling the nFRAME_nSYNC output signal and configuring it for the nSYNC mode. For more information, refer to “Shutter Mode Image Capture Process” on page 46, and “Operating Mode Timing Related Equations” on page 55.

3.4.3.10 Global Reset Period

The global reset period only occurs in the “Accumulation Mode” and the duration is determined by the exposure reset duration plus a constant number of overhead cycles. Form more information, refer to “Operating Mode Timing Related Equations” on page 55, and “Accumulation Mode Image Capture Process” on page 48.

3.4.4 Timing Equations

Symbol	Equation	Units	Description
T		Time	System clock period.
TSO	TSO = 1	Cycles	Timing controller start overhead. Delay from internal assertion of the RUN bit of the CONTROL register to when the timing controller starts operating.
ER	ER = 100	Cycles	Exposure reset duration.

Table 28. General Timing Controller Equations

Symbol	Equation	Units	Description
PI	PI = CP + (REXP * RP) if REXP <= NRP PI = CP + (NRP * RP) if REXP > NRP	Cycles	The pre-integration time occurs only in the “Normal” mode and depends on the row exposure settings and the row processing time.
IFD	IFD = 0 if REXP < NRP IFD = (REXP - NRP) + 1 if REXP >= NRP	Cycles	The inter-frame delay time occurs only in the “Normal” mode if the row exposure count exceeds the number of rows processed minus one.
FP	FP = NRP * RP	Cycles	The frame processing time is defined by the number of rows processed and the row processing time.
FRR	FRR = NRP * (ER + 4)	Cycles	The fast rolling reset period occurs only in the “Shutter” mode and is equal to the number of rows processed times the exposure reset duration plus a constant.
ED	ED = REXP * RP	Cycles	The exposure delay occurs only in the “Shutter” mode and is equal to the row exposure count processed times the row processing time.
GR	GR = ER + 3	Cycles	The global reset delay occurs only in the “Accumulation” mode and is equal to the exposure reset duration plus a constant.
SDO	Normal Mode: SDO = TSO + PI + IFD + RS Accumulation Mode: SDO = TSO + GR + RS Shutter Mode: SDO = TSO + FRR + ED + RS	Cycles	The delay from the start of an image capture process to the first data output depends on the operating mode and row exposure settings.

Table 29. Operating Mode Timing Related Equations

Symbol	Equation	Units	Description
RS	RS = 186	Cycles	The row sample period is constant.
RP	RP = RS + CP	Cycles	The row processing period is determined by the sum of the row sample and column processing periods.
RSSF	RSSF = 1 if RSS = “0” RSSF = 2 if RSS is “1”	Cycles	The row sub-sample scale factor is determined by the state of the row sub-sample enable (see the RSS field of CONFIG register).
NRP	NRP = [last row address - first row address + 1] / RSSF	Cycles	The Number of Rows Processed is determined by the vertical sizeof the image window and the state of the row sub-sample enable.

Table 30. Row Timing Related Equations

Symbol	Equation (units of clock cycles)	Units	Description
CTO	CTO = 4	Cycles	Column timing overhead.
PS	4 <= PS <= 31	Cycles	PGA sample signal duration defined by PSMP field of TCTRL reg. The PGA sample signal duration m
AS	2 <= AS <= 5	Cycles	ADC start signal duration defined by the ASTRT field of TCTRL reg.
CT	CT = CTO + PS + AS PS + CTO + 1 >= ARES	Cycles	The column timing period equals column timing overhead plus the PGA sample and ADC start signal durations. **Note:** The column timing period must be sufficient to allow for the ADC conversion time which depends on the operating mode.
CPO	CPO = 2	Cycles	The column processing overhead.
SCSF	SCSF = 1 if CHSEL = “1x” SCSF = 2 if CHSEL is “0x”	Cycles	The single channel scale factor is determined solely by the state of the single channel mode enable (see the CHSEL field of TEST3 register).
CSSF	CSSF = 1 if CSS = “0” CSSF = 2 if CSS = “1”	Cycles	The column sub-sample scale factor is determined by the state of the column sub-sample enable (see the CSS field of CONFIG register).
NCP	NCP = [last column address - first column address + 1] / CSSF	Cycles	The number of columns processed is determined by the width of the image window and the state of the column sub-sample enable.
CP	CP = CPO + (NCP * CT / SCSF)	Cycles	The column processing period is determined by the number of columns processed, the column processing overhead, and the column timing, and whether single channel mode is enabled.
MINC	**Accumulation Mode:** MINC >= 4 **Shutter Mode:** MINC >= 4 **Normal Mode:** MINC >= (ER + 5) * SCSF * CSSF / CT	Cols	The minimum allowable number of columns in the image window (MINC) is a function of the major operating mode, the minor operating mode, and the selected column timing. **Note:** The number of columns in every image window is forced to be a multiple of four by the register set interface. If not an integer, or not a multiple of four, MINC must be rounded up to the next highest multiple of four that satisfies the expression for MINC.

Table 31. Column Timing Related Equations

Symbol	Equation (units of clock cycles)	Units	Description
MNCT	MNCT >= (ER + 5) / CT **Note:** If not an integer, MNCT must be rounded up to the next highest integer that satisfies the expression for MINC.	CT	The minum allowable number of column timing periods within the column processing period applies only to the “Normal” mode of operation when calculating the sub-row exposure register settings.
SROWEXP	SROWEXP = {SROWEXPH, SROWEXPL} 0 <= SROWEXP <= CP - (MNCT * CT) - 1	Cycles	The sub-row exposure register count is equal to the number formed by the concatenation of the SROWEXPH and SROWEXPL registers, and bounded by the duration of the column processing period.
NCTD	NCTD = (SROWEXP - 3) / CT **Note:** If not an integer, NCTD must be rounded up to the next highest integer.	CT	The number of column timing periods of delay from the start of the column processing period to the start of the exposure reset is controlled by the sub-row exposure register settings and the synchronization of the start of the exposure reset within a column timing period.
SREXP	SREXP = CP - (NCTD * CT) - ER - 5 A simpler equation with an error (ERR) range of 0 <= ERR <= CT is: SREXP = CP - SROWEXP - ER - 6	Cycles	The sub-row exposure period applies only to the “Normal Mode” and is equal to the column processing time minus the sum of the sub-row exposure count and the minimum number of column timing periods required for the exposure reset period.
IEXP	IEXP = RS + (MNCT * CT)	Cycles	The duration of the illegal exposure reset time slot is equal to the sum of the row sample period and product of the minimum allowable number of columing timing periods and the column timing period.
ROWEXP	ROWEXP = {ROWEXPH, ROWEXPL}	Cycles	The row exposure count is equal to the number formed by the concatenation of the ROWEXPH and ROWEXPL registers.
EXP	**Normal Mode:** EXP = T * [SREXP + REXP * RP] **Shutter Mode:** EXP = T * REXP * RP	Time	In the “Normal” mode EXP represents the period of time that each pixel is exposed for. In the “Shutter” mode, EXP represents the “Exposure Delay Period” (see“Graphical Depiction of the Shutter Mode Image Capture Process” on page 47). EXP does not apply to the “Accumulation” mode.

Table 32. Exposure Control Related Equations

3.4.5 Exposure Control

The term “exposure” refers to the duration of time between the point at which a pixel is reset and subsequently sampled. Another term for this is the “integration time”. This section is intended to describe the mechanics of programming the HDCS sensor to expose each pixel for a pre-determined period of time. While methods of determining the correct exposure duration is not within the scope of this section, one should note that the PGA gain settings also factor into determining the correct exposure duration.

By default, pixels in the HDCS image sensor arrays are continuously integrating ambient light. During an image capture process, the period of time that a given row of pixels is integrated starts when an exposure reset is asserted and ends when either a sample reset is asserted or, in the case of consecutive “Accumulation Mode” image capture processes, a subsequent exposure reset is asserted. The time slot that an exposure (and sample) reset occurs in depends on the operat ing mode, but is of equal duration in all modes.

3.4.5.1 Accumulation Mode Exposure Control

In the “Accumulation Mode” the exposure reset occurs when all rows in the array are reset simultaneously at the beginning of the image capture process (see “Accumulation Mode Image Capture Process”) and is referred to as the global reset. Following the global reset, no rows are reset (either a sample or exposure reset) until a subsequent image cap ture process is initiated.

When operating in video mode, each row may be sampled multiple times without either an exposure or sample reset occuring on that row. Therefore, the duration of time that each row is exposed for is equal to the time from the start of the image capture process to when that particular row is sampled. The absolute time can be calculated as a function of the input clock frequency, the total number of rows that have been processed since the start of the image capture process, and the row processing time. Note that the row and sub-row exposure registers have no affect on the actual exposure duration in this mode of operation.

3.4.5.2 Shutter Mode Exposure Control

In the “Shutter Mode” a series of consecutive exposure resets, collectively called the “fast rolling reset”, are sequentially asserted in ascending order on individual rows within the image window boundary. The fast rolling reset occurs at the start of each captured frame. Note that in this mode the period of time between the exposure reset and the subsequent sample reset is not equal for each row and increases from the start of the frame to the end of the frame. For this mode to produce high quality pictures, the majority of the light integrated must be introduced during the exposure delay period by means of opening a mechanical shutter or timing the assertion of a bright flash of light.

The duration of the exposure delay period is primarily controlled by the row exposure register settings (ROWEXPH, ROWEXPL) which define the number of row processing periods to delay for. The row processing period is determined by the minor operating modes selected, the image window size, the selected column timing, and the system clock frequency. Since the exposure delay period is essentially and inter-frame delay, increasing the row exposure register value decreases the frame rate. Note that the sub-row exposure register settings have no effect in this mode of operation.

For more information, refer to“Shutter Mode Image Capture Process” on page 46, “Row Processing Period” on page 51, and “Timing Equations” on page 54.

3.4.5.3 Normal Mode Exposure Control

In the “Normal Mode” each row is exposed for an equal time duration that is programmed via the row exposure, sub-row exposure, column timing, configuration, and window coordinate registers. The resulting exposure time is therefore a function of the size of the image window, whether or not sub-sampling is enabled, whether or not both PGA/ADC channels are used, and the period of time required to process each row in the image window. The time required to process each row is a function of the number of columns processed in the image window and the time required to process each column.

The row exposure registers define the number of row processing periods that each row is integrated for and therefore control the majority of the integration time. Note that the row exposure registers value can exceed the number of rows in the image window by a significant amount. When this occurs, a delay is inserted between each frame which decreases the frame rate from the maximum possible rate. As the name implies, the sub-row exposure registers provide exposure control granularity of fractions of row processing periods.

For more information, refer to “Normal Image Capture Mode” on page 42, , “Basic Timing Controller Operations” on page 51, and “Timing Equations” on page 54.

3.4.5.4 Sub-row Exposure Control

The sub-row exposure registers only affect system behaviour when operating in the “Normal” mode. In this operating mode, exposure resets are asserted during the column processing time slot. As such, the duration of the exposure reset defines the minimum acceptable column processing duration, and hence the minimum number of columns of the image window for a set of operating conditions and timing parameters. When image windows with a sufficient number of columns are used, the sub-row exposure registers ({SROWEXPH, SROWEXPL}) can be used to skew the assertion of the exposure reset within the column processing time to provide for sub-row granularity of the integration time. While the sub-row exposure register is programmed in units of clock cycles, the initiation of the exposure reset is internally synchronized within the column timing time slot which results in an effective granularity of one column timing period. Note that increasing the sub-row exposure register value increases the delay from the start of column processing to the start of the exposure reset, and therefore decreases the sub-row exposure time.

Should the host system program an incompatible configuration such that either the exposure reset does not fit within the column processing time slot, or the sub-row exposure register values are so large that the exposure reset is delayed past the end of the column processing time slot, an internal flag is asserted and can be used to notify the host system of the error condition. In the event an exposure reset error condition occurs, the “EEF” flag of the “STATUS” register will be asserted and will remain asserted until cleared by host system intervention. The system can also be programmed to generate an interrupt request when this flag is asserted.

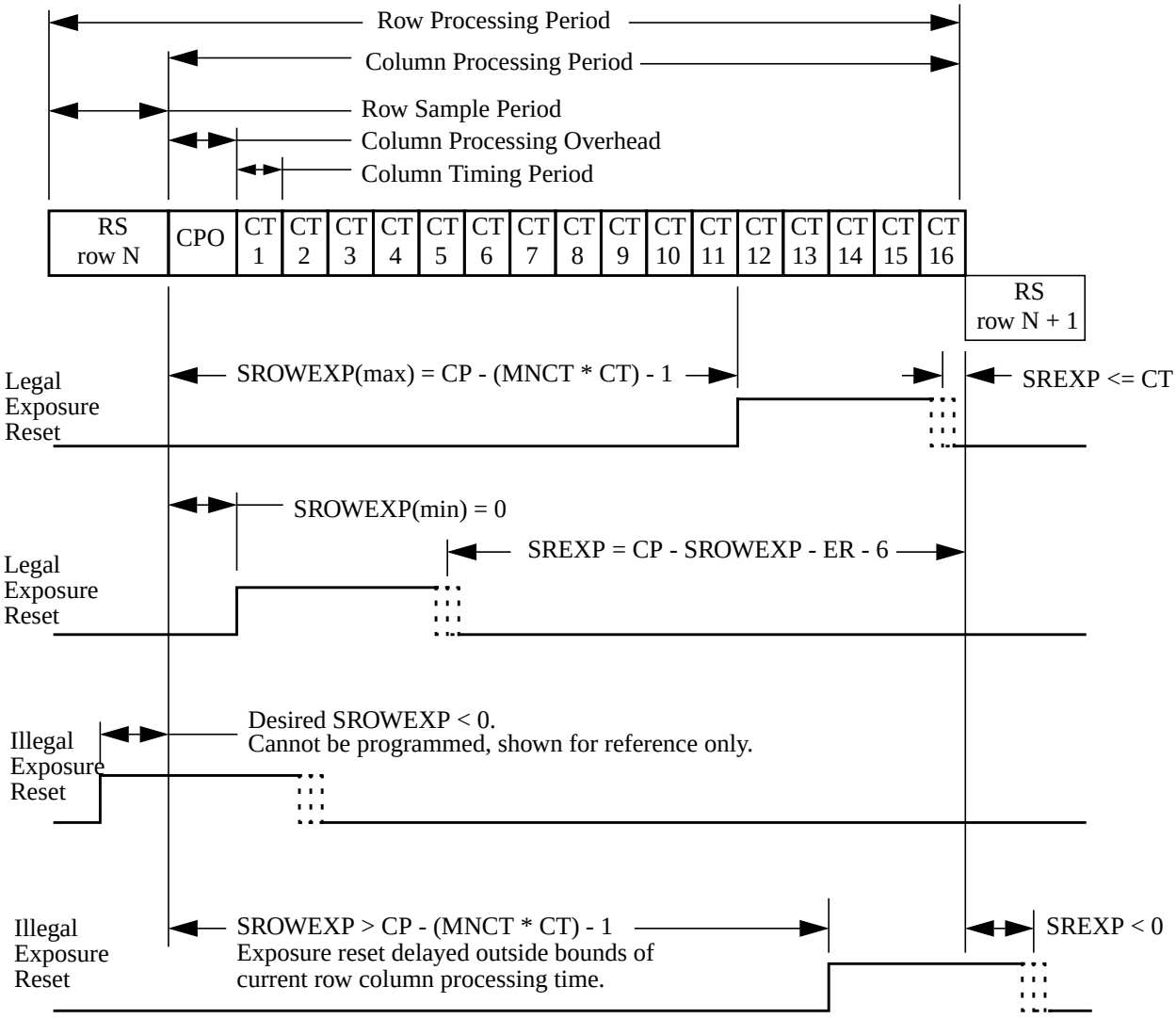


Figure 37. Sub-row Exposure Control

3.4.5.5 Determining the Normal Mode Exposure Register Settings

Assuming the desired integration time is known, an integral number of clock cycles, and represented by “TEXP”, the row exposure register formed by the concatenation of ROWEXPH and ROWEXPL should be loaded with the integer quotient of the desired integration time divided by the time required to process one row;

ROWEXP = {ROWEXPH, ROWEXPL} = quotient (TEXP / (T * RP))

Letting the remaining integration time be represented by SREXP, the sub-row exposure (SROWEXP) register formed by the concatenation of the SROWEXPH and SROWEXPH registers should be loaded with a value determined by the following equations:

SREXP = TEXP / T - (ROWEXP * RP)

SROWEXP = CP - SREXP - ER - 6

A negative SROWEXP value resulting from the above calculation indicates that desired integration time, combined with the configured row processing time, corresponds to an illegal value. A value greater than the legal range indicates an attempt to skew the exposure reset into the sample reset time.

3.4.5.6 Compensating for Illegal SROWEXP Settings.

When the desired integration time results in an illegal SROWEXP register value, the programmer must make a decision on how to compensate for this. The options include setting the SROWEXP register to the nearest legal value or modifying the column processing time to shift the row sample time slots such that they no longer coincide with the desired integration time.

Setting the SROWEXP register value to the nearest legal value will result in the actual integration time deviating from the desired integration time by up to one half of the sum of the row sample time plus the product of minimum allowable number of column timing periods multiplied by the column timing period (0.5 * (RS + MNCT * CT)). At 25 MHz and assuming maximum column timing, this corresponds to a deviation of approximately:

MNCT >= (ER + 5) / CT = (100 + 5) / 40 = 2.6 which, rounded up to the next highest integer results in: MNCT = 3.

T * 0.5 * [RS + (MNCT * CTmax)] = 40 ns * 0.5 * [186 + (3 * 40)] = 6.12 us.

While this likely to be negligible in the vast majority of cases, should this deviation prove to be unacceptable the programmer has the option of modifying either the window size or the column timing to shift the row sample time such that it no longer coincides with the desired integration setting.

For example the column processing time for several configurations at 25 MHz is listed below:

VGA window, single channel mode disabled, column sub-sampling disabled, 11 cycle column timing: 140.9 us

VGA window, single channel mode disabled, column sub-sampling disabled, 12 cycle column timing: 153.7 us

CIF window, single channel mode disabled, column sub-sampling disabled, 11 cycle column timing: 77.5 us

CIF window, single channel mode disabled, column sub-sampling disabled, 12 cycle column timing: 84.6us

Depending on the window size and operating mode, increasing the column timing by approximately one clock cycle is sufficient to shift the row sample time to no longer coincide with the desired integration time. While increasing the column timing does have a negative impact on the overall frame rate, the actual percent impact varies depending on the selected exposure settings, column timing, and the window size.

3.4.5.7 Exposure Control Example: Legal SROWEXP value

The following example is intended to depict how a host system programmer would determine the correct exposure register settings to achieve an exposure of a predefined duration that results in legal sub-row exposure register settings.

Using the appropriate equations (see “Timing Equations” on page 54) and assuming the desired exposure duration is 5 ms, 11 cycle column timing, a VGA image window, column sub-sampling is disabled, single channel mode is disabled, and a 25 MHz clock input:

T = 40 ns

The number of columns processed is: NCP = (last address - first address + 1) / CSSF = (639 - 0 + 1) / 1 = 640

The number of cycles required to process all columns in one row is:

CP = CPO + (CT * NCP) / SCSF = 2 + (11 * 640) / 2 = 3,522 cycles

The time required to process an entire row is:

RP = [RS + CP] = [186 + 3,522] = 3,708 cycles.

The ROWEXP registers should be loaded with the integer quotient of the desired time divided by the time required to process one row.

ROWEXP = TEXP / (T * RPC) = 5 ms / (40 ns * 3,708 cycles) = 33.711 rows => integer quotient = 33 rows. Therefore, ROWEXPH = 0, and ROWEXPL = 33.

The remaining time corresponds to:

SREXP = TEXP / T - (ROWEXP * RP) = (5 ms / 40 ns) - (33 * 3,708) = 2,636 cycles.

SROWEXP = CP - ER - 6 - SREXP = 3,522 - 100 - 6 - 2,636 = 780

The desired sub-row exposure register value must now be compared to the legal range. The minimum allowable number of column timing periods for the current configuration is:

MNCT >= (ER +5) / CT = (100 + 5) / 11 which, rounded up to the next highest integer equals 10.

Therefore, the maximum sub-row exposure register value for the current configuration is:

SROWEXP(max) = CP - (MNCT * CT) - 1 = 3,522 - (10 * 11) - 1 = 3,411 cycles.

The resulting SROWEXP value is within the legal range of 0 - 3,411 cycles. Since there is no need to choose the nearest legal value of modify the column timing, the SROWEXPH register should be loaded with 3, and the SROWEXPL register should be loaded with 12 (decimal).

3.4.5.8 Exposure Control Example: Illegal SROWEXP value

The following example is intended to depict how a host system programmer would determine the correct exposure register settings to achieve an exposure of a predefined duration, and compensate for a result that corresponds to illegal sub-row exposure register settings.

Using the appropriate equations (see “Timing Equations” on page 54) and assuming the desired exposure duration is 5.04 ms, 11 cycle column timing, a VGA image window, column sub-sampling is disabled, single channel mode is disabled, and a 25 MHz clock input:

T = 40 ns

The number of columns processed is: NCP = (last address - first address + 1) / CSSF = (639 - 0 + 1) / 1 = 640

The number of cycles required to process all columns in one row is:

CP = CPO + (CT * NCP) / SCSF = 2 + (11 * 640) / 2 = 3,522 cycles

The time required to process an entire row is:

RP = [RS + CP] = [186 + 3,522] = 3,708 cycles.

The ROWEXP registers should be loaded with the integer quotient of the desired time divided by the time required to process one row.

ROWEXP = TEXP / (T * RPC) = 5.04 ms / (40 ns * 3,708 cycles) = 33.981 rows => integer quotient = 33 rows. Therefore, ROWEXPH = 0, and ROWEXPL = 33.

The remaining time corresponds to:

SREXP = TEXP / T - (ROWEXP * RP) = (5.04 ms / 40 ns) - (33 * 3,708) = 3,636 cycles.

SROWEXP = CP - ER - 6 - SREXP = 3,522 - 100 - 6 - 3,636 = -220 cycles.

The result is a negative number which indicates that the desired exposure reset timing does not fall within the column processing time slot. If this error is acceptable, the programmer could simply set the sub-row exposure register value to 0 and leave the row exposure register set to 33 which, at 25 MHz corresponds to the exposure duration being 8.8 us seconds less than desired. A slightly better result could be obtained by recognizing that 220 cycles is greater than half of the duration of the illegal exposure reset time slot which can be calculated as follows:

MNCT >= (ER +5) / CT = (100 + 5) / 11 which, rounded up to the next highest integer equals 10.

IEXP = RS + (MNCT * CT) = 186 + (10 * 11) = 296 cycles.

By setting the row exposure registers to correspond to 34 rows and setting the sub-row exposure register to it’s maximum value the deviation from the desired exposure duration can be reduced from 220 cycles to 76 cycles (296 - 220) which corresponds to an error of 3.04 us longer than desired. If this is still unacceptable for some reason, the programmer could modify the column timing to shift the illegal exposure reset time slot relative to the desired exposure duration.

4. Interface Reference

4.1 System Configuration

4.1.1 Serial Interface

When IMODE equals ‘0’ the serial interface operates as a synchronous serial slave. The 7 bit device address is ‘101_0101’. The device address may be ignored by setting the DAD bit of the ICTRL register.

When IMODE equals ‘1’ and TCLK equals ‘0’ the serial interface operates as a half duplex UART slave. After system reset the UART operates at 9600 baud. Register writes to the BRATE and BFRAC registers can increase the BAUD rate.

4.1.2 Pad Speed

The PDRV register controls the switching speed of the HDCS sensor output pins. There are four groupings of output pins that can be controlled independently: DATA, DRDY, TxD, and STATUS. The STATUS group includes nROW, nFRAME_nSYNC, and nIRQ_nCC. Each group has 4 possible switching speed options. After system reset, the output pins are initialized to the fastest switching speed.

Since faster switching pads generate a small amount of noise, it is possible that under some conditions image quality could be enhanced by slowing the switching speed of the output pins.

4.1.3 Status Flags

There are three status output pins: nROW, nFRAME_nSYNC, and nIRQ_nCC. The status flags are all active low.

PCTRL[RCE]	PCTRL[LVR]	Mode: Notes
‘0’	‘x’	nROW Disabled. Drives a constant ‘1’.
‘1’	‘0’	nROW pulse mode. Assert low for 4 cycles after last data for a sensor row is transferred.
‘1’	‘1’	nROW level mode. Assert low when first data is transferred for a sensor row. De-assert when last data is transferred for a sensor row.

Table 33. nROW Status Flag Control

PCTRL[FSE]	PCTRL[FSS]	PCTRL[LVF]	Mode: Notes
‘0’	‘x’	‘x’	nFRAME_nSYNC is disabled. Drives a constant ‘1’.
‘1’	‘1’	‘0’	nSYNC Pulse Mode. Assert 4 cycle active low pulse at the start of integration.
‘1’	‘1’	‘1’	nSYNC Level Mode. Assert low at beginning of integration. De-assert when first data is transferred.
‘1’	‘0’	‘0’	nFRAME Pulse Mode. Assert low for 4 cycles after the last data for a frame is transferred.
‘1’	‘0’	‘1’	nFRAME Level Mode. Assert low when first data for a frame is transferred. De-assert after last data for a frame is transferred.

Table 34. nFRAME_nSYNC Status Flag Control

PCTRL[ICE]	PCTRL[IPD]	PCTRL[LVC]	Mode: Notes
‘0’	‘0’	‘x’	Open Drain IRQ with weak pull-up. Interupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
‘0’	‘1’	‘x’	IRQ driving to full high and low levels. Interupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
‘1’	‘x’	‘0’	nCC (capture complete) pulse mode. Assert low for 4 cycles when the capture process completes. (After last data from last frame is transferred)
‘1’	‘x’	‘1’	nCC (capture complete) level mode. Assert low when RUN bit is set. De-Assert after capture completes. (After last data for last frame is transferred).

Table 35. nIRQ_nCC Status Flag Control

CONFIG[CFC] continuos frame capture	CONFIG[SFC] stop when frame complete	Capture Complete when ...
‘0’	‘0’	At end of the first frame if CONTROL[RUN] is not de-asserted. Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode
‘0’	‘1’	After last data is transferred for first frame.is de-asserted in.

Table 36. Capture Complete

CONFIG[CFC] continuos frame capture	CONFIG[SFC] stop when frame complete	Capture Complete when ...
'1'	'0'	Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode
'1'	'1'	After last data is transferred for frame that CONTROL[RUN] is de-asserted in.

Table 36. Capture Complete

4.1.4 DATA and DRDY timing

The timing of the DATA and DRDY pins is set by the DSC field of the ICTRL register, and the RPC field and DHC fields of the IFTMG register. See figure 88 in the Parallel Sensor Data Out section of the System Interface chapter for a timing diagram. The DATA/DRDY timing is set relative to the column timing. Data for 2 pixels are transferred during each period of column timing. Column timing is set by the ASTRT and PSMP fields of the TCTRL register.

4.1.5 DATA formatting

The ARES field of the ADCCTRL register determines the number of bits of resolution produced by the ADC. Legal values are 8, 9, and 10. The MSB for the ADC is always output on DATA[9]. The unused LSB bits of DATA will be '0'. It is possible to have the ADC produce 10 bits of resolution, then apply a transform to the ADC data to cut it down to 8 bits. The DOD field of the ICTRL register selects a data transforms. The data transforms are 1) pass the data directly without transform, 2) rounding, 3) saturation.

4.1.6 Setting Viewing Window Co-ordinates

The FWCOL register specifies the first column in the viewing window. The LWCOL register specifies the last column in the viewing window. The FWROW register specifies the first row in the viewing window. The LWROW register specifies the last row in the viewing window.

The array is surrounded by 4 border pixels and 8 dark pixels. The border and dark pixels are also addressable.

PIXEL TYPE	VGA (640) COLUMN ADDRESS	VGA (480) ROW ADDRESS	CIF (352) COLUMN ADDRESS	CIF (288) ROW ADDRESS
Dark Pixels	0-7	0-7	0-7	0-7
Border Pixels	8-11	8-11	8-11	8-11

Table 37. HDCS Sensor Viewing Window Co-ordinates

PIXEL TYPE	VGA (640) COLUMN ADDRESS	VGA (480) ROW ADDRESS	CIF (352) COLUMN ADDRESS	CIF (288) ROW ADDRESS
Normal Viewing Pixels	12-651	12-491	12-363	12-299
Border Pixels	652-655	492-495	364-367	300-303
Dark Pixels	651-663	496-503	368-375	304-311

Table 37. HDCS Sensor Viewing Window Co-ordinates

Note that the FWCOL, LWCOL, FWROW, LWCOL registers do not include the 2 LSB. The FWCOL and FWROW registers add the 2 LSB ‘00’ on to the binary number you specify. While LWCOL and LWCOL add the 2 LSB ‘11’ onto the number you specify. For example say you want to specify the normal 640 by 480 viewing window in HDCS 2000/2100. Set FWCOL to ‘0000_0011’, set FWROW to ‘0000_0011’, set LWCOL to ‘1010_0010’ and set LWROW to ‘0111_1110’. Internally, the sensor appends the 2 LSB to achieve: first column address equals ‘00_0000_1100’ (12), last column address equals ‘10_1000_1011’ (651), first row address equals ‘00_0000_1100’ (12), and last row address equals ‘01_1111_1011’ (491).

4.1.7 Setting Column Timing

Column timing is determined by PSMP and ASTRT fields of the TCTRL register. Column timing is the number of cycles to sample and convert 2 pixels (there are 2 parallel PGA/ADC channels). The number of cycles to sample and convert pixel data is PSMP + ASTRT + 4. This is also the number of cycles in which 2 pixels are output. See the Programming Reference chapter for more details.

The faster the column timing the faster the data output, and the less motion artifacts in the picture.

4.1.8 Setting Exposure

There are 2 components of exposure (integration) time: 1) Row Exposure and 2) Sub-row Exposure. Total integration time equals row exposure time plus sub-row exposure time. The ROWEXPL and ROWEXPH registers determine the row exposure time. The SROWEXPL and SUBROWEXPH registers determine the sub-row exposure time. See the Programming Reference chapter for more details.

Row exposure is the number of row processing periods to wait. Row exposure is based on the number of columns per row, and the column processing time. Sub-row exposure is an additional delay that is shorter than 1 row.

4.1.9 Selecting Mode of Operation

The MODE field of the CONFIG register determines the operating mode. There are three mode of operation: 1) Normal, 2) Shutter, and 3) Accumulation.

4.1.10 Selecting Mode of Scanning

The CSS (column sub-sample) and RSS (row sub-sample) fields of the CONFIG register determine scanning mode. Note that when CSS is active the number of effective columns to use in calculating exposure is cut in half. Note that when RSS

is active the number of effective rows used to calculate exposure is cut in half. For example if you want row exposure to be the time to process 8 rows, if RSS equals ‘1’ then the number 16 should be put into the ROWEXPL register.

The HAVG bit of the ICTRL register enables horizontal averaging mode. This does not effect the exposure time, but it halves the number of pixels that are output per row. For each row every other pixel of the same color is averaged together and only one value is output. If CSS equals ‘1’ then the averaging is performed after column sub-sampling.

CSS	HAVG	Pixel Columns Read	Pixel Columns Output
0	0	64	64
0	1	64	32
1	0	32	32
1	1	32	16

Table 38. Effect of CSS and HAVG for viewing window with 64 columns.

4.1.11 Starting and Stopping Operation

Operation starts when the RUN bit of the CONTROL register is asserted. If the CFC (continuous frame capture) bit of the CONFIG register equals ‘0’, operation automatically stops at the end of the first frame. If CFC equals ‘1’ operation does not terminate until RUN is de-asserted. If the SFC (stop when frame complete) bit of the CONFIG register equals ‘0’ when the RUN bit is de-asserted operation immediately halts, even if the current frame is only partially processed. If SFC equals ‘1’ when run is de-asserted, then operation stops at the end of the current frame.

4.2 Sending Commands on the Serial Interface

4.2.1 Device Address Control

The DAD (device address disable) bit of the ICTRL register can disable the requirement to send the device address byte for the serial synchronous interface. After system reset, the HDCS Chip requires that the serial synchronous interface use the device address byte. The first register write must use the device address. If the serial interface is point to point, the device address is unnecessary overhead. If the first write sets DAD to ‘1’, then the device address will not be required again. See the Serial Interface section of the Host System Interface chapter.

If the serial interface is configured as a UART slave, the interface must be point to point, and the device address is not used.

4.2.2 Polling the STATUS register

It is not necessary to poll the register set if the status flags are used. However if the status pins are not used it may be necessary to poll the STATUS register to detect an event such as the end of a frame. The AAD (auto address disable) bit of the ICTRL register normally equals ‘0’ so that the register address is incremented after each transfer of a multiple byte transfer. For the UART this means that a 2 byte read command must be transmitted for each read of the STATUS register. For the serial synchronous interface with the device address enabled a 2 byte write command to set up the register address followed by a one byte read command is required for each reading of the STATUS register. For the serial synchronous interface with the device address disabled a one byte read command must be transmitted for each reading of the STATUS register.

If AAD equals ‘1’ the register address does not increment between transfers. In UART mode the register address can be set to the STATUS register and the transfer count of the read command can be set to ‘N’. HDCS Sensor will transmit the value of the STATUS register ‘N’ times. In serial synchronous mode if a read command is issued to the STATUS register address, the STATUS register will be repeatedly transmitted until a NACK or STOP.

4.3 Serial Synchronous Setup Example

Assume that the HDCS Sensor needs to be configured to continuously transmit CIF (352 by 288) frames with no subsampling or averaging using a point to point serial synchronous interface. The desired column timing is 12 cycles per pixel pair. Every 12 cycles 2 data values must be sent, so each data will be driven 6 cycles with a 3 cycle DRDY. Assume integration time equal to 743.36 uSec. If part of a frame is transmitted, then the entire frame must be transmitted. The nROW, nFRAME, nCC status flags will be used as levels. Border pixels will not be used.

Integration time of 743.36 uSec equals 18584 at 25 MHz. There are 352 columns, so there are 176 column pairs to process. Each pixel pair is processed for 12 cycles, for a total read out time of 2112 cycles per row. There are 202 cycles of overhead per row for a total of 2314 cycles per row. Eight rows of integration takes 18512 cycles, which leaves 72 cycles of sub-row exposure. The Exposure register should be set to 8 rows.

The sub-row exposure register is then set to 2040 cycles (2112 cycles of readout time - 72 cycles of extra exposure).

95.440 uSec equals Each row has 352 columns. Columns are processed in pairs. There are 176 (352/2) column pairs in a row. To add 6 columns of integration delay for the sub-row delay, the sub-row exposure register pair must be set to delay for 170 (176-6) column timing delays. The sub-row exposure register must be set to 2040 (170 * 12) cycles. See the Programming Reference chapter for more details.

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: start condition			
master:1010101_0 slave: 0 (ACK)	Command		[7:1] Device Address [0] Write
master: 0_000011_0 slave: 0 (ACK)	Register Address	PCTRL (3)	[7] reserved [6:1] Register Address [0] Write
master: 111_11_01_1 slave: 0 (ACK)	Write Data	PCTRL(3)	[7:5] Status Flags Act as levels [4:3] Enable nCC (capture complete) [2:1] Enable nFRAME [0] Enable nROW
master: 00_00_00_00 slave: 0 (ACK)	Write Data	PDRV(4)	[7:6] Fastest switching speed for TxD [5:4] Fastest switching speed for Status Flags [3:2] Fastest switching speed for DRDY [1:0] Fastest switching speed for DATA
master: 0_10_0_00_1_0 slave: 0 (ACK)	Write Data	ICTRL(5)	[7] Do not use Horizontal Averaging [6:5] DSC: 2 cycle DATA valid before assert DRDY [4] No phase shift of DRDY/DATA [3:2] Normal 10 bit output without rounding etc. [1] Disable the device address for future serial commands. [0] Register Address automatically increments. (If this bit is set it must be last byte of the command)
master: 00_0_01_010 slave: 0 (ACK)	Write Data	ITMG(6)	[7:6] Reserved [5] Positive active DRDY [4:3] DHC: DATA still valid 1 cycle after DRDY deasserts [2:0] RPC: DRDY high for 3 cycles. (note DATA driven for a total of 6 cycles DSC+RPC+DHC)
master: 00000000 slave: 0 (ACK)	Write Data	BFRAC(7)	Not using UART, so value does not matter.
master: 00000000 slave: 0 (ACK)	Write Data	BRATE(8)	Not using UART, so value does not matter.

Table 39. Serial Synchronous Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0000_1010 slave: 0 (ACK)	Write Data	ADCCTRL(9)	[7:4] Reserved [3:0] 10 bit ADC resolution
master: 00000011 slave: 0 (ACK)	Write Data	FWROW(10)	[7:0] The HDCS Sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first row in the viewing window is row 12. (this skips 8 dark pixels and 4 border pixels)
master: 00000011 slave: 0 (ACK)	Write Data	FWCOL(11)	[7:0] The HDCS sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first column of the viewing window is 12. (this skips 8 dark pixels and 4 border pixels)
master: 01001010 slave: 0 (ACK)	Write Data	LWROW(12)	[7:0] The HDCS sensor tacks ‘11’ on the LSB end of this number to get 01_0010_1011 (299). The last row of the viewing window is 299. A total of 288 rows for CIF.
master: 10010010 slave: 0 (ACK)	Write Data	LWCOL(13)	[7:0] The HDCS sensor tacks ‘11’ on the LSB end of this number to get 10_0100_1011 (363). The last column of the viewing window is 363. A total of 352 columns for CIF.
master: 0_00_00110 slave: 0 (ACK)	Write Data	TCTRL(14)	[7] Reserved [6:5] ASTRT = 2 cycles [4:0] PSMP = 6 cycles This sets the column timing. Number of cycles to process a column pair = SCC = PSMP +ASTRT + 4 = 12 cycles.
master: 0_0000101 slave: 0 (ACK)	Write Data	ERECPGA(15)	PGA gain for green pixels in green/red rows. This number should come from prior measurements.
master: 0_0000111 slave: 0 (ACK)	Write Data	EROCPGA(16)	PGA gain for red pixels. This number should come from prior measurements.
master: 0_0001010 slave: 0 (ACK)	Write Data	ORECPGA(17)	PGA gain for blue pixels. This number should come from prior measurements.
master: 0_0000101 slave: 0 (ACK)	Write Data	OROCPGA(18)	PGA gain for green pixels in green/blue rows. This number should come from prior measurements.
master: 0000_1000 slave: 0 (ACK)	Write Data	ROWEXPL(19)	Low Bits of Row Exposure. Integration lasts 8whole rows.
master: 0000_0000 slave: 0 (ACK)	Write Data	ROWEXPH(20)	High Bits of Row Exposure. Integration lasts 8 whole rows.
master:0100_1000 slave: 0 (ACK)	Write Data	SROWEXPL(21)	Low Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 1111_1000 slave: 0 (ACK)	Write Data	SROWEXPH(22)	High Bits of Sub-row Exposure. Total of 2040 cycles as explained above.

Table 39. Serial Synchronous Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 00_00_11_00 slave: 0 (ACK)	Write Data	CONFIG(23)	[7:6] Reserved [5:4] No row or column subsampling [3] Continuous frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset
master: 00000_1_00 slave: 0 (ACK)	Write Data	CONTROL(24)	[2] RUN bit. Integration begins when this pin is turned on.
master: stop condition			nCC asserts as an active low level.

Table 39. Serial Synchronous Setup Example

4.4 Example of Changing Modes

In this example the previous capture process must be changed capture a single CIF frame with the same exposure time but using column subsampling and row subsampling.

In order to change modes the initial capture process must first be stopped. Then the new register settings must be applied, and then the new capture process must be started.

Since column subsampling effectively changes the number of columns, and the row exposure is based on the number of columns, the exposure registers need to be updated to keep the same exposure time. The integration time was previously calculated to be 18584 cycles. With subsampling only 176 (352/2) columns will be sampled which means there are 88 (176/2) column pairs. Read out time for the columns will be 1056 cycles per row (88 * 12). Each row has 202 cycles of overhead for a total of 1258 cycles per row. Setting the row exposure register to 14 rows will account for 17612 cycles, leaving 972 cycles that sub-row exposure register must account for. The sub-row exposure register should be set to 24 (1056 - 972).

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: start condition			Note: the previous example disabled the need for a device address.
master: 0_011000_0 slave: 0 (ACK)	Register Address	CONTROL(24)	[7] reserved [6:1] Register Address [0] Write
master: 00000_0_00 slave: 0 (ACK)	Write Data	CONTROL(24)	[3] Turn off the RUN bit. Since SFC == ‘1’, The HDCS sensor will stop at the end of the current frame.

Table 40. Serial Synchronous Change Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: stop condition			Master waits for the end of the capture process when the nCC status flag (acting as a level) de-asserts. If the nCC status flag is not used, this can be determined by polling the STATUS register.
master: start condition			
master: 0_010011_0 slave: 0 (ACK)	Register Address	ROWEXPL(19)	[7] reserved [6:1] Register Address [0] Write
master: 0000_1110 slave: 0 (ACK)	Write Data	ROWEXPL(19)	Low Bits of Row Exposure. Integration lasts 14 whole rows.
master: 0000_0000 slave: 0 (ACK)	Write Data	ROWEXPH(20)	High Bits of Row Exposure. Integration lasts 14 whole rows.
master:0001_1000 slave: 0 (ACK)	Write Data	SROWEXPL(21)	Low Bits of Sub-row Exposure. Total of 24 cycles as explained above.
master: 0000_0000 slave: 0 (ACK)	Write Data	SROWEXPH(22)	High Bits of Sub-row Exposure. Total of 24 cycles as explained above.
master: 00_11_01_00 slave: 0 (ACK)	Write Data	CONFIG(23)	[7:6] Reserved [5:4] Row subsampling and Column subsampling both enabled. [3] Single frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset
master: 00000_1_00 slave: 0 (ACK)	Write Data	CONTROL(24)	[2] RUN bit. Integration begins when this pin is turned on. The above settings will run 1 frame and automatically stop. nCC will de-assert when done.
master: stop condition			nCC asserts as an active low level.

Table 40. Serial Synchronous Change Example

4.5 UART Setup Example

Same setup as the serial synchronous setup example. Only difference is that an additional write is performed to increase the bit rate to send 1 bit every 16 cyles (640 nSec).

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 0000111_0 master: 1 (stop)	Register Address	BFRAC(7)	[7:1] Device Address [0] Write
master: 0 (start) master: 0000_0001 master: 1 (stop)	Transfer Count		Transfer 2 bytes
master: 00000000 slave: 0 (ACK)	Write Data byte 1	BFRAC(7)	Change bit rate to 1 bit every 16 cycles.
master: 00000000 slave: 0 (ACK)	Write Data byte 2	BRATE(8)	Change bit rate to 1 bit every 16 cycles. New Bit Rate in effect after this write.
master: 0 (start) master: 0000011_0 master: 1 (stop)	Register Address	PCTRL(3)	[7:1] Device Address [0] Write
master: 0 (start) master: 0001_0101 master: 1 (stop)	Transfer Count		Transfer 22 bytes
master: 0 (start) master: 111_11_01_1 master: 1 (stop)	Write Data byte 1	PCTRL(3)	[7:5] Status Flags Act as levels [4:3] Enable nCC (capture complete) [2:1] Enable nFRAME [0] Enable nROW
master: 0 (start) master: 00_00_00_00 master: 1 (stop)	Write Data byte 2	PDRV(4)	[7:6] Fastest switching speed for TxD [5:4] Fastest switching speed for Status Flags [3:2] Fastest switching speed for DRDY [1:0] Fastest switching speed for DATA
master: 0 (start) master: 0_10_0_00_1_0 master: 1 (stop)	Write Data byte 3	ICTRL(5)	[7] Do not use Horizontal Averaging [6:5] DSC: 2 cycle DATA valid before assert DRDY [4] No phase shift of DRDY/DATA [3:2] Normal 10 bit output without rounding etc. [1] Disable the device address for future serial commands. [0] Register Address automatically increments. (If this bit is set it must be last byte of the command)

Table 41. UART Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 00_0_01_010 master: 1 (stop)	Write Data byte 4	ITMG(6)	[7:6] Reserved [5] Positive active DRDY [4:3] DHC: DATA still valid 1 cycle after DRDY de-asserts [2:0] RPC: DRDY high for 3 cycles. (note DATA driven for a total of 6 cycles DSC+RPC+DHC)
master: 0 (start) master: 00000000 master: 1 (stop)	Write Data byte 5	BFRAC(7)	same as current value..
master: 0 (start) master: 00000000 master: 1 (stop)	Write Data byte 6	BRATE(8)	same as current value.not matter.
master: 0 (start) master: 0000_1010 master: 1 (stop)	Write Data byte 7	ADCCTRL(9)	[7:4] Reserved [3:0] 10 bit ADC resolution
master: 0 (start) master: 00000011 master: 1 (stop)	Write Data byte 8	FWROW(10)	[7:0] The HDCS sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first row in the viewing window is row 12. (this skips 8 dark pixels and 4 border pixels)
master: 0 (start) master: 00000011 master: 1 (stop)	Write Data byte 9	FWCOL(11)	[7:0] The HDCS sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first column of the viewing window is 12. (this skips 8 dark pixels and 4 border pixels)
master: 0 (start) master: 01001010 master: 1 (stop)	Write Data byte 10	LWROW(12)	[7:0] The HDCS sensor tacks ‘11’ on the LSB end of this number to get 01_0010_1011 (299). The last row of the viewing window is 299. A total of 288 rows for CIF.
master: 0 (start) master: 10010010 master: 1 (stop)	Write Data byte 11	LWCOL(13)	[7:0] The HDCS sensor tacks ‘11’ on the LSB end of this number to get 10_0100_1011 (363). The last column of the viewing window is 363. A total of 352 columns for CIF.
master: 0 (start) master: 0_00_00110 master: 1 (stop)	Write Data byte 12	TCTRL(14)	[7] Reserved [6:5] ASTRT = 2 cycles [4:0] PSMP = 6 cycles This sets the column timing. Number of cycles to process a column pair = SCC = PSMP +ASTRT + 4 = 12 cycles.
master: 0 (start) master: 0_0000101 master: 1 (stop)	Write Data byte 13	ERECPGA(15)	PGA gain for green pixels in green/red rows. This number should come from prior measurements.

Table 41. UART Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 0_0000111 master: 1 (stop)	Write Data byte 14	EROCPGA(16)	PGA gain for red pixels. This number should come from prior measurements.
master: 0 (start) master: 0_0001010 master: 1 (stop)	Write Data byte 15	ORECPGA(17)	PGA gain for blue pixels. This number should come from prior measurements.
master: 0 (start) master: 0_0000101 master: 1 (stop)	Write Data byte 16	OROCPGA(18)	PGA gain for green pixels in green/blue rows. This number should come from prior measurements.
master: 0 (start) master: 0000_1000 master: 1 (stop)	Write Data byte 17	ROWEXPL(19)	Low Bits of Row Exposure. Integration lasts 8whole rows.
master: 0 (start) master: 0000_0000 master: 1 (stop)	Write Data byte 18	ROWEXPH(20)	High Bits of Row Exposure. Integration lasts 8 whole rows.
master: 0 (start) master:0100_1000 master: 1 (stop)	Write Data byte 19	SROWEXPL(21)	Low Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 0 (start) master: 1111_1000 master: 1 (stop)	Write Data byte 20	SROWEXPH(22)	High Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 0 (start) master: 00_00_11_00 master: 1 (stop)	Write Data byte 21	CONFIG(23)	[7:6] Reserved [5:4] No row or column subsampling [3] Continuous frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset
master: 0 (start) master: 00000_1_00 master: 1 (stop)	Write Data byte 22	CONTROL(24)	[2] RUN bit. Integration begins when this pin is turned on.
			nCC asserts as an active low level.

Table 41. UART Setup Example

5. Host System Interface

5.1 Overview of Host System Interface

The host system interface is comprised of two data paths and status flags. The serial data path is used to read and write to the HDCS sensor register set. The parallel data path is used to output 10 bit sensor array data along with a valid signal. The status signals are nROW, nFRAME_nSYNC, and nIRQ_nCC. The status signals operate in multiple modes and are described below.

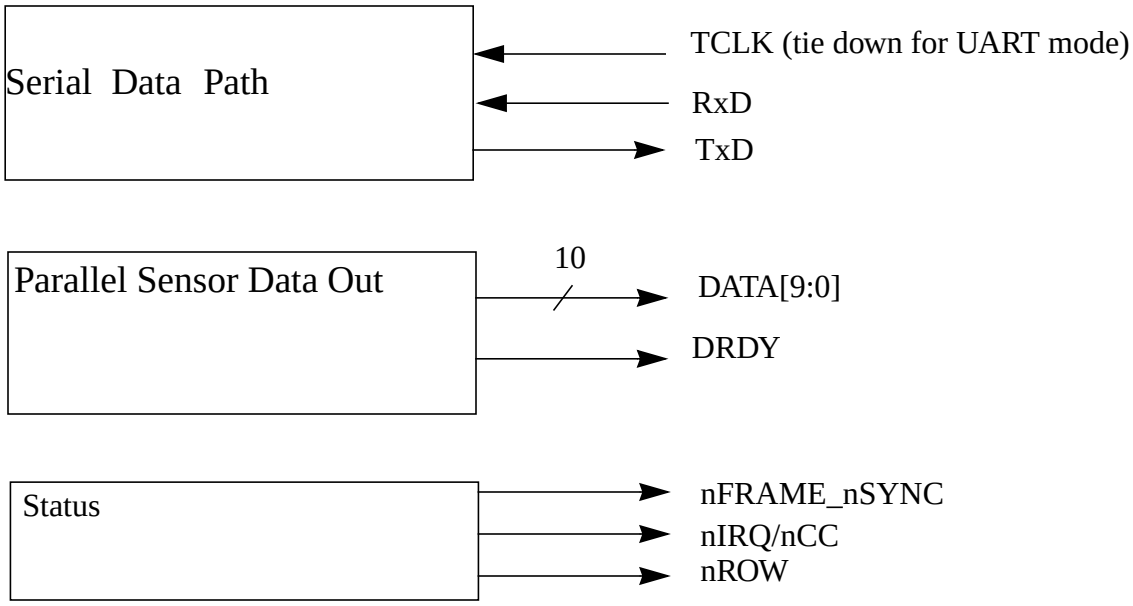


Figure 38. The HDCS sensor Data Paths

5.2 The HDCS sensor 44 pin package diagram

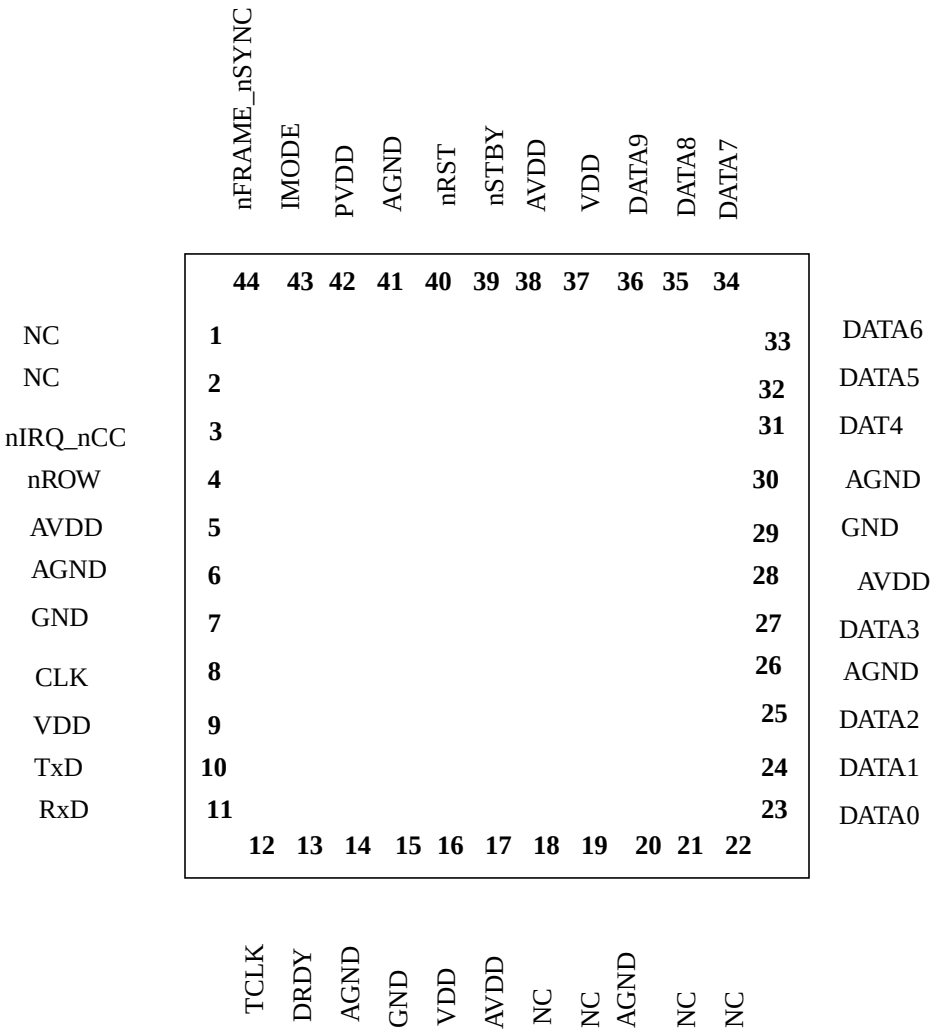


Figure 39. HDCS 44 pin package diagram

5.3 HDCS Image Sensor Pin Description

Pkg Pins	Signal Name	Type	Value after System Reset
1	nReset	Input	
1	Clock	Input	
1	nSTBY	Input	
1	IMODE	Input	
10	Data9, Data8, Data7, Data6, Data5, Data4, Data3, Data2, Data1, Data0	Output	“00_0000_0000”
1	DRDY	Output	“0”
1	RxD	Input	
1	TxD	Output	“1”
1	TCLK	Input	
1	nFRAME_nSYNC	I/O	“1”
1	nROW	Output	“1”
1	nIRQ_nCC	Output	“1”
3	VDD	VDD	Digital Power
3	GND	GND	Digital Ground
1	PVDD	PVDD	Array Power
4	AVDD	AVDD	Analog Power
6	AGND	AGND	Analog and Substrate Ground
6	NC	NC	No Connect
44			

Table 42. External Pin List

5.3.1 Pad Descriptions.

5.3.1.1Note for all PADS.

- When asserted low nRST performs a full system reset with the clock running. When asserted low nSTBY gates the clock and also does a system reset. When nRST and nSTBY are asserted at the same time the output pads

are tri-stated as a board test function. During normal operation it is not valid to assert nRST and nSTBY at the same time.

5.3.1.2DRDY

- DESCRIPTION:

  Data valid for parallel digitized pixel data out.

  The timing of DRDY is controlled by the DSC field of the ICTRL register and by the RPC and DHC fields of the ITMG register.

ICTRL/ITMG FIELD	# bits	meaning
ICTRL[DSC]	2	Number of cycles (0-3) DATA is valid before DRDY is asserted. “00 “ means 0 cycles, “01” means 2 cycles ...
IFTMG[RPC]	3	Number of cycles (1-8) that DRDY is asserted. DATA is also driven during this time. “000” means 1 cycle, “001” means 2 cycles ...
IFTMG[DHC]	2	Number of cycles (0-3) DATA is driven after DRDY is de-asserted. “00” means 0 cycles, “01” means 2 cycles...

Table 43. DRDY and DATA timing control.

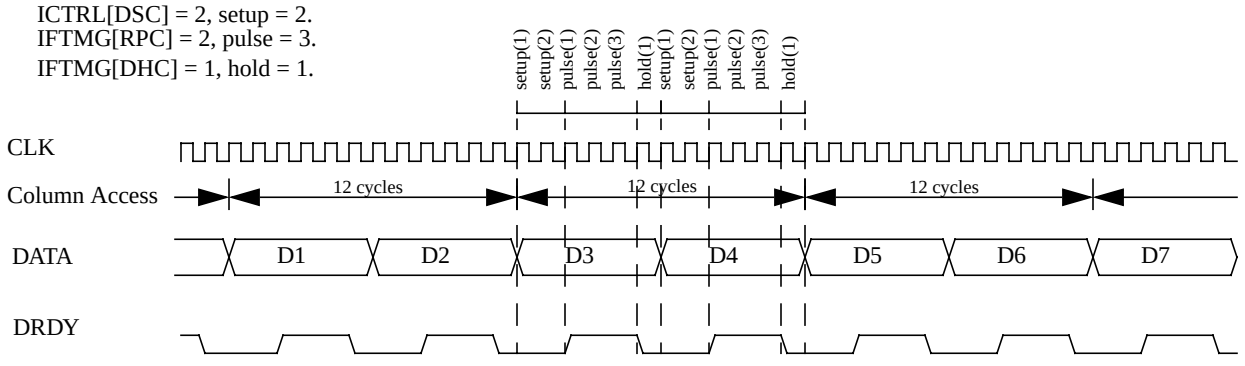


Figure 40. DRDY timing for 12 cycle column access, DSC=2, RPC=2, DHC=1.

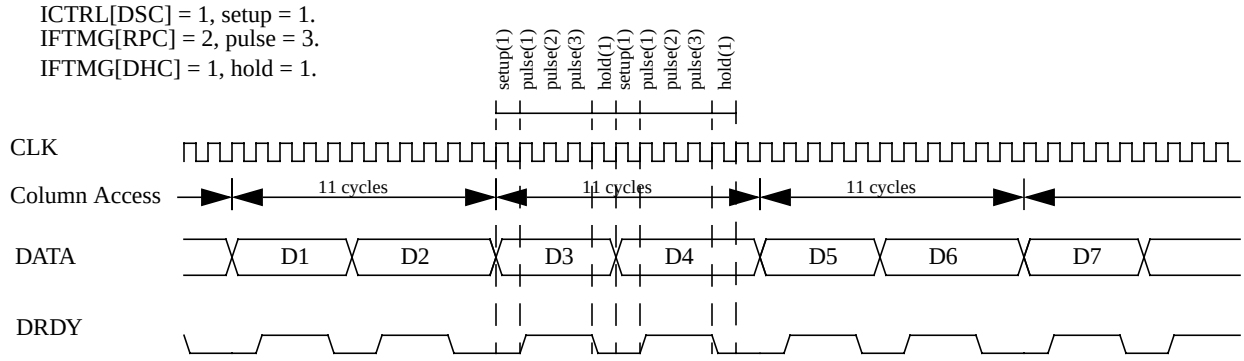


Figure 41. DRDY timing for 11 cycle column access, DSC=1, RPC=2, DHC=1.

The DDO field of the ICTRL register controls the point in the cycle DRDY is driven. If DDO==’0’ DRDY begins driving when CLK makes a rising transition. If DDO==’1’ DRDY begins driving when CLK makes a falling transition.

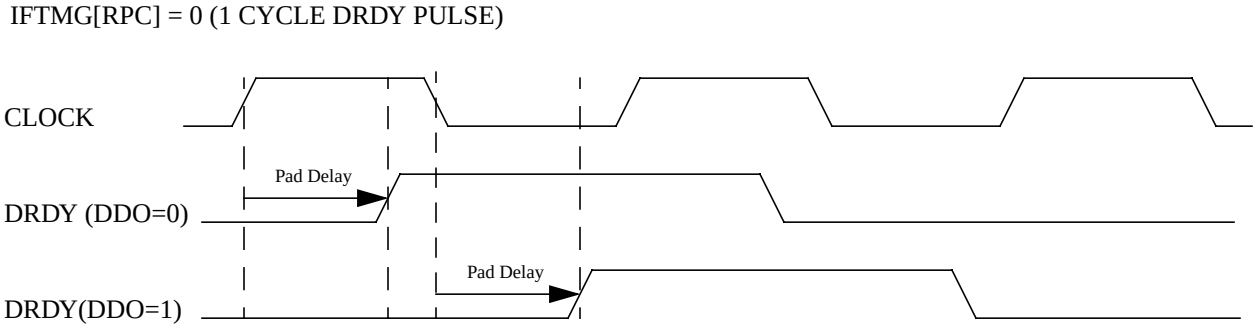


Figure 42. DRDY timing altered by DDO bit of ICTRL register.

When the DPS field of the ITMG register equals ‘0’ DRDY is active high. When DPS equals ‘1’ DRDY is active low.

- CONNECTION INFORMATION:
- PAD CONTROL:

DRDY is controlled by the DOD,DDO, DSC, and HAVG fields of the ICTRL register, and the RPC, DHC, and DPS fields of the ITMG register. The RDYDRV field of the PDRV register controls the switching speed of DRDY.

5.3.1.3DATA9,DATA8,DATA7,...DATA0

- DESCRIPTION:

  Parallel digitized pixel data out.

  The timing of DATA is defined in the DRDY pin description.

  The DOD field of the ICTRL register defines 4 modes of modifying 10 bit output. If the ADCs are programmed to output less than 10 bits, the MSB of the output data is aligned to DATA[9].

DOD value	mode	DATA[9:0]
00	normal	DATA[9:0] = ADC_DATA[9:0];

01	rounding	if (ADC_DATA[9:2]==”1111_1111”)
		ADC_rounded[9:0] = “11_1111_1111”
		else
		ADC_rounded[9:0] = ADC_DATA + “00_0000_0010”;
		DATA[9:2] = ADC_rounded[9:2];
		DATA[1:0] = “00”

10	saturation	if ((ADC_DATA[9] == 1) or (ADC_DATA[8] ==1))
		DATA[9:2] = “1111_1111” ; //saturation
		else DATA[9:2] = ADC_DATA[7:0];
		Data[1:0] = “00”

11	truncated saturation	if (ADC_DATA[9]==1) DATA[9:2] = “1111_1111”; // saturation
		else DATA[9:2] = ADC_DATA[8:1];
		DATA[1:0] = “00”

Table 44. DOD bits of IFCTRL controlling DATA out.

Number of ADC bits	DATA9 (MSB) - DATA0 (LSB)
10	ADC_DATA[9:0]
9	ADC_DATA[9:1], ‘0’
8	ADC_DATA[9:2], ‘00’

Table 45. Data Alignment of ADC output for DOD = ‘00’

When IMODE==”1” and TCLK==”1” the chip is in test_mode, and the function of DATA[5:0] is modified.

The sequencing of data output from the sensor is influenced by the HAVG bit of the ICTRL register and by the CSS bit of the CONFIG register.

Assume Sampling Window from column 12 to column 19. nROW in level mode.

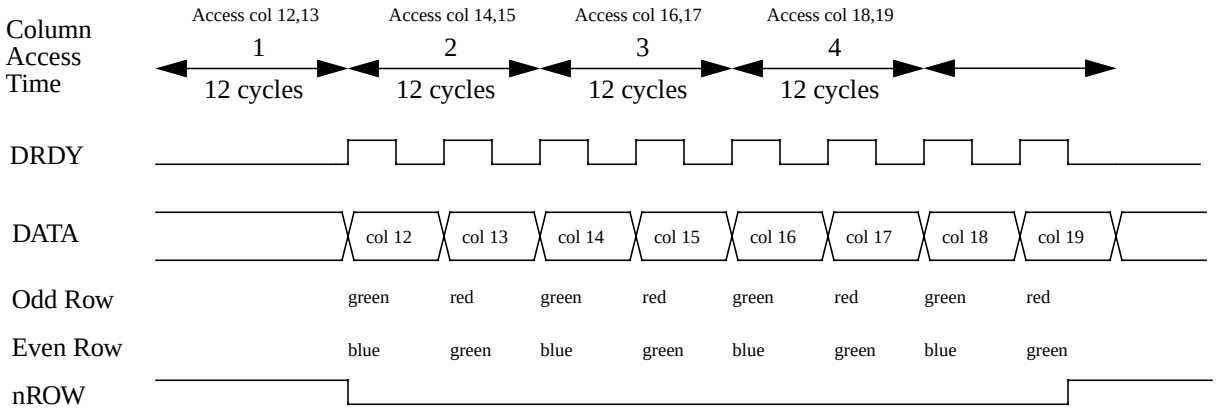


Figure 43. DATA Sequencing: CONFIG[CSS] = ‘0’, ICTRL[HAVG] = ‘0’

Assume Sampling Window from column 12 to column 19. nROW in level mode.

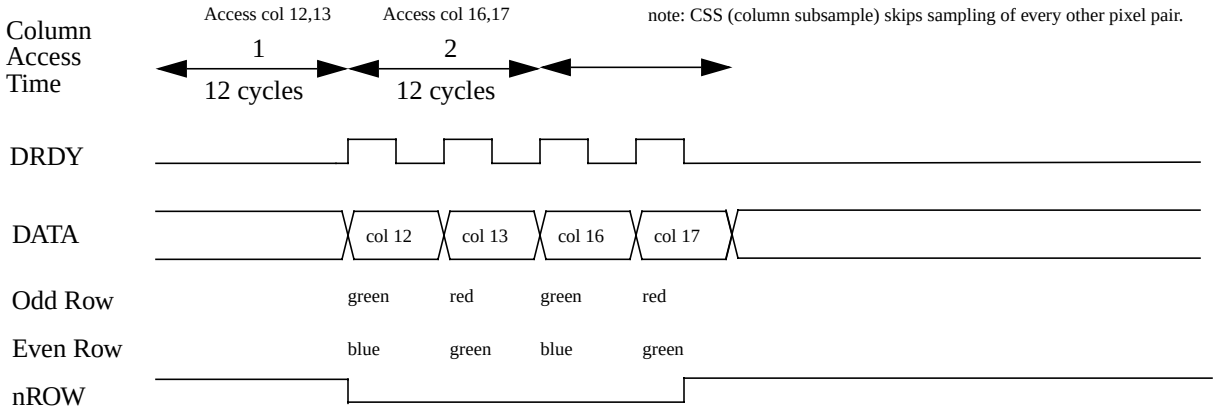


Figure 44. DATA Sequencing: CONFIG[CSS] = ‘1’, ICTRL[HAVG] = ‘0’.

Assume Sampling Window from column 12 to column 19. nROW in level mode.

note: HAVG (horizontal averaging) averages neighbor pixel pairs .

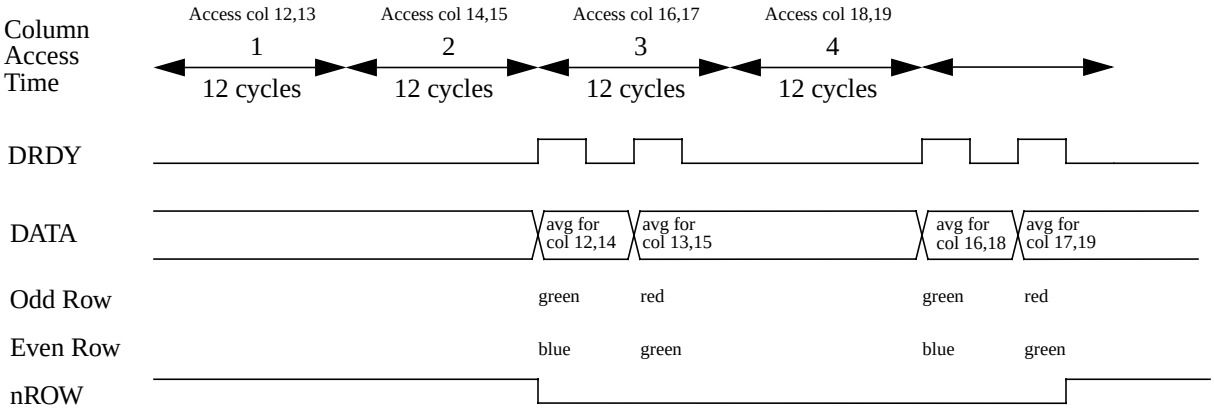


Figure 45. DATA Sequencing: CONFIG[CSS] = ‘0’, ICTRL[HAVG] = ‘1’.

Assume Sampling Window from column 12 to column 19. nROW in level mode.

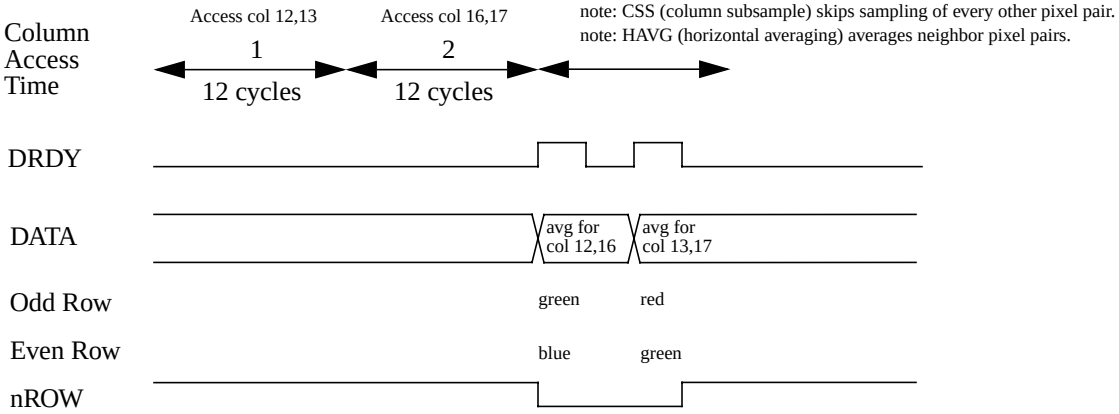


Figure 46. DATA Sequencing: CONFIG[CSS] = ‘1’, ICTRL[HAVG] = ‘1’.

- CONNECTION INFORMATION:

  If operating only in one of the 8 bit modes, do not connect the LSB, DATA[1:0]. The LSB will always be driven to 0 in 8 bit modes.

- PAD CONTROL:

  DATA[9:0] is controlled by the DOD, DDO, DSC, and HAVG fields of the ICTRL register, and by the RPC, DHC, and DPS fields of the ITMG register. The DATDRV field of the PDRV register controls

the switching speed of DATA. When IMODE==”1” and TCLK==”1” the chip is in test_mode and the function of DATA[7:0] is modified as described above.

5.3.1.4IMODE

- DESCRIPTION:

  The IMODE input defines the interface mode. In conduction with TCLK, it also defines test mode.

IMODE/TCLK	Interface Mode Description
IMODE==”0”	Synchronous Serial Slave Mode. • TCLK_nFRAME operates as the TCLK (transfer clock) input. • IMODE[0] operates as a chip select.
IMODE==”1” and TCLK==”0”	Half Duplex UART Slave Mode. • TCLK_nFRAME operates as the nFRAME output flag.
IMODE==”1” and TCLK==”1”	Test Mode. • DATA pin function changed.

Table 46. Interface Modes

- CONNECTION INFORMATION:

  IMODE should be tied high for half duplex UART slave mode, or tied low for Synchronous Serial mode. TCLK should be tied low for UART mode. Synchronous Serial interface, or connected to a positive active chip select for a multi-point interface.

- PAD CONTROL:

  IMODE modifies the function of DATA[7:0], TCLK_nFRAME, RxD and TxD.

5.3.1.5TCLK

- DESCRIPTION:

  The TCLK input is the transfer clock for Synchronous Serial Mode. See the System Interface section for more details.

- CONNECTION INFORMATION:

  TCLK must be tied low in UART mode.

- PAD CONTROL:

  IMODE controls whether TCLK is used as an input for synchronous serial mode, or needs to be tied low for UART mode.

5.3.1.6TxD

- DESCRIPTION:

  TxD is the serial output data. The default value is ‘1’. Since The HDCS sensor is a slave only device, TxD will only switch in response to a serial read command received on RxD. If IMODE==’1’ TxD follows the UART protocol, if IMODE==’0’ TxD follows the Synchronous Serial protocol.

- CONNECTION INFORMATION:
- PAD CONTROL:

IMODE controls if TxD is in UART mode or Synchronous Serial mode. The TXDDRV field of the PDRV register controls the switching speed of TxD.

5.3.1.7RxD

- DESCRIPTION:

  RxD is the serial data input. If IMODE==’1’ RxD follows the UART protocol. If IMODE==’0’ RxD follows the Synchronous Serial protocol.

- CONNECTION INFORMATION:
- PAD CONTROL:

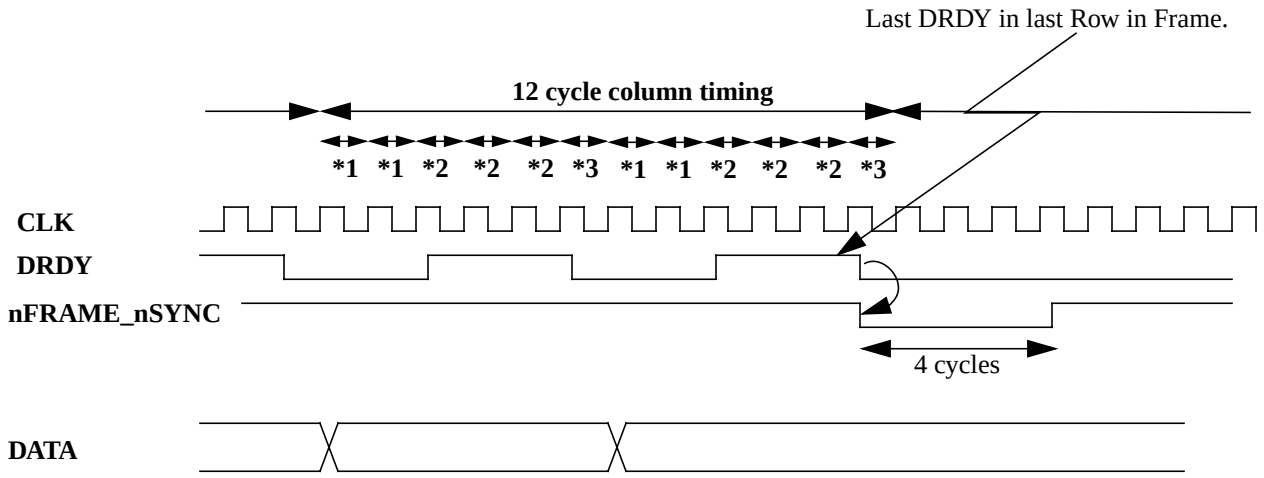
  If IMODE]==’1’ RxD follows the UART protocol. If IMODE==’0’ RxD follows the Synchronous Serial protocol.

5.3.1.8nFRAME_nSYNC

- DESCRIPTION

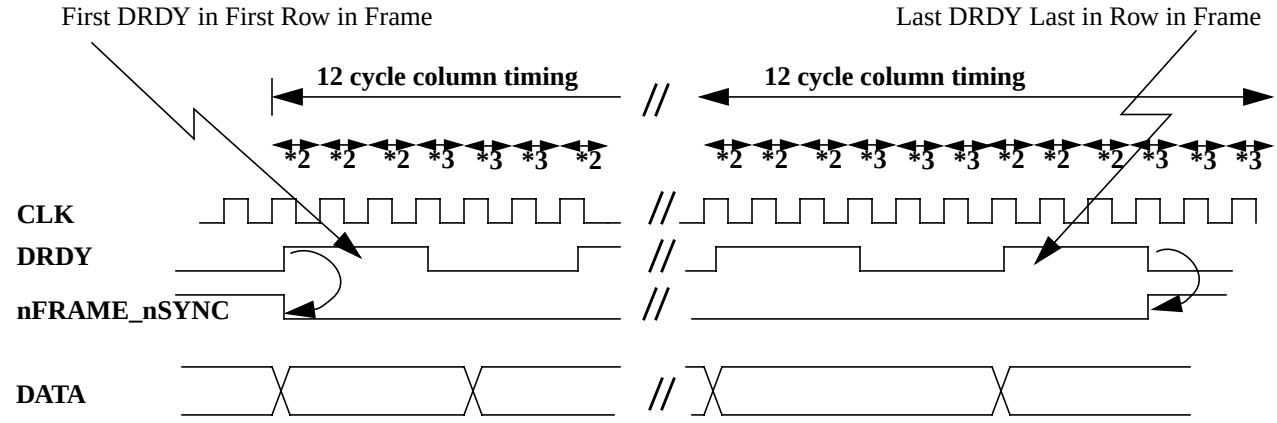
PCTRL[FSE]	PCTRL[FSS]	PCTRL[LVF]	Mode: Notes
‘0’	‘x’	‘x’	nFRAME_nSYNC is disabled. Drives a constant ‘1’.
‘1’	‘1’	‘0’	nSYNC Pulse Mode. Assert 4 cycle active low pulse at the start of integration.
‘1’	‘1’	‘1’	nSYNC Level Mode. Assert low at start of integration. De-assert when first data is transferred.
‘1’	‘0’	‘0’	nFRAME Pulse Mode. Assert low for 4 cycles after the last data for a frame is transferred. If CONFIG[SFC] (stop when frame complete) equals ‘0’, if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current frame, then nFRAME is asserted low for 4 cycles.
‘1’	‘0’	‘1’	nFRAME Level Mode. Assert low when first data for a frame is transferred. De-assert after last data for a frame is transferred. If CONFIG[SFC] (stop when frame complete) equals ‘0, nFRAME is de-asserted when CONTROL[RUN] is de-asserted.

Table 47. nFRAME_nSYNC Status Flag Control



*1 : ICTRL[DSC] = 2 (2 cycle) *2: IFTMG[RPC] = 2 (3 cycles) *3: IFTMG[DHC] = 1 (1 cycle)

Figure 47. nFRAME_nSYNC Timing in nFRAME Pulse Mode



*1 : ICTRL[DSC] = 0 (0 cycle) *2: IFTMG[RPC] = 2 (3 cycles) *3: IFTMG[DHC] = 3 (3 cycle)

Figure 48. nFRAME_nSYNC Timing in nFRAME Level Mode

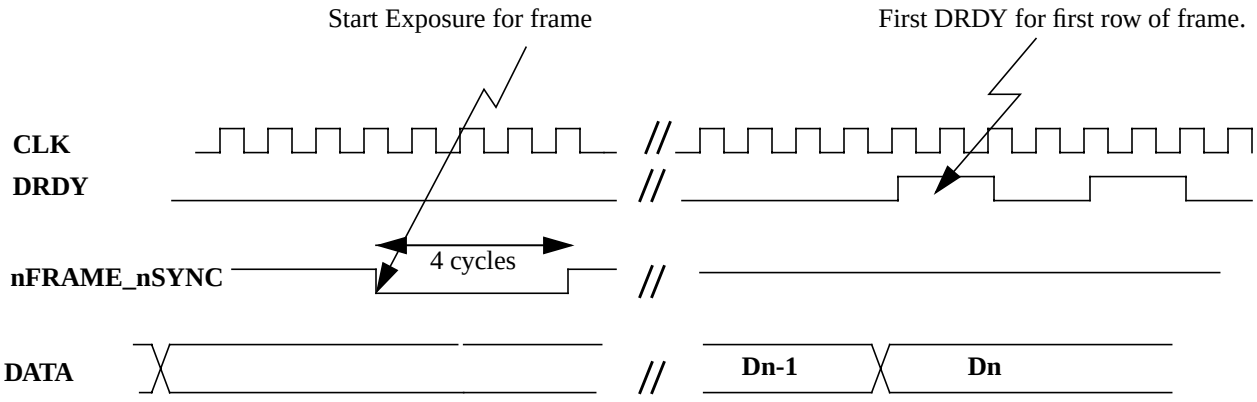


Figure 49. nFRAME_nSYNC Timing in Shutter Sync Pulse Mode

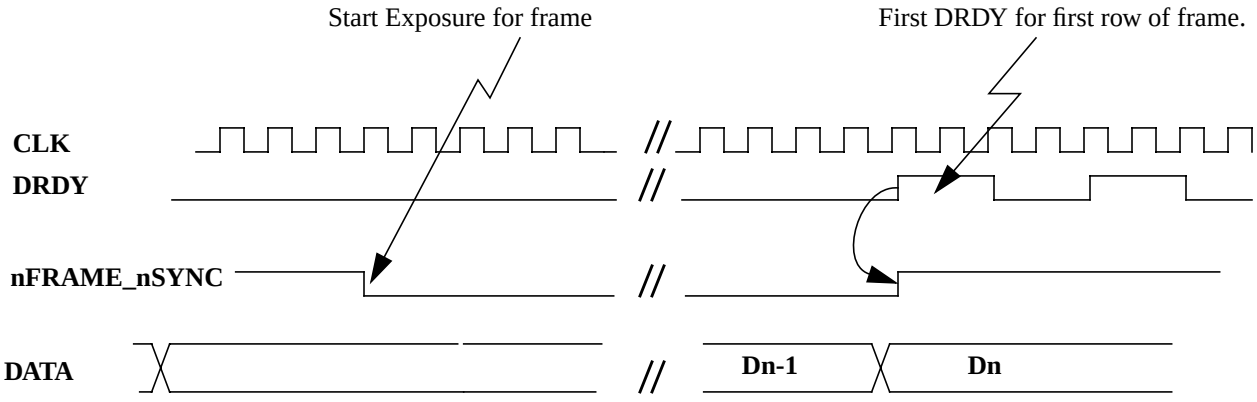
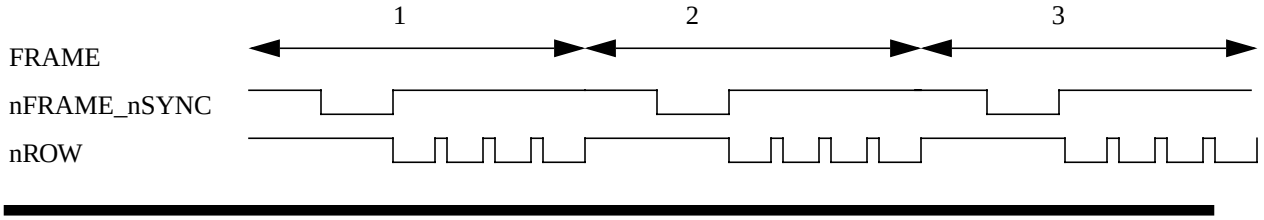
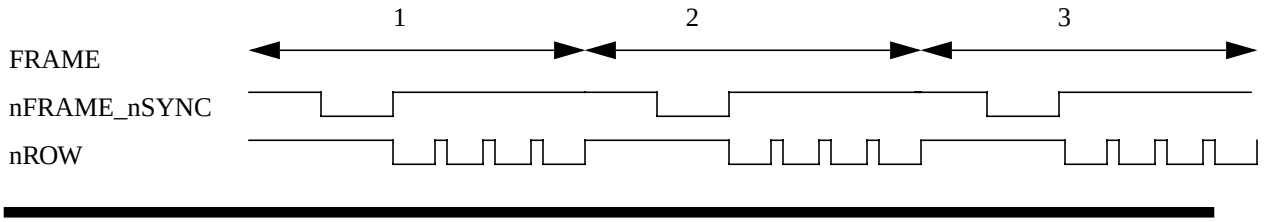


Figure 50. nFRAME_nSYNC Timing in Shutter Sync Level Mode

nROW in Level Mode, nFRAME_nSYNC in Shutter Sync Level Mode.
The sensor in Mechanical Shutter Mode with Continuous Frame Capture.



nROW in Level Mode, nFRAME_nSYNC in Shutter Sync Level Mode.
The HDCS sensor in Normal Mode with Continuous Frame Capture and integration time greater than time to cycle through a frame,



nROW in Level Mode, nFRAME_nSYNC in Shutter Sync Level Mode.
The HDCS sensor in Normal Mode with Continuous Frame Capture and integration time less than time to cycle through a frame,

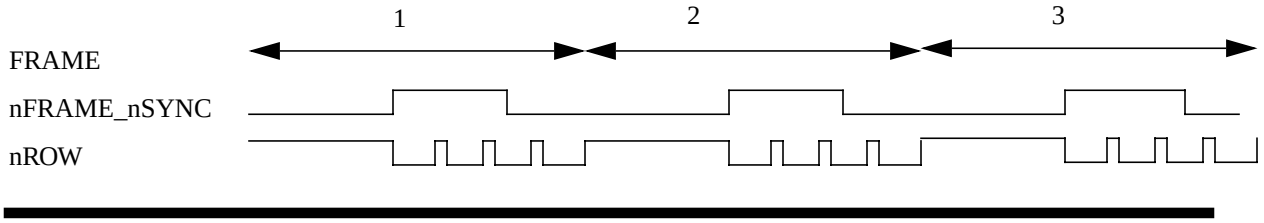


Figure 51. nFRAME_nSYNC in different operation modes.

- CONNECTION INFORMATION:

  If nFRAME_nSYNC is unused, then do not connect it.

- PAD CONTROL:

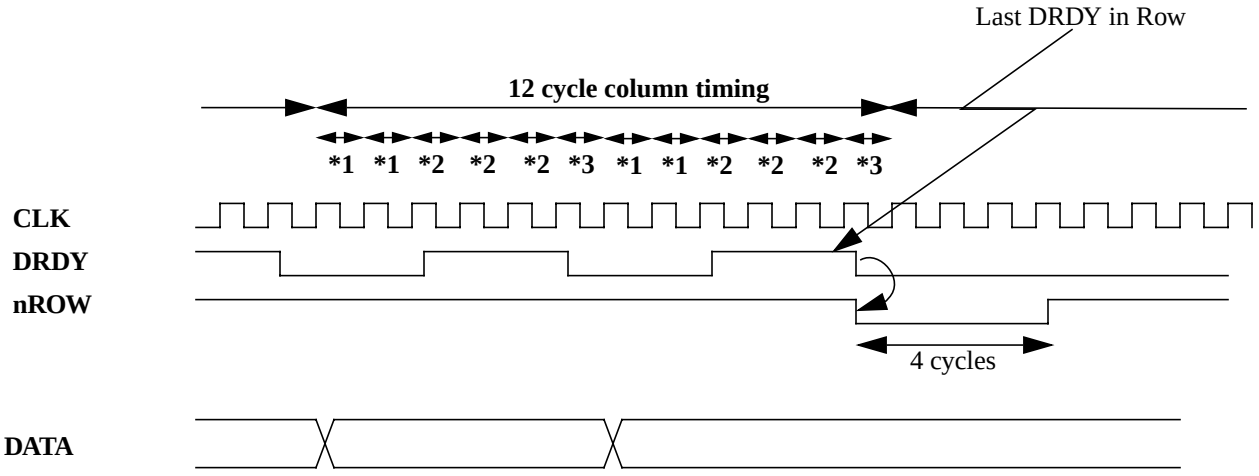
  The STATDRV field of the PDRV register controls the switching speed, and FSE field of the PCTRL register enables switching. The FSS field of the PCTRL register selects end of frame mode or shutter sync mode. The LVF field of the PCTRL register selects if nFRAME_nSYNC functions as a level or a pulse.

5.3.1.9nROW

- DESCRIPTION:

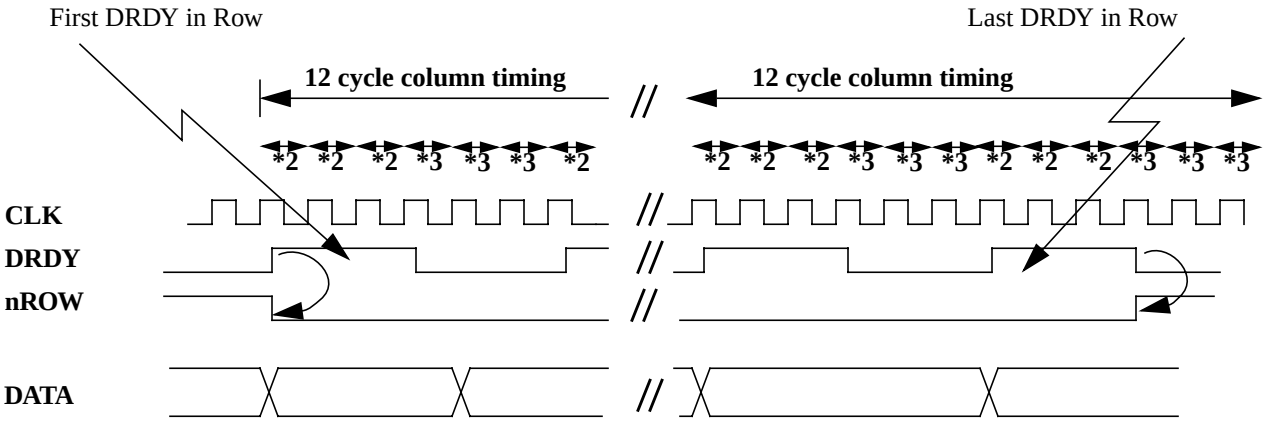
PCTRL[RCE]	PCTRL[LVR]	Mode: Notes
'0'	'x'	nROW Disabled. Drives a constant '1'.
'1'	'0'	nROW pulse mode. Assert low for 4 cycles after last data for a sensor row is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current row, then nROW is asserted low for 4 cycles.
'1'	'1'	nROW level mode. Assert low when first data is transferred for a sensor row. De-assert when last data is transferred for a sensor row. If CONFIG[SFC] (stop when frame complete) equals '0, nROW is de-asserted when CONTROL[RUN] is de-asserted.

Table 48. nROW Status Flag Control



*1 : ICTRL[DSC] = 2 (2 cycle) *2: IFTMG[RPC] = 2 (3 cycles) *3: IFTMG[DHC] = 1 (1 cycle)

Figure 52. nROW Timing in Pulse Mode



*1 : ICTRL[DSC] = 0 (0 cycle) *2: IFTMG[RPC] = 2 (3 cycles) *3: IFTMG[DHC] = 3 (3 cycle)

Figure 53. nROW Timing in Level Mode

- CONNECTION INFORMATION:

  If nROW is unused, then do not connect it.

- PAD CONTROL:

  The STATDRV of the PDRV register controls the switching speed, and the RCE field of the PCTRL register enables switching. The LVR field of the PCTRL register selects if nROW functions as a level or a pulse.

5.3.1.10nIRQ_nCC

- DESCRIPTION:

PCTRL[ICE]	PCTRL[IPD]	PCTRL[LVC]	Mode: Notes
'0'	'0'	'x'	Open Drain IRQ (interrupt request) with weak pull-up. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
'0'	'1'	'x'	IRQ (interrupt request) driving to full high and low levels. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.

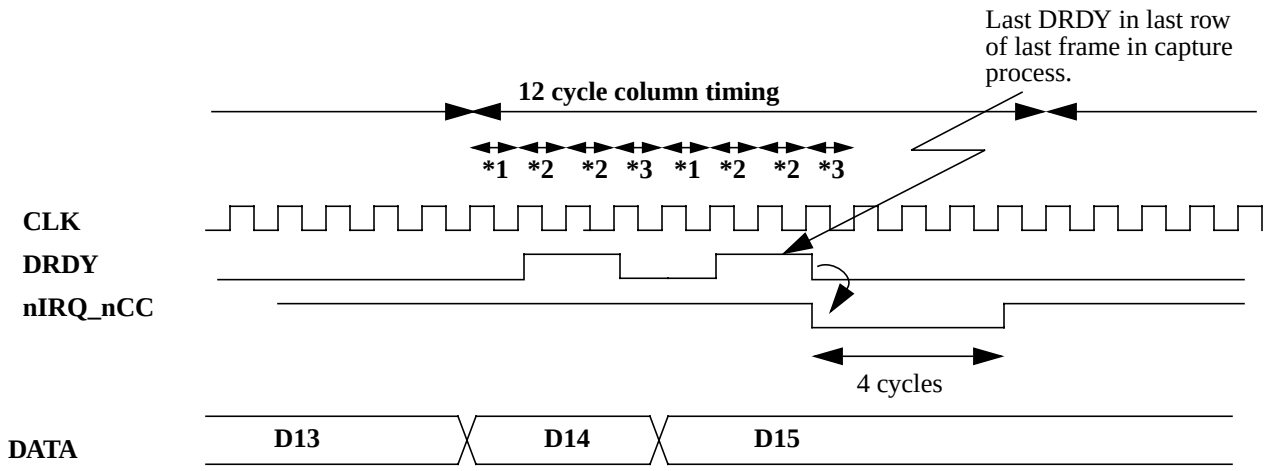
Table 49. nIRQ_nCC Status Flag Control

PCTRL[ICE]	PCTRL[IPD]	PCTRL[LVC]	Mode: Notes
‘1’	‘x’	‘0’	nCC (capture complete) pulse mode. Assert low for 4 cycles when the capture process completes. (After last data from last frame is transferred) If CONFIG[SFC] (stop when frame complete) equals ‘0’, if CONTROL[RUN] is de-asserted, then nCC is asserted low for 4 cycles.
‘1’	‘x’	‘1’	nCC (capture complete) level mode. Assert low when RUN bit is set. De-Assert after capture completes. (After last data for last frame is transferred). If CONFIG[SFC] (stop when frame complete) equals ‘0, nCC is de-asserted when CONTROL[RUN] is de-asserted.

Table 49. nIRQ_nCC Status Flag Control

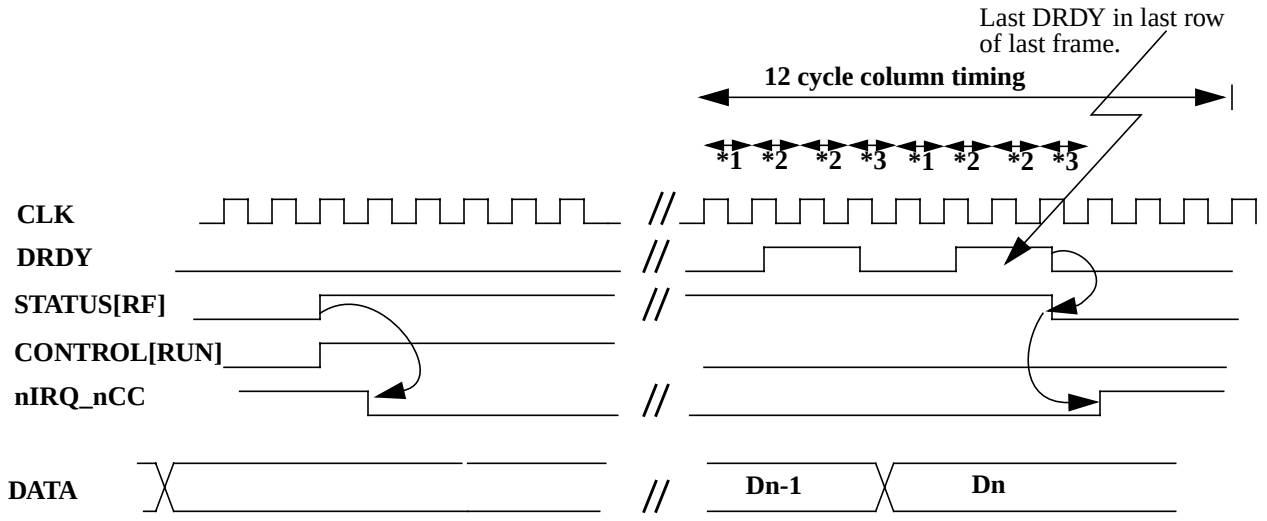
CONFIG[CFC] continuous frame capture	CONFIG[SFC] stop when frame complete	Capture Complete when...
‘0’	‘0’	At end of the first frame if CONTROL[RUN] is not de-asserted. Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode
‘0’	‘1’	After last data is transferred for first frame.is de-asserted in.
‘1’	‘0’	Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode
‘1’	‘1’	After last data is transferred for frame that CONTROL[RUN] is de-asserted in.

Table 50. Capture Complete Definition



*1 : ICTRL[DSC] = 1 (1 cycle) *2: IFTMG[RPC] = 1 (2 cycles) *3: IFTMG[DHC] = 1 (1 cycle)

Figure 54. nIRQ_nCC Timing in Capture Complete Pulse Mode



*1 : ICTRL[DSC] = 1 (1 cycle) *2: IFTMG[RPC] = 1 (2 cycles) *3: IFTMG[DHC] = 1 (1 cycle)

Figure 55. nIRQ_nCC Timing in Capture Complete Level Mode

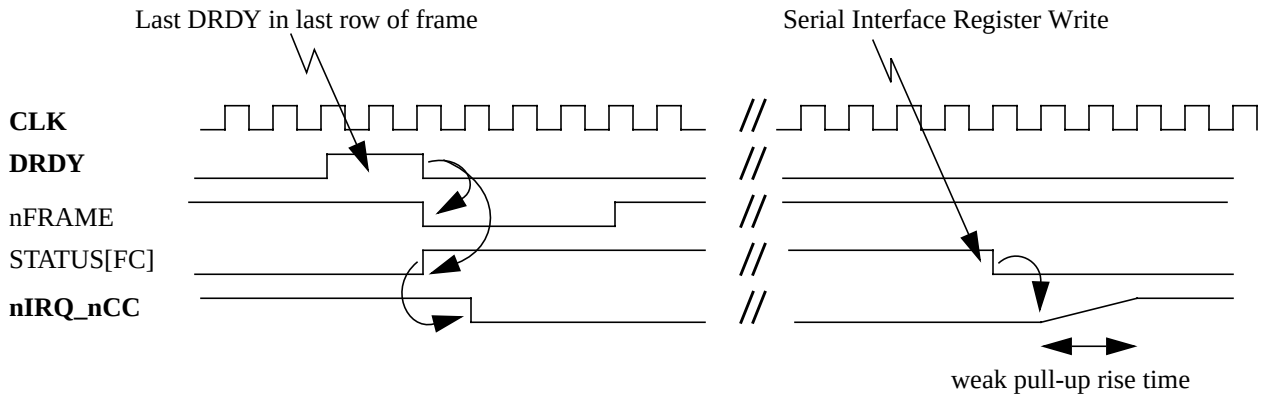


Figure 56. nIRQ_nCC Timing in Interrupt Request Mode with Open Drain. (interrupt on end of frame)

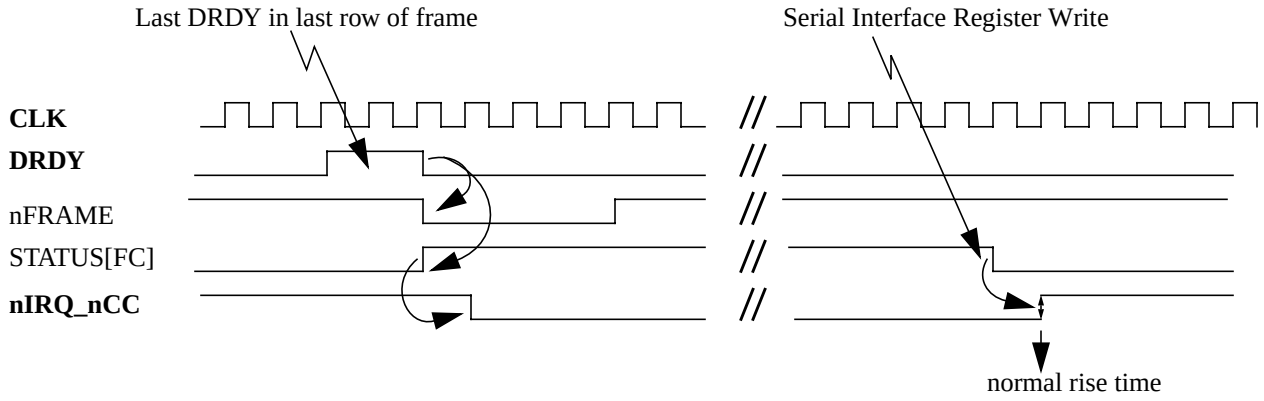


Figure 57. nIRQ_nCC Timing in Interrupt Request Mode without Open Drain. (interrupt on end of frame)

- CONNECTION INFORMATION:

  If nIRQ_nCC is unused, do not connect this pin.

- PAD CONTROL:

  The ICE field of the PCTRL register selects whether nIRQ_nCC functions as nIRQ or nCC. When functioning as nIRQ, the IPD field of the PCRTL register disables the weak internal pull up. When functioning as nIRQ, the IMASK register enables the events that cause nIRQ to assert low. The STATUS (interrupt status) register identifies the reason nIRQ was driven low. The STATDRV field of the PDRV register sets the switching speed for nIRQ_nCC. When ICE equals ‘1’, the LVC field of the PCTRL register selects if nIRQ_nCC acts as a level or a pulse.

5.3.1.11CLK

- DESCRIPTION:

  System Clock. The maximum frequency is 25 MHz. The frame rate is related to frequency of CLK. See the Reset and Low Power section for more details.

- CONNECTION INFORMATION:

  CLK must be connected for proper operation.

- PAD CONTROL:

  As a low power feature CLK can be internally disabled by asserting nSTBY. The system will be in the reset state when nSTBY is de-asserted. The SLP bit of the CONFIG register also causes partial internal clock gating. The serial interface clocks are not disabled to allow turning SLP bit off. The system registers maintain their value while SLP is asserted, unless the RST bit of the CONFIG register is also asserted. See the Reset and Low Power section for more details.

5.3.1.12nRST

- DESCRIPTION:

  Active low system reset input. See the Reset and Low Power section for more details.

- CONNECTION INFORMATION:

  nRST must be connected.

- PAD CONTROL:

  When nRST and nSTBY are asserted at the same time all outputs are tri-stated.

5.3.1.13nSTBY

- DESCRIPTION:

  Active low stand-by mode input. Asserting nSTBY gates the system clock to save power. nSTBY also causes a system reset with the exception of the 3 flipflops that synchronize the clock. See the Reset and Low Power section for more details.

- CONNECTION INFORMATION:

  nSTBY must be connected.

- PAD CONTROL:

  When nRST and nSTBY are asserted at the same time all outputs are tri-stated.

5.3.1.14 VDD

- DESCRIPTION:

  Digital Power Supply.

5.3.1.15 GND

- DESCRIPTION:

  Digital Ground.

5.3.1.16 AVDD

- DESCRIPTION:

  Analog Power Supply.

5.3.1.17 AGND

- DESCRIPTION:

  Analog, Array, and Substrate Ground.

5.3.1.18 PVDD

- DESCRIPTION:

  Array Power Supply.

5.4 Serial Interface

The serial interface has two modes of operation: 1) Synchronous Serial Slave Mode, and 2) UART Half-Duplex Slave Mode. When IMODE equals “0” the serial interface operates in Synchronous Serial Slave Mode. When IMODE equals “1” and TCLK equals “0” the serial interface operates in UART Half-Duplex Slave Mode.

The HDCS sensors function only as slaves, they do not initiate transfers.

5.4.1 Synchronous Serial Slave Mode

Synchronous Serial Slave mode uses 3 pins: RxD (receive serial data), TxD (transmit serial data), TCLK (transfer clock). TCLK and RxD are driven by the master. TxD is driven by the slave (The HDCS sensor).

The TCLK signal synchronizes the serial transmission of each data bit. A data bit on RxD or TxD is valid and stable when TCLK is high. The minimum timing for TCLK is: high at least 4 CLK cycles, and low for at least 4 CLK cycles. The frequency of TCLK may vary throughout at transfer as long as its timing is greater than the minimum timing. Transitions for data bits on TxD and RxD occur when TCLK is low. If RxD transitions while TCLK is high it is interpreted as a START condition or a STOP condition. A START condition occurs when RxD falls while TCLK is high. A STOP condition occurs when RxD rises while TCLK is high.

The default state for RxD and TxD is ‘1’. TxD transitions are triggered by TCLK falling. RxD is sampled when TCLK rises.

Information is transmitted in 9 bit packets which consist of 8 data bits followed by an ACK (acknowledge). There are two types of packet transmissions, master driven packets and slave driven packets. In a master driven packet the master drives 8 data bits and the slave follows with one ACK. If the slave does not issue an ACK it is an error condition. In a slave driven packet the slave drives 8 data bits followed by an ACK from the master. If the master does not issue an ACK the transfer terminates.

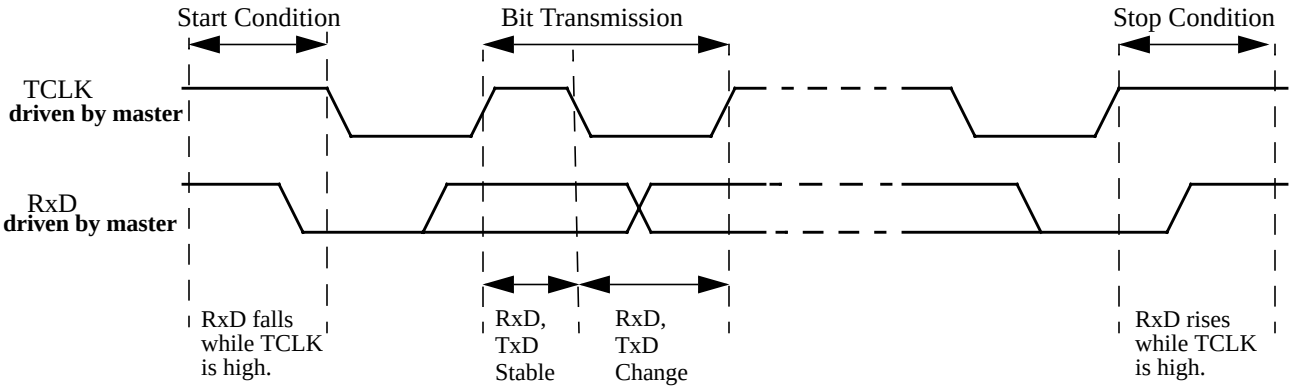


Figure 58. Synchronous Serial Bit Timing

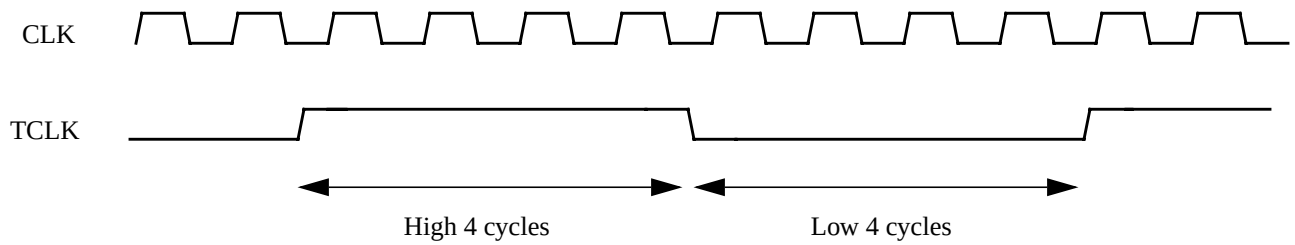


Figure 59. Minimum Timing for TCLK

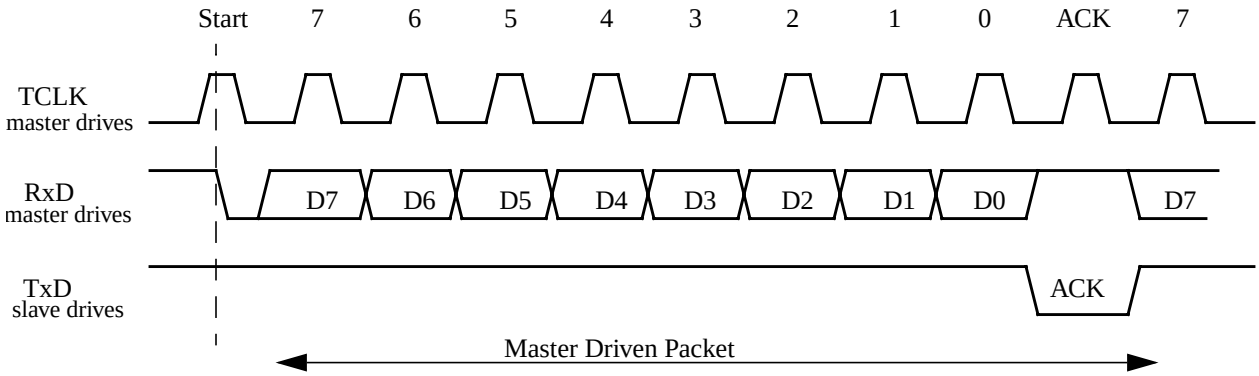


Figure 60. Acknowledge for Master Driven Packet

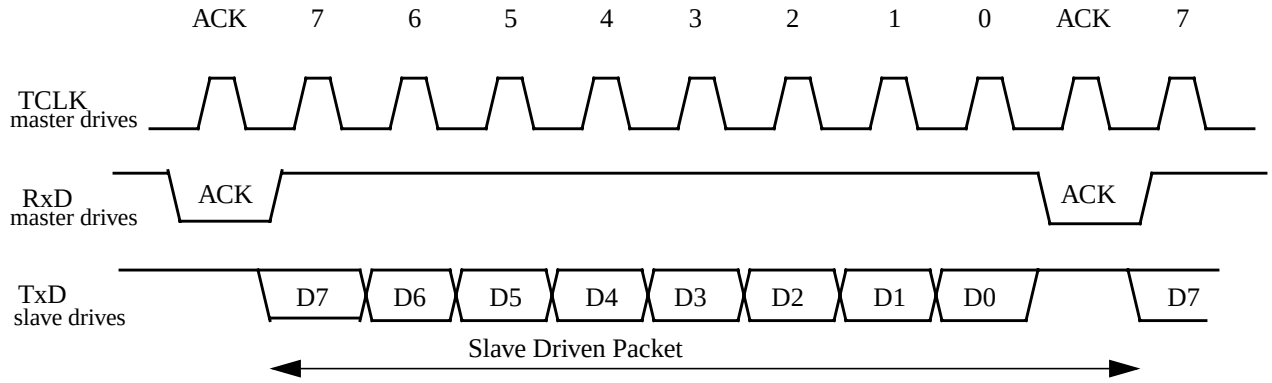


Figure 61. Acknowledge for Slave Driven Packet

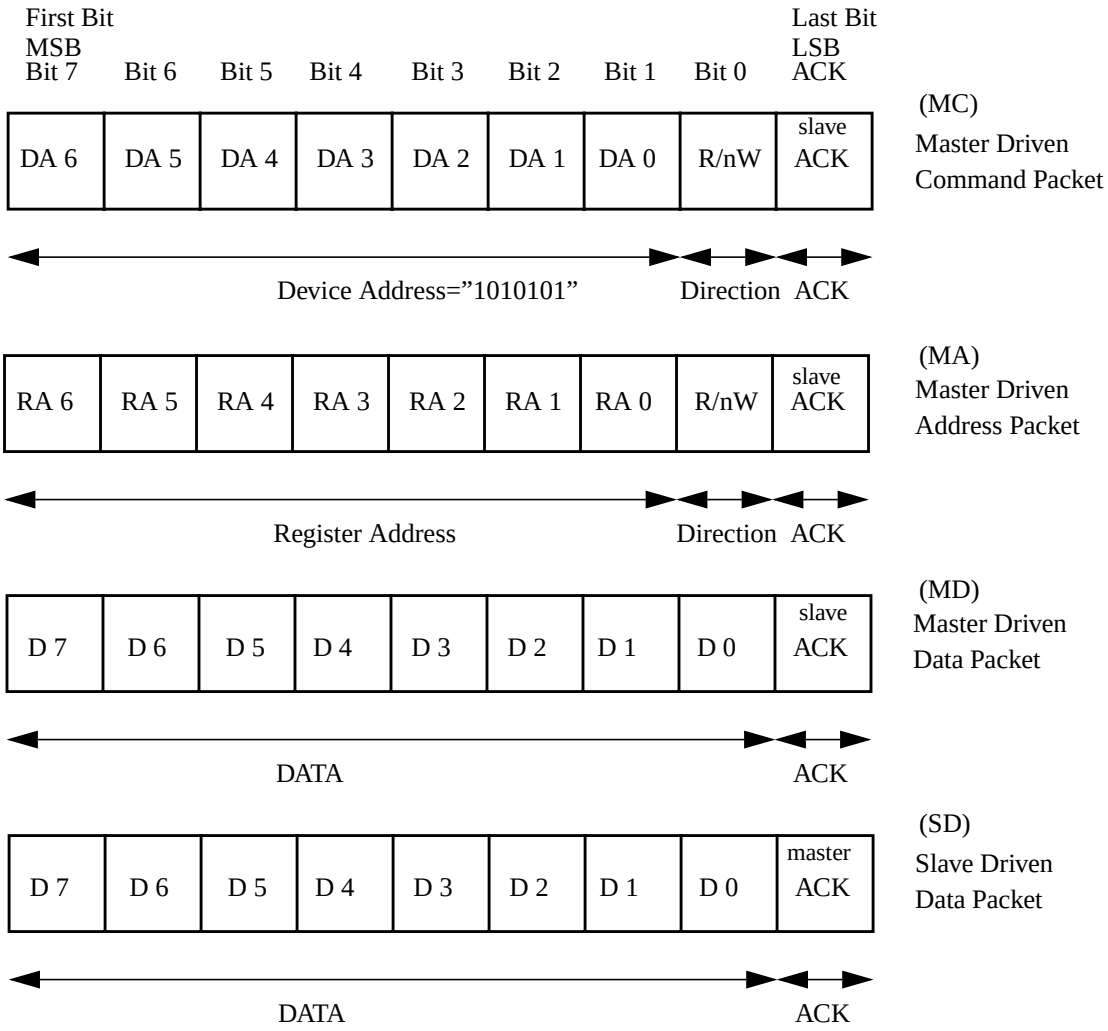


Figure 62. Synchronous Serial Packet Formats

The serial communication sequence is initiated when the master issues a START condition. The transfer terminates at any point where the master issues a STOP condition, or another START condition, or where the master fails to ACK. A failure to ACK by the master is called a NACK.

The DAD (device address disable) and AAD (automatic address increment disable) bits of the ICTRL register alter the behavior of a serial communication sequence. The DAD bit eliminates the requirement for the MC (master driven command) packet which contains the device address. This is intended for point to point control interfaces. When AAD equals of the register address automatically increments after each MD (master driven data) packet and each SD (slave driven

data) packet. When AAD equals ‘1’the register address does not increment after SD and MD packets. This is intended for register polling.

Packet Number		1	2	3	4	5	6	
Packet Type		MC	MA	MD	MD	MD	MC	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
RxD (master)	start	1010_1010_1	0001_1110_1	0001_0010_1	0011_0100_1	0101_0110_1	0111_1000_1	stop
TxD (slave)	1	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_0	1
Register Address	x	x	x	x0F	x10	x11	x12	x13

Write 4 registers (addresses x0F, x10, x11, x12) with data (x12, x34, x56, x78).

Figure 63. Serial Synchronous N Byte Write with DAD=0 and AAD=0.

Packet Number		1	2	3	4	5	6		
Packet Type		MC	MA	MC	SD	SD	SD		
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A		
RxD (master)	start	1010_1010_1	0001_1110_1	start	1010_1011_1	1111_1111_0	1111_1111_0	1111_1111_1	stop
TxD (slave)	1	1111_1111_0	1111_1111_0	1	1111_1111_0	0001_0010_1	0011_0100_1	0101_0110_1	1
Register Address	x	x	x	x0F	x0F	x0F	x10	x11	x12

Read 3 registers (addresses x0F, x10, x11) which contain data (x12, x34, x56).

NOTE: When DAD=0 a write sequence is used to set up the read address.

Figure 64. Serial Synchronous N Byte Read with DAD=0 and AAD=0.

Packet Number		1	2	3	4	5	
Packet Type		MA	MD	MD	MD	MD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
RxD (master)	start	0001_1110_1	0001_0010_1	0011_0100_1	0101_0110_1	0111_1000_1	stop
TxD (slave)	1	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_0	1
Register Address	x	x	x0F	x10	x11	x12	x13

Write 4 registers (addresses x0F, x10, x11, x12) with data (x12, x34, x56, x78).

Figure 65. Serial Synchronous N Byte Write with DAD=1 and AAD=0.

Packet Number		1	2	3	4	5	
Packet Type		MA	SD	SD	SD	SD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
RxD (master)	start	0001_1111_1	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_1	stop
TxD (slave)	1	1111_1111_0	0001_0010_1	0011_0100_1	0101_0110_1	0111_1000_1	1
Register Address	x	x	x0F	x10	x11	x12	x13

Read 4 registers (addresses x0F, x10, x11, x12) which contain data (x12, x34, x56, x78).

NOTE: When DAD=1, a seperate command to set up the starting register address is not required.

Figure 66. Serial Synchronous N Byte Read with DAD=1 and AAD=0.

Packet Number		1	2	3	4	5	
Packet Type		MA	SD	SD	SD	SD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
RxD (master)	start	0000_0011_1	1111_1111_0	1111_1111_0	1111_1111_0	1111_1111_1	stop
TxD (slave)	1	1111_1111_0	0000_0011_1	0000_0011_1	0000_0011_1	0000_0011_1	1
Register Address	x	x	x01	x01	x01	x01	x01

Read 1 register 4 times (addresses x01) which contain data (x03).

NOTE: When DAD=1, a seperate command to set up the starting register address is not required.

When AAD=1 the register address does not auto increment. This is useful for register polling.

Figure 67. Serial Synchronous N Byte Read with DAD=1 and AAD=1.

5.4.2 Synchronous Serial Sequence Diagrams

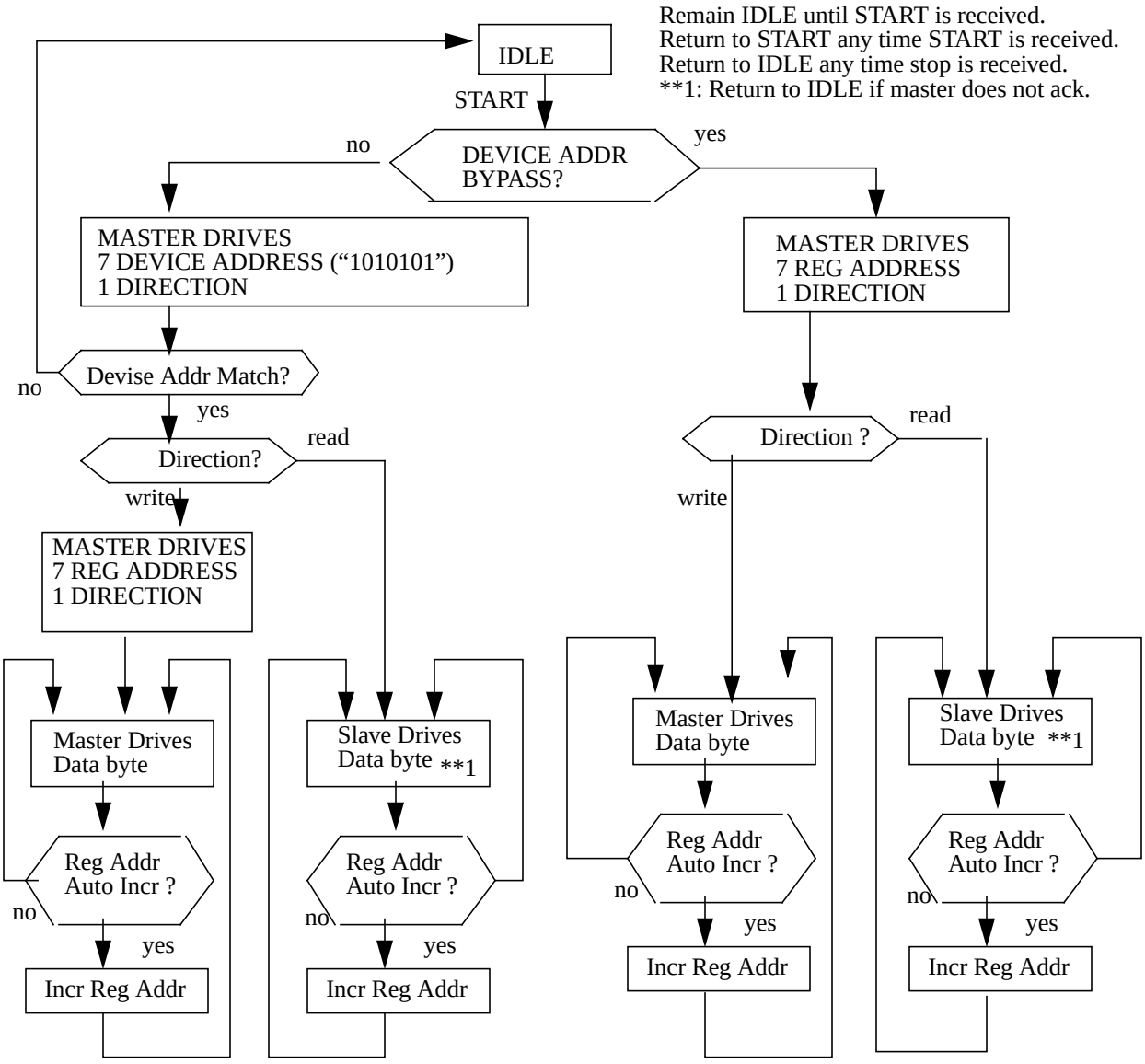


Figure 68. Synchronous Serial byte protocol

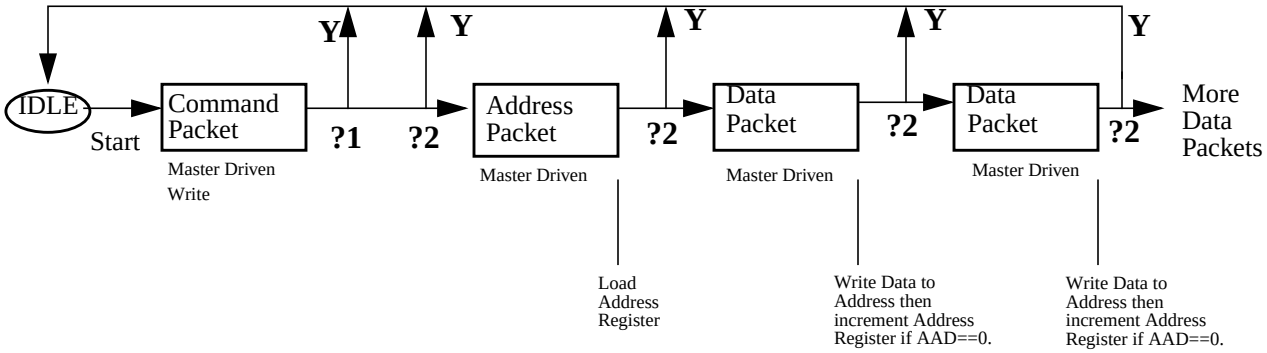


Figure 69. Write Operation Using Device Addr (ICTRL.DAD==’0’)

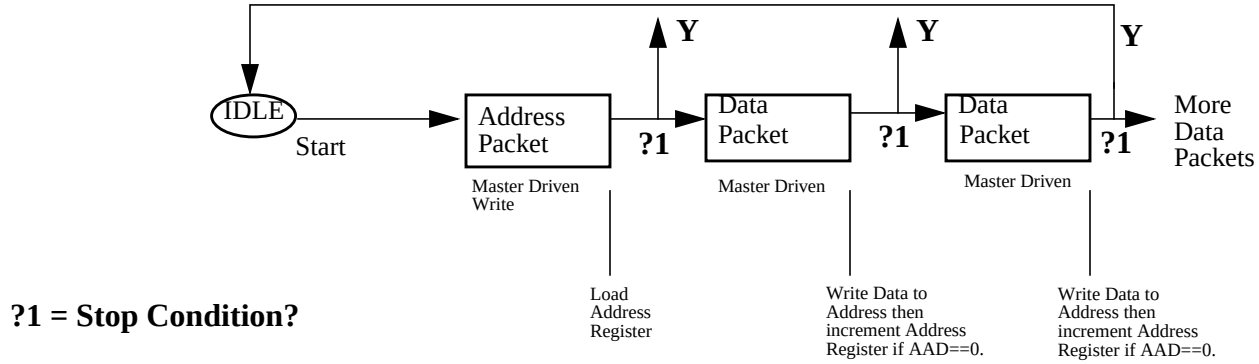


Figure 70. Write Operation Without Device Addr (ICTRL.DAD==’1’)

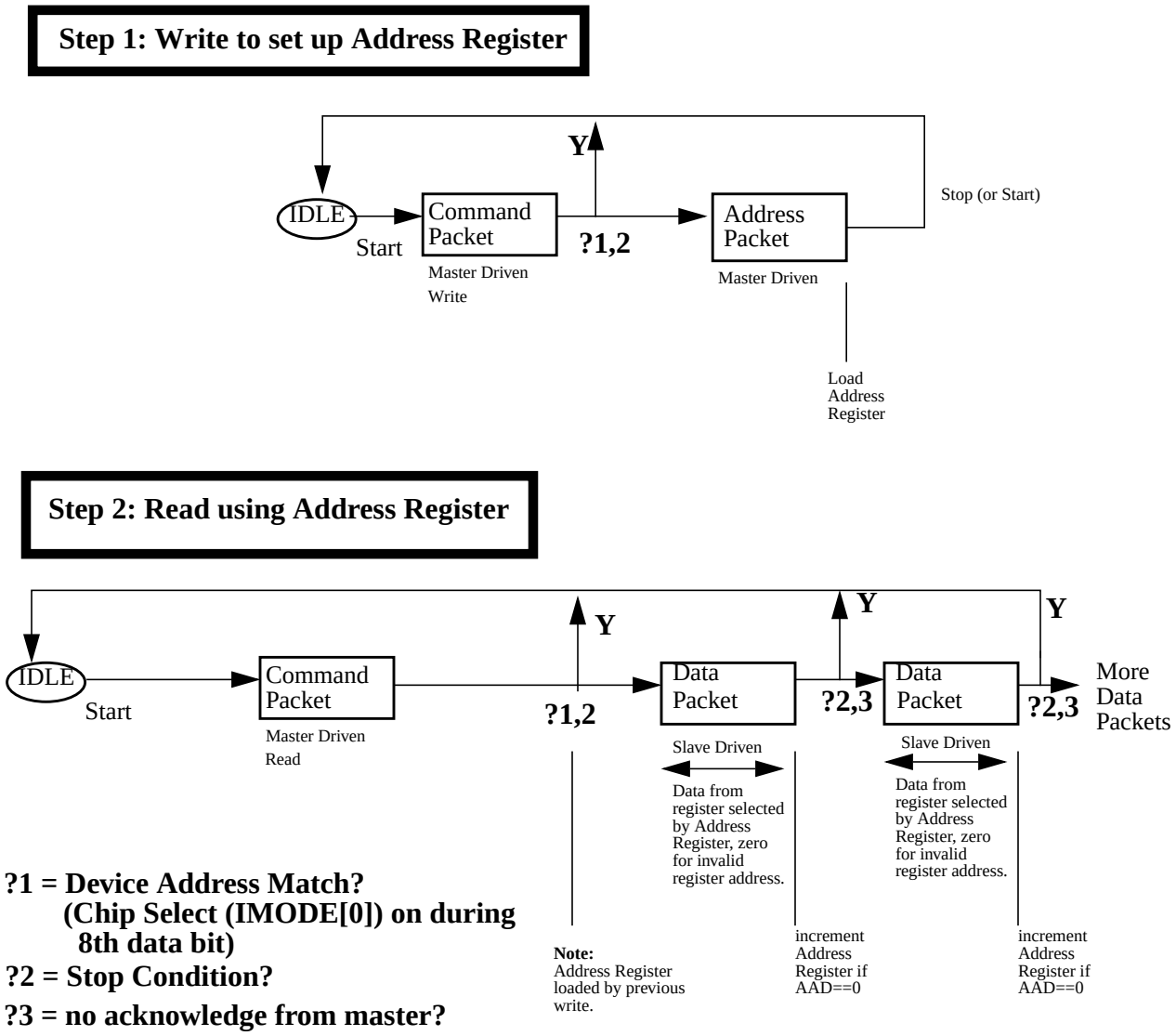


Figure 71. Read Operation Using Device Addr (ICTRL.DAD==’0’)

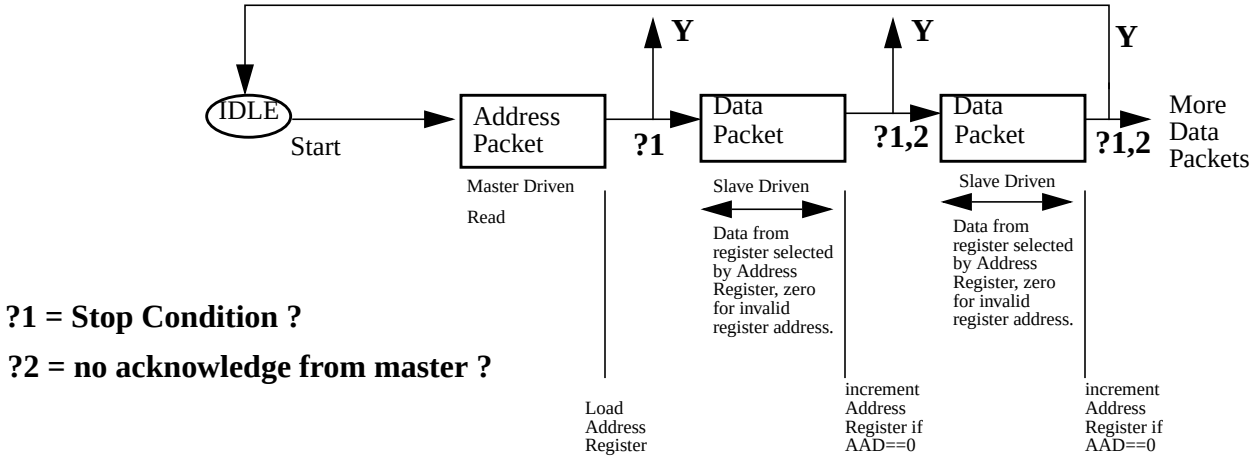


Figure 72. Read Operation Without Device Addr (ICTRL.DAD==’1’)

5.4.3 Serial Interface: UART Half-Duplex Slave Mode.

UART Half-Duplex Slave Mode uses 2 pins: RxD (receive serial data), and TxD (transmit serial data). The RxD pin is driven by the master, and TxD is driven by the slave (The HDCS sensor).

Each serial bit is driven for a fixed time duration called the Bit Time. A Bit Time is 16 roll-overs of the Bit Time Counter. The number of system clocks required to increment the Bit Time Counter is determined by the BRATE and BFRAC registers. The value of a data bit is the majority vote of its value at the beginning of the 7th, 8th, and 9th roll-overs of the Bit Time Counter.

Data is transmitted in 10 bit packets. The first bit of a packet is the start bit. The start bit (‘0’) is followed by 8 data bits. The first data bit is the LSB. The 8 data bits are followed by one stop bit (‘1’).

The default (idle) state of RxD and TxD is ‘1’. When RxD transitions low for the Start Bit, The HDCS sensor synchronizes by resetting its Bit Time Counter and starts the receiving process.

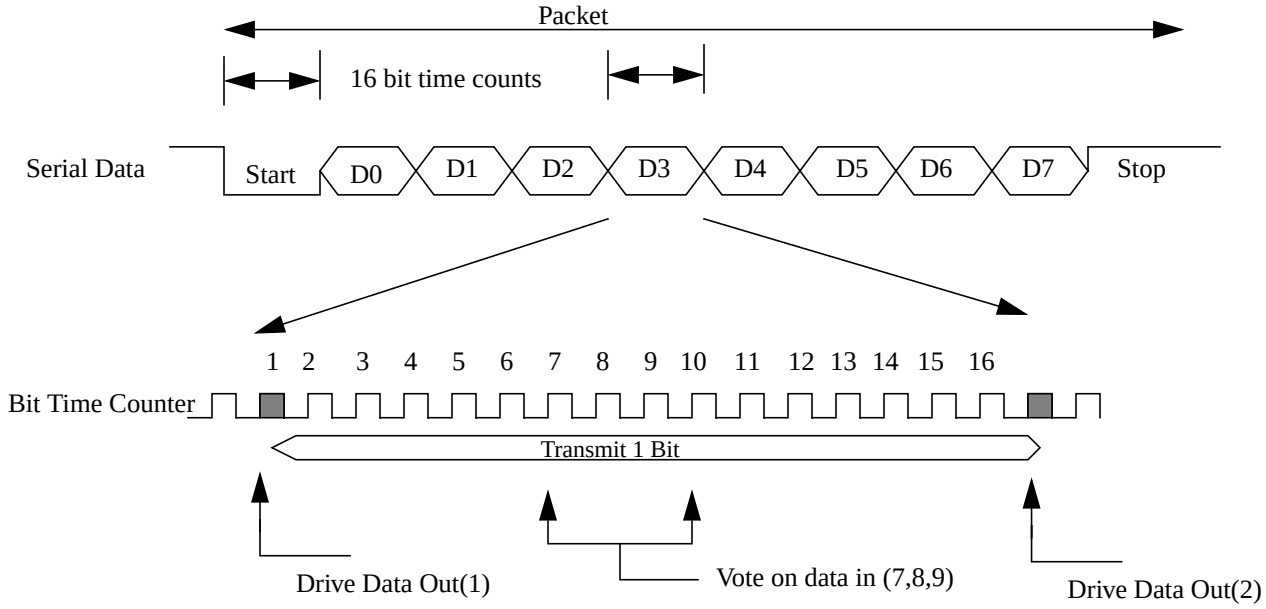


Figure 73. UART Bit Protocol

$$ClocksPerBitTime = (16 \times \{BRATE + 1\}) + (4 \times BFRAC)$$

$$BitTime = ClockPeriod \times ClocksPerBitTime$$

$$BaudRate = (ClockFrequency)/(ClocksPerBitTime)$$

Figure 74. Bit Rate Equations

$$BRATE = 155 \quad BFRAC = 1$$
$$ClockFrequency = 24MHz$$
$$ClockPeriod = \frac{1}{24} \times 10^{-6} = 41.67 \times 10^{-9} nS$$
$$BitTime = 104.17uS = 2500 \times 41.67 \times 10^{-9} nS = 2500 \times \frac{1}{24} \times 10^{-6}$$
$$ClocksPerBitTime = 2500 = (16 \times 156) + (4 \times 1)$$
$$BaudRate = 9600Baud = (24 \times 10^{6})/(2500)$$

Figure 75. Initial Bit Rate Setting

Target Baud Rate	9600	19200	28800	38800	57600	115200
BFRAC [a]	0x9b	0x4d	0x33	0x25	0x19	0x0c
BRATE	0x01	0x00	0x00	0x02	0x00	0x00
%Error of act. BR	0.00	0.16	0.16	0.41	0.15	0.15
1 Byte Min Baud [b]	9056	18113	27272	36923	54545	109090
1 Byte Max Baud	10105	20253	30379	41025	60759	121827
1 Byte %Err Min	6.00	6.00	5.00	5.00	5.00	5.00
1 Byte %Err Max	5.00	5.00	5.00	5.00	5.00	5.00
8 Byte Min Baud[c]	9056	18113	27272	36923	54545	109090
8 Byte Max Baud	9669	19370	29055	39215	58111	115942
8 Byte %Err Min	6.00	6.00	5.00	5.00	5.00	5.00
8 Byte %Err Max	0.72	0.88	0.88	1.06	0.88	0.64
# Cycles/Bit ideal	2500	1250	833.33	618.56	416.67	208.33
# Cycles/Bit actual	2500	1248	832	616	416	208

Table 51. UART Characterization data with 24 Mhz Clock

a. Value to set the BFRAC and BRATE Registers to obtain desired baud rate

b. Acceptable baud min/max range for given BFRAC/BRATE settings. Transmitting 1 byte.

c. These values for transmitting 8 bytes with no delay between bytes. Error accumilates for 8 byte transmission without delay between bytes if master is running faster than the HDCS Sensor.

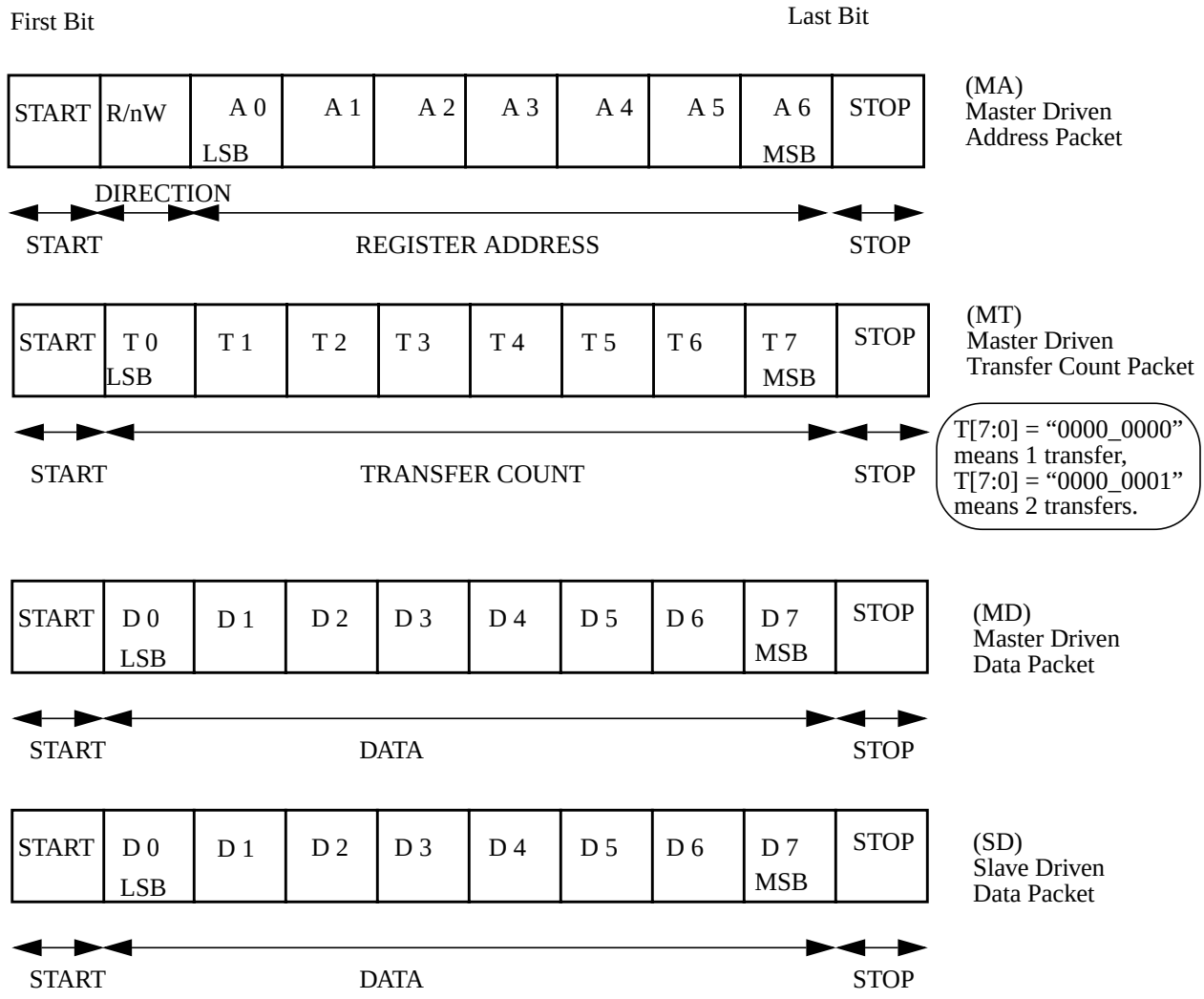
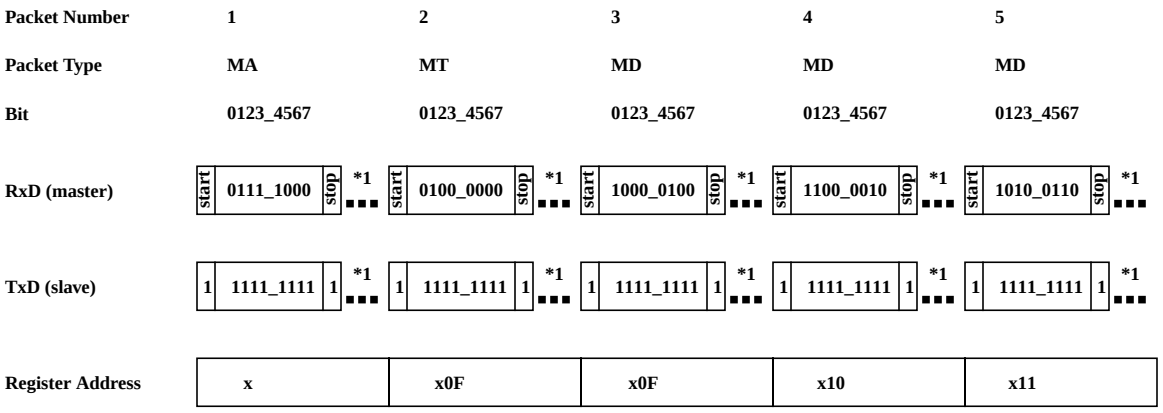


Figure 76. UART Packet Formats

The serial communication sequence is initiated when the master transmits a start bit on RxD. The master transmits the first 2 packets. The first packet (MA) indicates the starting register address and whether it is a read or a write sequence. The second packet (MT) indicates the number of bytes to be transferred. For a write sequence the master transmits the number of data packets (MD) on RxD equal to the transfer count. For a read sequence the slave transmits the number of data packets (SD) on TxD equal to the transfer count.

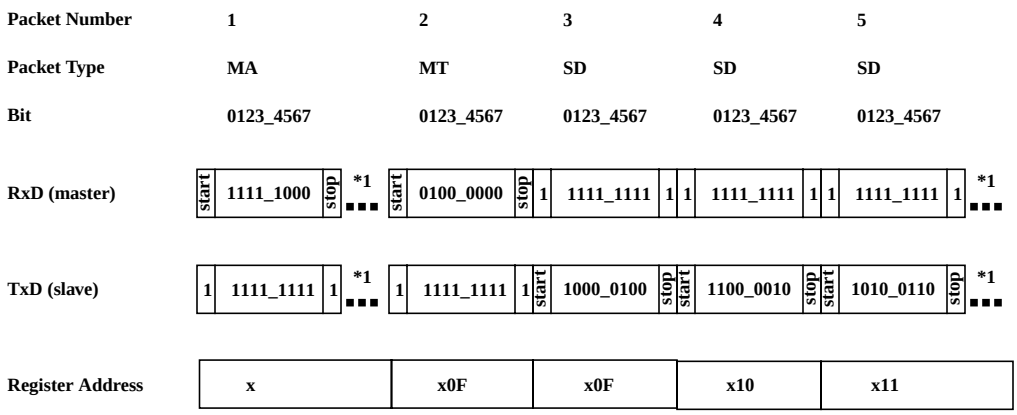
The AAD (automatic address increment disable) bit of the ICTRL register alters the behavior of the serial communication sequence. When AAD equals '0', the register address is automatically incremented after each MD or SD packet. When AAD equals '1', the register address does not increment after MD or SD packets. This is intended for use in register polling.



*1: Repeat N cycles (N>=0) of RxD = '1' and TxD = '1'.

Write 3 registers (addresses x0F, x10, x11) with data (x21, x34, x65).

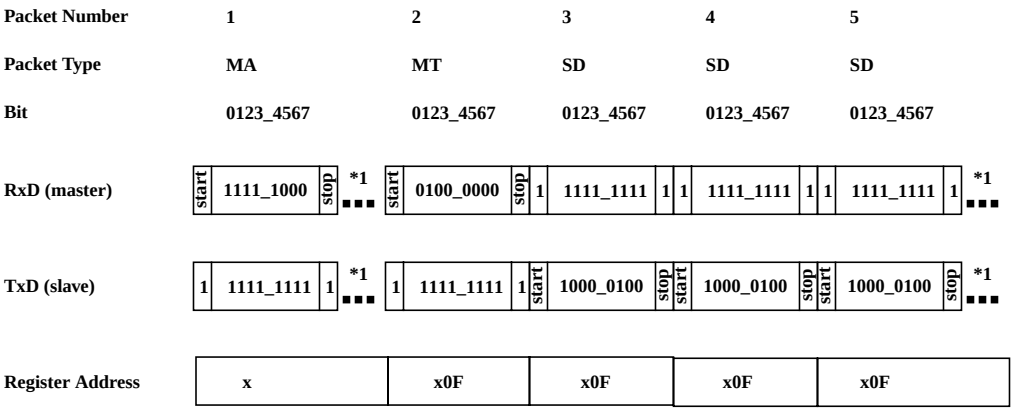
Figure 77. UART N Byte Write with AAD=0



*1: Repeat N cycles (N>=0) of RxD = '1' and TxD = '1'.

Read 3 registers (addresses x0F, x10, x11) which contain data (x21, x34, x65).

Figure 78. UART N Byte Read with AAD=0

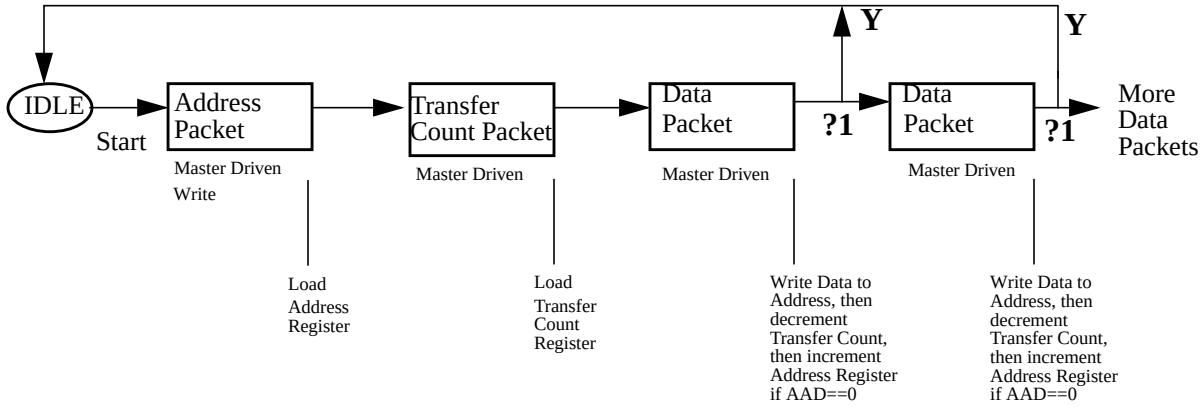


***1: Repeat N cycles (N>=0) of RxD = '1' and TxD = '1'.**

Read 1 register 3 times (addresses x0F) which contain data (x21).

Figure 79. UART N Byte Read with AAD=1

5.4.4 UART Sequence Diagrams



?1 := Transfer Count == 0.

Figure 80. UART Write Sequence

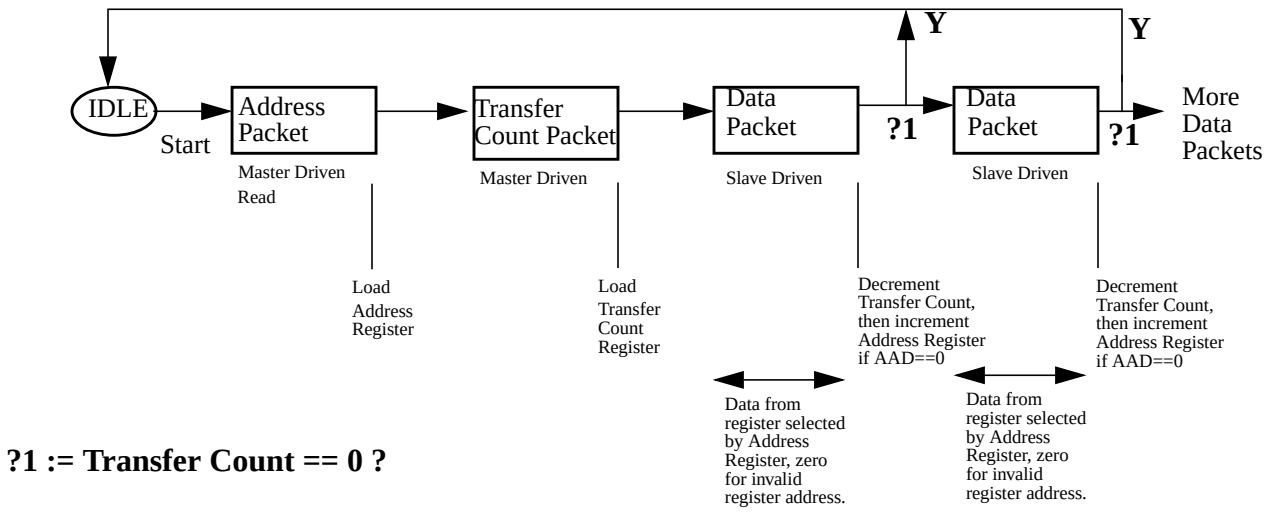


Figure 81. UART Read Sequence

6. System Reset and Low power modes

6.1 System Reset

A system hard reset is required before the HDCS Sensor will function properly. The Sensor may be reset using the external nRST pin (hard reset). A partial reset may be done by setting the RST bit of the CONFIG register (soft reset), or by asserting the SLP bit of th CONFIG register (soft sleep), or by asserting the external pin nSTBY (hard sleep). The external nRST pin should be held low for 1 us while nSTBY is high and CLK is running. The nSTBY and nRST pins should not be asserted at the same time. This causes all outputs to tri-state for board test. At the end of system reset the RUN bit of the CONFIG register is off. All system activity and sequencers remain IDLE until RUN bit of the CONFIG register is set, except for the system interface and CONFIG register, which is required to set the RUN bit. The System interface remains IDLE until serial data is received. It takes at least 64 cycles to transmit the serial command to write the RUN bit.

For board test function, if the external pins nRST and nSTBY are both asserted low at the same time all drivers are tri-stated.

Synchronous exit of reset is guaranteed. There must be a minimum of 8 clocks before nRST is de-asserted.

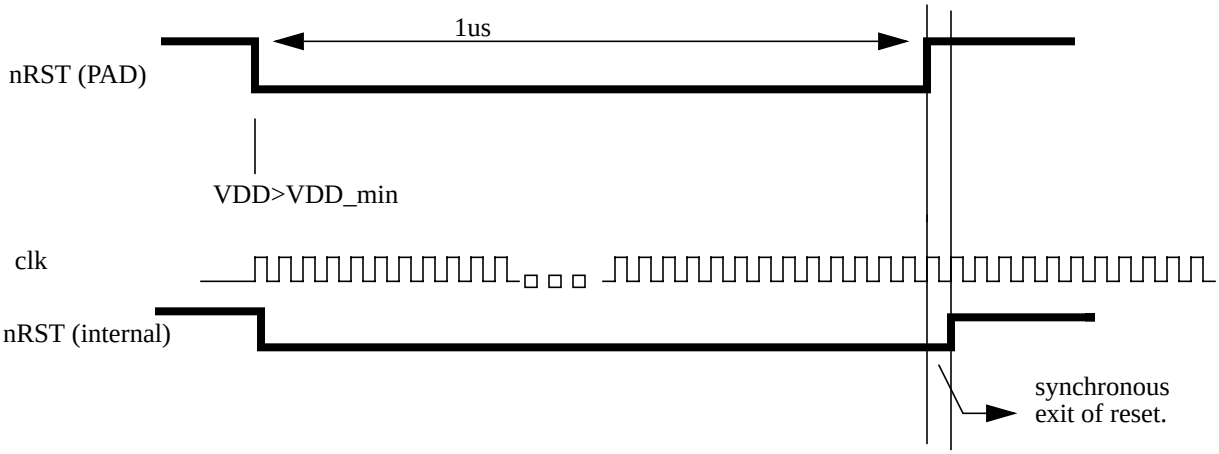
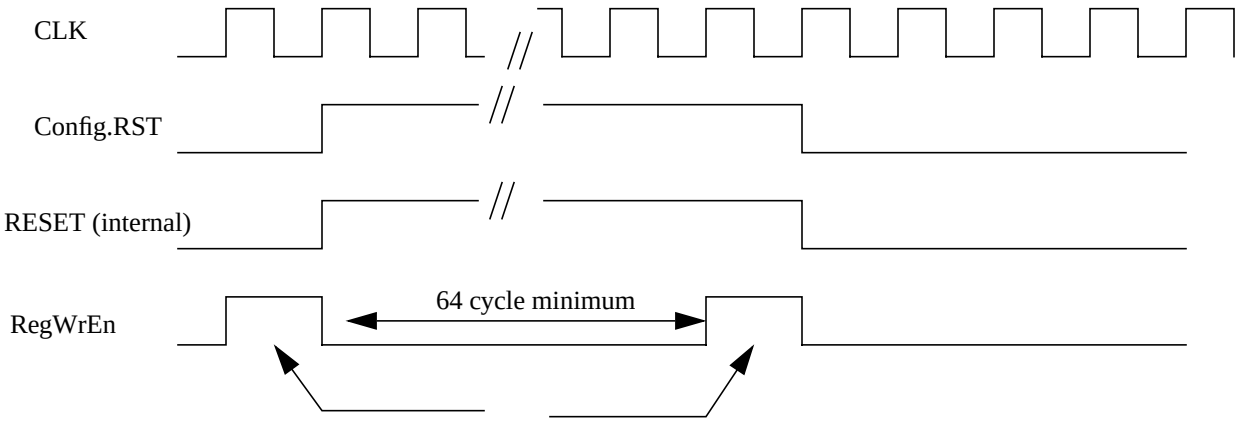


Figure 82. System Reset Using External nRST pin.

The HDCS Sensor provide a soft reset by writing the RST bit of the CONFIG Register. System reset must occur before soft reset. The RUN bit of the CONFIG register is reset after a soft reset, and after a soft sleep.



RST bit of CONFIG reg is set by the serial interface. 9 bits must be transmitted on the serial interface (fastet speed is 8 cycles per bit) between the set and reset of the RST bit.

Figure 83. System Soft Reset using RUN bit of CONFIG reg.

6.2 Low Power / Clock Domains.

The HDCS Sensor provides 2 low power modes. The first mode uses the external pin, nSTBY, to turn off all clocks and DC currents. Asserting the nSTBY pin also performs a partial reset. The system registers are preserved, but sequencers are reset. The system interface is not operating in this mode. The second low power mode uses the SLP (sleep) bit of the CONFIG register. This mode turns off all DC currents, and de-gates all clocks, except for the system interface and CONFIG register.

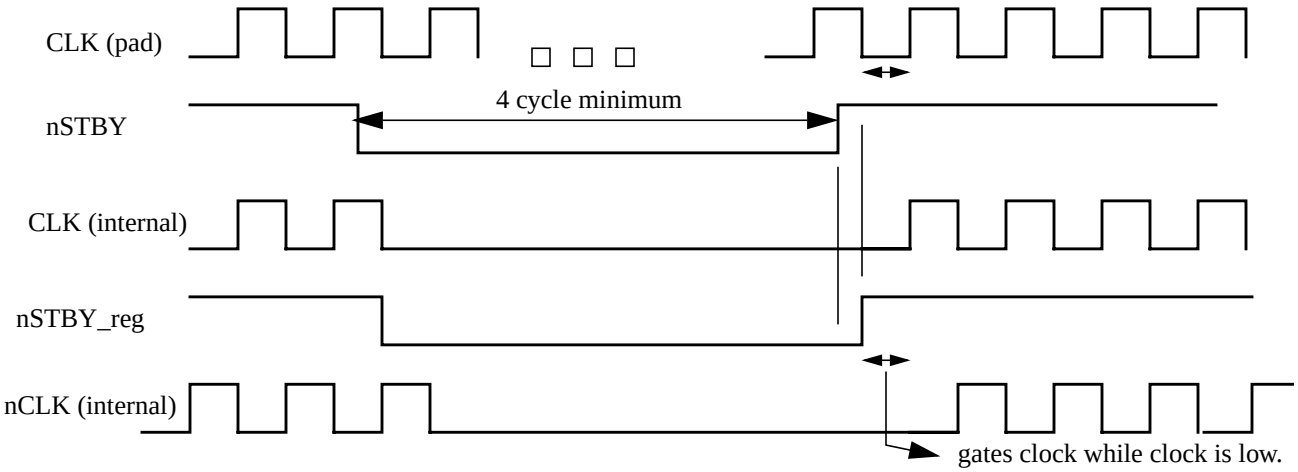
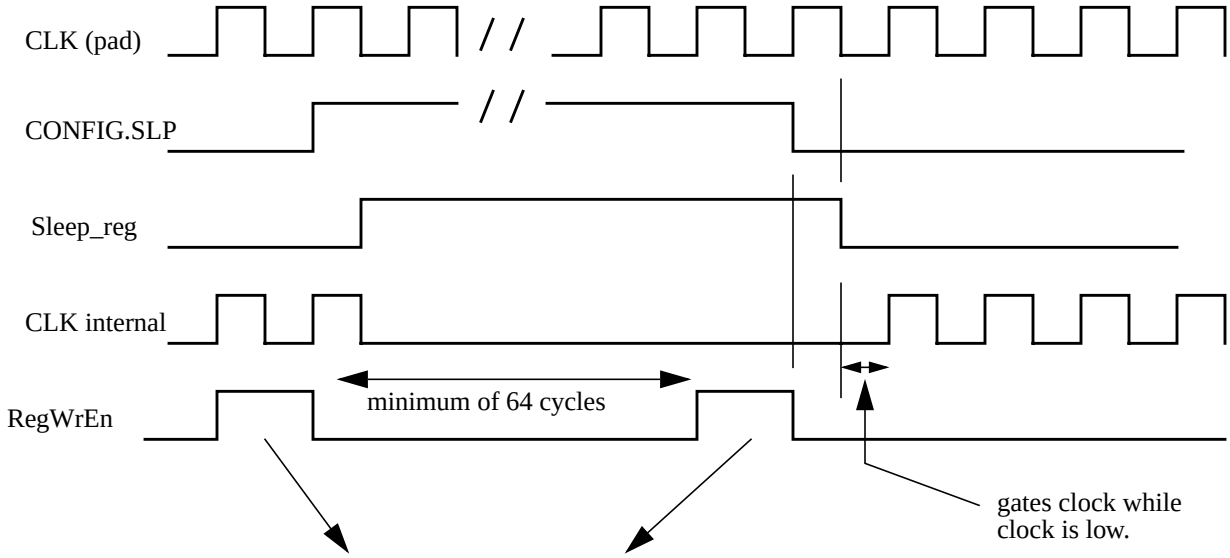


Figure 84. Low Power Mode using external nSTBY pad.



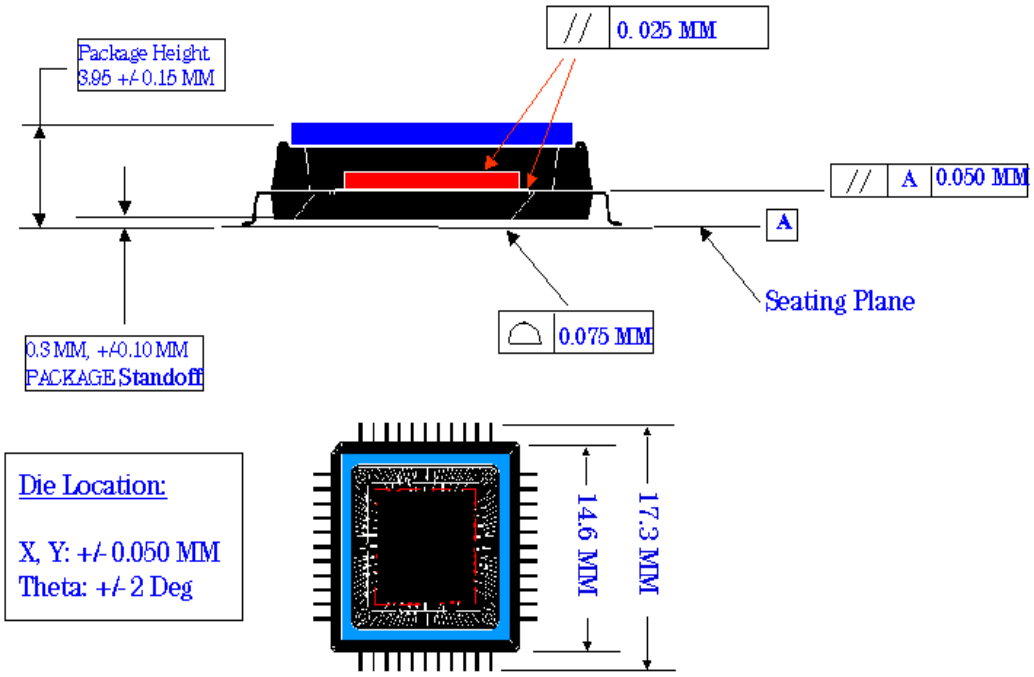
The SLP bit of the CONFIG registeris is set by the serial interface. 9 bits must be transmitted on the serial interface (fastet speed is 8 cycles per bit) between the set and reset of the SLP bit.

Figure 85. Low Power Mode using SLP bit of CONFIG reg.

7. Packaging

7.0.1 General Package Specs

- # of Leads (package): 44 (11 per side) gull wing leads
- Leadframe - Copper



Dimensions Shown = Millimeters

Figure 86. Package Drawing

7.1 Package Pin List

PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	NC	12	TCLK	23	DATA0	34	DATA7
2	NC	13	DRDY	24	DATA1	35	DATA8
3	nIRQ_NCC	14	AGND	25	DATA2	36	DATA9
4	nROW	15	GND	26	AGND	37	VDD
5	AVDD	16	VDD	27	DATA3	38	AVDD
6	AGND	17	AVDD	28	AVDD	39	nSTBY
7	GND	18	NC	29	GND	40	nRST
8	CLK	19	NC	30	AGND	41	AGND
9	VDD	20	AGND	31	DATA4	42	PVDD
10	TxD	21	NC	32	DATA5	43	IMODE
11	RxD	22	NC	33	DATA6	44	nFRAME_NSYNC

Table 52. Package Pin List

8. Electrical and Power Specifications

8.1 Electrical Specifications

This section covers the electrical and power specifications of the HDCS Image Sensor.

8.1.1 Absolute Maximum Ratings

Specification	Description	Min	Max	Units
VDD	Power supply voltage		3.6	V
V_{port}	DC input voltage at any port		3.6	V
Tj	Junction temperature	0	110	C

Table 53. Absolute Maximum Rating

8.1.2 DC Power Specifications

Specification	Description	Conditions	Min	Typ	Max	Units
VDD	Operating Power Supply Voltage		3.0	3.3	3.6	V

Table 54. DC Specifications

8.1.3 Pin Capacitance

Specification	Description	Max	Units
CinCLK	CLK Input Port Capacitance	2	pF
Cin	All Other Input Port Capacitances	1	pF

Table 55. Pin Capacitance

9. Glossary

ADC	Acronym for “analog to digital converter”.
APS	Acronym for “Active Pixel Sensor”.
CIF	Acronym for “Common Intermediate Format”. Commonly used to define a pixel array of 352 columns by 288 rows.
Column Processing	Refers to the portion of the row processing time that is used to perform an analog to digital conversion on the previously sampled pixel information for all of the pixels in one row of the selected image window.
Exposure	Duration of time that transpires from when a pixel is reset until it is subsequently sampled. Used synonomously with integration time.
fps	Acronym for “frames per second”.
Image Capture Process	Sequence of operations executed to expose, sample, convert, and output image sensor data. May be one or more frames.
Image Window	Rectangular region of the image sensor array that is sampled, converted, and output during an image capture process. The window coordinates are defined by the FWROW, FWCOL, LWROW, and LWCOL registers.
PGA	Acronym for “programmable gain amplifier”.
Pre-integration Period	The period of time starting when an image capture process is initiated and ending when the first row in the image window is sampled. Essentially equivalent in duration to the exposure duration, but it only occurs prior to sampling the first frame sampled during each image capture process.
Row Processing	Refers to the sequence of operations required to sample one row of pixels in the selected image window, convert the analog information to digital format and output it.
Timing Controller Start Overhead	Number of clock cycles required for the internal timing controller to begin operating after the internal assertion of the RUN bit of the CONTROL register.
VGA	Acronym for “video graphics adapter”. Commonly used to define a pixel array of 640 columns by 640 rows.

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