

HIGH VOLTAGE MONOLITHIC IC**HDL6V5583****Octal $\pm 100V$ 1.8A 3-level Ultrasound Pulser**

The HITACHI HDL6V5583 is an octal, high-voltage, high-speed fully-integrated pulser for medical ultrasound imaging applications. The HDL6V5583 consists of logic interface, level translators, MOSFET gate drive buffers with embedded/external-selectable floating voltage regulators, and high-voltage, high-current MOSFETs for pulsing and active ground clamping for each channel. The HDL6V5583 is pin-compatible with HDL6V5582/83E.

Functions

- 8-channel, 3-level pulser with active ground clamping with 2-input per channel

Features

- 0 to $\pm 100V$ output voltage
- $\pm 1.8A$ source and sink peak current for pulsing without output blocking high-voltage (HV) diodes
- $\pm 1.0A$ source and sink peak current for active ground clamping with output blocking HV diodes
- 500Ω ($\pm 0.05A$) active output termination working with active ground clamping
- Embedded/external-selectable floating voltage regulators to the gate drive buffers
- Input data synchronization with a clock signal (user-selectable)
- Integrated noise-cut low-voltage (LV) diodes
- Up to 20MHz operation frequency (@ $\pm 60V$ output, 220pF load)
- 1.8V to 5V CMOS logic interface
- 4-mode output drive current control for power saving
- Thermal protection
- Power supply sequence free
- Latch-up free, lower crosstalk between channels by SOI CMOS technology
- 52-lead 8mm x 8mm QFN package (RoHS compliant)
- Pin-compatible with HDL6V5582/83E

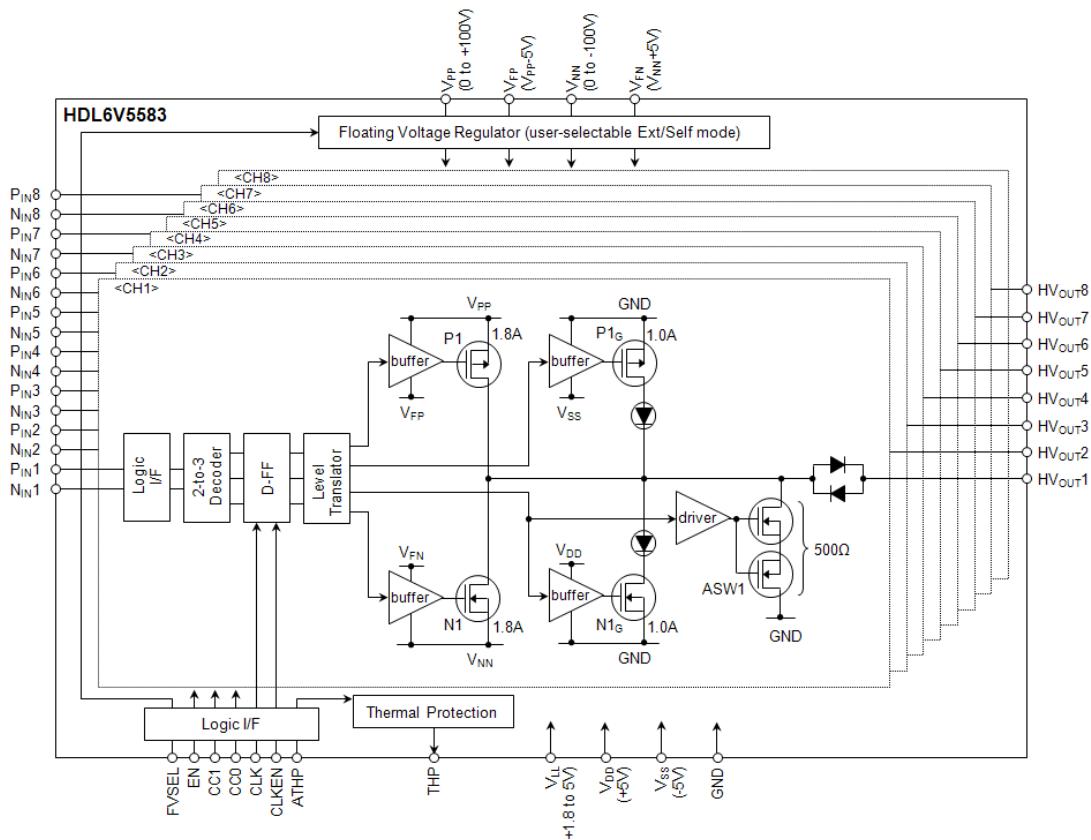


Fig.1 Block diagram

HITACHI

MDD-5583-1.0

Copyright (c)2010, Hitachi Ltd., Micro Device Division All rights reserved.

HDL6V5583

1. Absolute Maximum Ratings

$T_A=25^\circ\text{C}$ unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply	V_{LL}	-0.4 to +7	V	
2	Positive logic and level translator supply	V_{DD}	-0.4 to +7	V	
3	Negative logic and level translator supply	V_{SS}	-7 to +0.4	V	
4	Positive high voltage supply	V_{PP}	-0.5 to +105	V	
5	Negative high voltage supply	V_{NN}	-105 to +0.5	V	
6	Differential high voltage supply	$V_{PP}- V_{NN}$	+210	V	
7	High voltage outputs (x=1~8)*	HV_{OUTX}	-105 to +105	V	
8	Gate drive buffer voltages	$(V_{PP}- V_{FP}),$ $(V_{FN}- V_{NN})$	-0.4 to +7	V	FVSEL=0
9	THP (THERmal Protection) output	THP	-0.4 to +7	V	
10	All logic input voltages (x=1~8)	$P_{INX}, N_{INX}, EN, CLK,$ $CLKEN, CC1, CC0,$ $ATHP, FVSEL$	-0.4 to +7	V	
11	Operating junction temperature	T_{Jop}	-20 to +150	°C	
12	Storage temperature	T_{STG}	-55 to +150	°C	
13	Maximum power dissipation	P_{Dmax}	4	W	

Note: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Conditions, and Circuits (Recommended)

2.1 Operating Supply Voltages and Conditions

Table 2 Recommended Operating Supply Voltages and Conditions

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic voltage supply	V_{LL}	2.4	2.5 to 5	V_{DD}	V	Clock mode($\leq 80\text{MHz}$)
			2.6	2.7 to 5	V_{DD}	V	Clock mode($\leq 100\text{MHz}$)
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Positive low voltage supply	V_{DD}	4.75	5	5.25	V	
3	Negative low voltage supply	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high voltage supply	V_{PP}	0	-	100	V	
5	Negative high voltage supply	V_{NN}	-100	-	0	V	
6	Differential high voltage supply	$V_{PP}- V_{NN}$	0	-	200	V	
7	P-ch floating gate drive voltage supply	V_{FP}	$V_{PP}-5.25$	$V_{PP}-5$	$V_{PP}-4.75$	V	FVSEL=0
8	N-ch floating gate drive voltage supply	V_{FN}	$V_{NN}+4.75$	$V_{NN}+5$	$V_{NN}+5.25$	V	FVSEL=0
9	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V	
10	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V	
11	IC substrate voltage *	V_{SUB}	-	0	-	V	
12	Slew rate limit of V_{PP}, V_{NN}	SR_{MAX}	-	-	25	V/ms	
13	Operating free-air temperature	T_A	0	25	75	°C	

Note: * Substrate bottom is internally connected to the central thermal pad on the bottom of the package.

It must be soldered to the ground.

HDL6V5583

2.2 Power-Up/Down Sequence

Power-Supply Sequence is not required.

2.3 Application Circuits

(a) EMBEDDED floating voltage supplies (FVSEL=1)

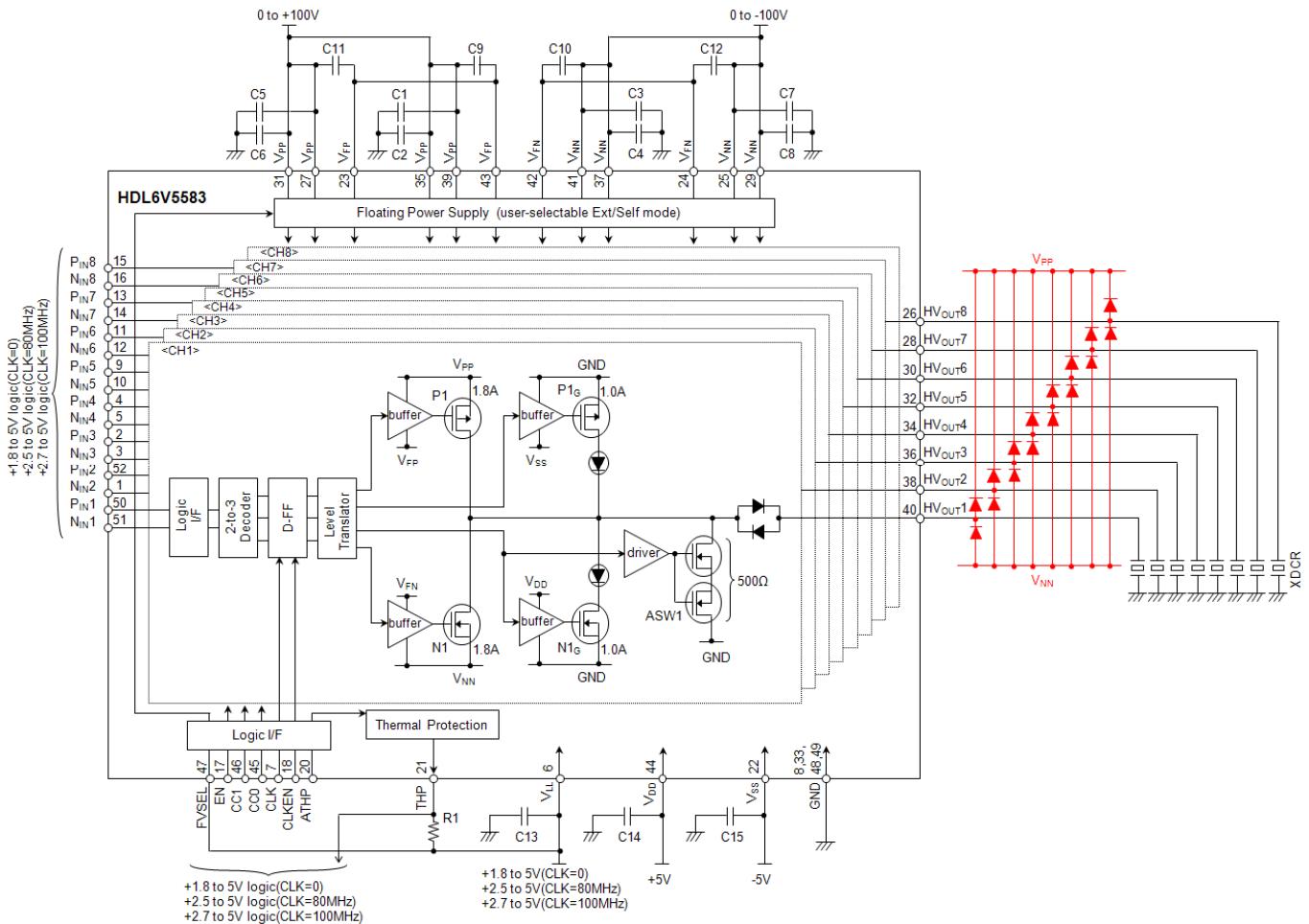


Fig. 2-(a) Typical Application Circuit-1

Note:

1. High-voltage power supply pins, V_{PP}/V_{NN} , can draw fast transient currents up to $\pm 1.8A$. Therefore, ceramic capacitors of over 200V 0.1 μF to 1 μF (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1 μF to 1 μF (C13~15) should also be connected close to the low-voltage power supply pins, $V_{LL}/V_{DD}/V_{SS}$.
2. Ceramic capacitors of over 15V 1 μF to 2.2 μF (C9~12) should be connected between each floating voltage pin (V_{FP}/V_{FN}) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. [PRECAUTION] External high-voltage clamp diodes between $HV_{OUT}X$ and V_{PP}/V_{NN} as shown in Fig.2-(a) are strongly recommended to mitigate excessive voltage overshoot caused by a reflection from a probe.

HDL6V5583

2.3 Application Circuits (Cont.)

(b) EXTERNAL floating voltage supplies (FVSEL=0)

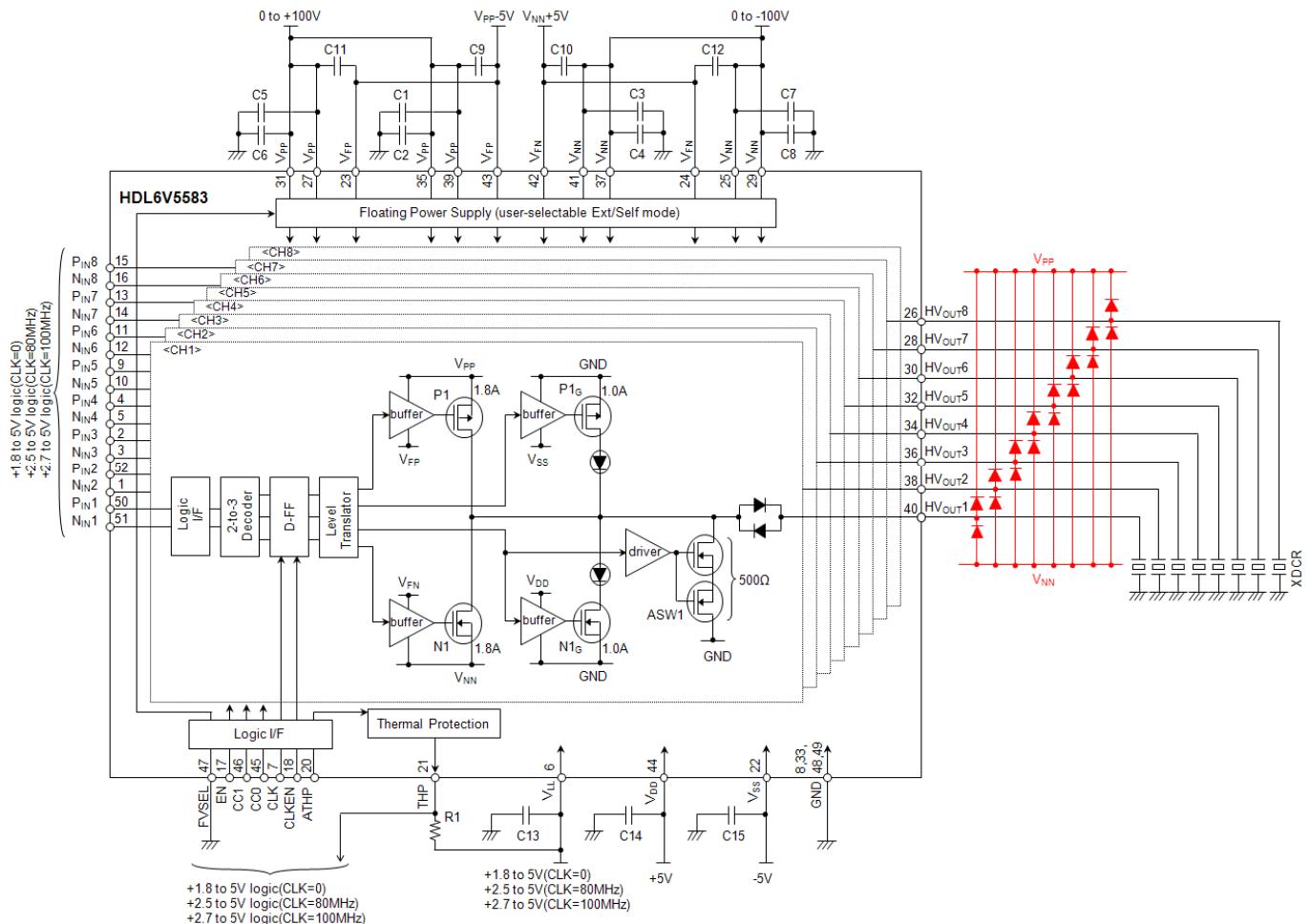


Fig. 2-(b) Typical Application Circuit-2

Note:

1. High-voltage power supply pins, V_{PP}/V_{NN} , can draw fast transient currents up to $\pm 1.8A$. Therefore, ceramic capacitors of over 200V 0.1μF to 1μF (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1μF to 1μF (C13~15) should also be connected close to the low-voltage power supply pins, $V_{LL}/V_{DD}/V_{SS}$.
2. Ceramic capacitors of over 15V 1μF to 2.2μF (C9~12) should be connected between each floating voltage pin (V_{FP}/V_{FN}) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between $HV_{OUT}x$ and V_{PP}/V_{NN} as shown in Fig.2-(b) are strongly recommended to mitigate excessive voltage overshoot caused by a reflection from a probe.

HDL6V5583

3. Electrical Characteristics

3.1 FVSEL=1 (EMBEDDED floating voltage supplies)

3.1.1 Clock Mode (CLKEN=0)

DC Characteristics

Table 3 DC Characteristics (Embedded FV, Clock mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $T_A=25^\circ C$, $220pF//1k\Omega$ load, $CLK=100MHz$, $ATHP=0$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	P_{INX} , N_{INX} , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	μA	ATHP 50k Ω internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	P_{INX} , N_{INX} , CLK, ATHP
			-	66	-	μA	EN, CC1, CC0, CLKEN, FVSEL 50k Ω internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	1.0	-	mA	Quiescent current-1 EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$
5	V_{DD} current	I_{DDQD}	-	14	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.15	-	mA	
7	V_{PP} current	I_{PPQD}	-	0.03	-	mA	
8	V_{NN} current	I_{NNQD}	-	0.03	-	mA	
9	V_{LL} current	I_{LLQE}	-	1.1	-	mA	
10	V_{DD} current	I_{DDQE}	-	18	-	mA	EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$ $P_{INX}=1$, $N_{INX}=1$ ($x=1-8$)
11	V_{SS} current	I_{SQQE}	-	5.0	-	mA	
12	V_{PP} current	I_{PPQE}	-	0.20	-	mA	
13	V_{NN} current	I_{NNQE}	-	0.20	-	mA	
14	V_{LL} current	I_{LLPW}	-	1.1	-	mA	Operating current-1 8-channel active Bipolar 1-cycle $f=5MHz$, $PRT=200\mu s$ $V_{PP}/V_{NN}=+/-60V$ $EN=0$, Current mode=4
15	V_{DD} current	I_{DDPW}	-	18	-	mA	
16	V_{SS} current	I_{SPPW}	-	7.6	-	mA	
17	V_{PP} current	I_{PPPW}	-	1.2	-	mA	
18	V_{NN} current	I_{NNPW}	-	1.8	-	mA	
19	V_{LL} current	I_{LLCW4}	-	1.2	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 $f=5MHz$, $V_{PP}/V_{NN}=+/-5V$ $EN=0$
20	V_{DD} current	I_{DDCW4}	-	43	-	mA	
21	V_{SS} current	I_{SCCW4}	-	33	-	mA	
22	V_{PP} current	I_{PPCW4}	-	178	-	mA	
23	V_{NN} current	I_{NCW4}	-	174	-	mA	
24	V_{LL} current	I_{LLCW3}	-	1.2	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 $f=5MHz$, $V_{PP}/V_{NN}=+/-5V$ $EN=0$
25	V_{DD} current	I_{DDCW3}	-	39	-	mA	
26	V_{SS} current	I_{SCCW3}	-	28	-	mA	
27	V_{PP} current	I_{PPCW3}	-	170	-	mA	
28	V_{NN} current	I_{NCW3}	-	166	-	mA	

HDL6V5583

Table 3 DC Characteristics (Embedded FV, Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
29	V _{LL} current	I _{LLCW2}	-	1.2	-	mA	Operating current-4
30	V _{DD} current	I _{DDCW2}	-	35	-	mA	8-channel active
31	V _{SS} current	I _{SSCW2}	-	22	-	mA	Bipolar Continuous Wave
32	V _{PP} current	I _{PPCW2}	-	162	-	mA	Current mode=2
33	V _{NN} current	I _{NNCW2}	-	158	-	mA	f=5MHz, V _{PP} /V _{NN} =+/-5V
34	V _{LL} current	I _{LLCW1}	-	1.3	-	mA	EN=0
35	V _{DD} current	I _{DDCW1}	-	31	-	mA	Operating current-5
36	V _{SS} current	I _{SSCW1}	-	17	-	mA	8-channel active
37	V _{PP} current	I _{PPCW1}	-	148	-	mA	Bipolar Continuous Wave
38	V _{NN} current	I _{NNCW1}	-	146	-	mA	Current mode=1
							f=5MHz, V _{PP} /V _{NN} =+/-5V
							EN=0

AC Characteristics

Table 4 AC Characteristics (Embedded FV, Clock mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, CLK=100MHz, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	f _{CLK}	-	100	-	MHz	See Fig.6 D=τ/T
2	Duty cycle	D	40	50	60	%	
3	Setup time	t _{SU}	-0.2	-	-	ns	
4	Hold time	t _{HOLD}	3.4	-	-	ns	
5	Delay time on outputs rise	t _{dr(on)}	-	53	-	ns	Bipolar half cycle f=5MHz, PRT=200μs V _{PP} /V _{NN} =+/-60V Current mode=4 See Fig.3
6	Delay time on outputs fall	t _{df(on)}	-	53	-	ns	
7	Delay time off outputs rise	t _{dr(off)}	-	53	-	ns	
8	Delay time off outputs fall	t _{df(off)}	-	53	-	ns	
9	t _{dr(on)} -t _{df(on)} Delay time matching	Δt _{delay(on)}	-	±1	±3	ns	
10	t _{dr(off)} -t _{df(off)} Delay time matching	Δt _{delay(off)}	-	±1	±3	ns	
11	Output frequency range	f _{OUT}	-	-	20	MHz	
12	Output rise time	t _r	-	18	-	ns	
13	Output fall time	t _f	-	18	-	ns	
14	Second harmonic distortion	HD2	-	-40	-	dBc	
15	Delay jitter on rise or fall	t _{Jr} , t _{Jf}	-	20	-	ps	Bipolar CW, f=5MHz V _{PP} /V _{NN} =+/-5V, Current mode=1 See Fig.5
16	Enable time	t _{EN}	-	57	-	ns	EN fall edge to output burst
17	Disable time	t _{DIS}	-	83	-	ns	EN rise edge to output HiZ
18	Clock Enable time	t _{CLKEN}	-	57	-	ns	CLKEN fall edge to output burst
19	Clock Disable time	t _{CLKDIS}	-	83	-	ns	CLKEN rise edge to output HiZ

HDL6V5583

Thermal Protection Characteristics

Table 5 Thermal Protection Characteristics

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	1.0	V	$V_{LL}=3.3V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	90	110	130	°C	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	°C	

Device Characteristics

Table 6 Output P-Channel MOSFET (Px) Characteristics

 $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUTP}	-	-1.8	-	A	$V_{GS}=-5V$, $V_{DS}=-100V$
2	Channel resistance	R_{ONP}	-	7	-	Ω	$V_{GS}=-5V$, $I_D=-0.5A$
3	Output capacitance	C_{OSSP}	-	27	-	pF	$V_{GS}=0V$, $V_{DS}=-10V$, $f=1MHz$

Note: These items above are not tested when shipped.

Table 7 Output N-Channel MOSFET (Nx) Characteristics

 $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUTN}	-	1.8	-	A	$V_{GS}=5V$, $V_{DS}=100V$
2	Channel resistance	R_{ONN}	-	7	-	Ω	$V_{GS}=5V$, $I_D=0.5A$
3	Output capacitance	C_{OSSN}	-	11	-	pF	$V_{GS}=0V$, $V_{DS}=10V$, $f=1MHz$

Note: These items above are not tested when shipped.

Table 8 Output GND-Clamp P-Channel MOSFET (Px_G) Characteristics $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUTPG}	-	-1.0	-	A	$V_{GS}=-5V$, $V_{DS}=-100V$
2	Channel resistance	R_{ONG}	-	13	-	Ω	$V_{GS}=-5V$, $I_D=-0.1A$
3	Output capacitance	C_{OSSPG}	-	15	-	pF	$V_{GS}=0V$, $V_{DS}=-10V$, $f=1MHz$

Note: These items above are not tested when shipped.

Table 9 Output GND-Clamp N-Channel MOSFET (Nx_G) Characteristics $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	I_{OUTNG}	-	1.0	-	A	$V_{GS}=5V$, $V_{DS}=100V$
2	Channel resistance	R_{ONG}	-	13	-	Ω	$V_{GS}=5V$, $I_D=0.1A$
3	Output capacitance	C_{OSSNG}	-	6	-	pF	$V_{GS}=0V$, $V_{DS}=10V$, $f=1MHz$

Note: These items above are not tested when shipped.

HDL6V5583

Table 10 Output GND-Clamp Analog Switch (ASWx) Characteristics

 $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	On-state resistance	R_{ONASW}	-	500	-	Ω	$V_{GS}=5V, I_D=0.01A$

Note: These items above are not tested when shipped.

Table 11 Output Blocking HV Diode Characteristics

 $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	$V_{F DHV}$	-	1.0	-	V	$I_F=100mA$
2	Reverse voltage	$V_{R DHV}$	200	-	-	V	$I_R=1\mu A$

Note: These items above are not tested when shipped.

Table 12 Output Noise-Cut LV Diode Characteristics

 $T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FDLV}	-	0.85	-	V	$I_F=100mA$

Note: These items above are not tested when shipped.

HDL6V5583

3.1.2 Transparent Mode (CLKEN=1)

DC Characteristics

Table 13 DC Characteristics (Embedded FV, Transparent mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $T_A=25^\circ C$, $220pF//1k\Omega$ load, $CLK=0$, $ATHP=0$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	$P_{INX}, N_{INX}, EN, CC1, CC0, CLK, CLKEN, FVSEL$
			-	66	-	μA	$ATHP$ 50k Ω internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	$P_{INX}, N_{INX}, CLK, ATHP$
			-	66	-	μA	$EN, CC1, CC0, CLKEN, FVSEL$ 50k Ω internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	0.5	-	μA	Quiescent current-1 $EN=1$ (Disable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$
5	V_{DD} current	I_{DDQD}	-	1.1	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.10	-	mA	
7	V_{PP} current	I_{PPQD}	-	0.03	-	mA	
8	V_{NN} current	I_{NNQD}	-	0.03	-	mA	
9	V_{LL} current	I_{LLQE}	-	66	-	μA	Quiescent current-2 $EN=0$ (Enable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$ $P_{INx}=1, N_{INx}=1$ (x=1~8)
10	V_{DD} current	I_{DDQE}	-	5.5	-	mA	
11	V_{SS} current	I_{SSQE}	-	5.0	-	mA	
12	V_{PP} current	I_{PPQE}	-	0.15	-	mA	
13	V_{NN} current	I_{NNQE}	-	0.15	-	mA	
14	V_{LL} current	I_{LLPW}	-	75	-	μA	Operating current-1 8-channel active Bipolar 1-cycle $f=5MHz, PRT=200\mu s$ $V_{PP}/V_{NN}=+/-60V$ $EN=0$, Current mode=4
15	V_{DD} current	I_{DDPW}	-	5.6	-	mA	
16	V_{SS} current	I_{SSPW}	-	5.1	-	mA	
17	V_{PP} current	I_{PPPW}	-	1.2	-	mA	
18	V_{NN} current	I_{NNPW}	-	1.8	-	mA	
19	V_{LL} current	I_{LLCW4}	-	0.60	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 $f=5MHz, V_{PP}/V_{NN}=+/-5V$ $EN=0$
20	V_{DD} current	I_{DDCW4}	-	32	-	mA	
21	V_{SS} current	I_{SSCW4}	-	34	-	mA	
22	V_{PP} current	I_{PPCW4}	-	178	-	mA	
23	V_{NN} current	I_{NNCW4}	-	174	-	mA	
24	V_{LL} current	I_{LLCW3}	-	0.65	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 $f=5MHz, V_{PP}/V_{NN}=+/-5V$ $EN=0$
25	V_{DD} current	I_{DDCW3}	-	28	-	mA	
26	V_{SS} current	I_{SSCW3}	-	28	-	mA	
27	V_{PP} current	I_{PPCW3}	-	170	-	mA	
28	V_{NN} current	I_{NNCW3}	-	166	-	mA	

HDL6V5583

Table 13 DC Characteristics (Embedded FV, Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
29	V _{LL} current	I _{LLCW2}	-	0.65	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
30	V _{DD} current	I _{DDCW2}	-	24	-	mA	
31	V _{SS} current	I _{SSCW2}	-	22	-	mA	
32	V _{PP} current	I _{PPCW2}	-	162	-	mA	
33	V _{NN} current	I _{NNCW2}	-	158	-	mA	
34	V _{LL} current	I _{LLCW1}	-	0.70	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
35	V _{DD} current	I _{DDCW1}	-	20	-	mA	
36	V _{SS} current	I _{SSCW1}	-	17	-	mA	
37	V _{PP} current	I _{PPCW1}	-	148	-	mA	
38	V _{NN} current	I _{NNCW1}	-	146	-	mA	

AC Characteristics

Table 14 AC Characteristics (Embedded FV, Transparent mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, CLK=0, EN=0, ATHP=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	t _{dr(on)}	-	48	-	ns	Bipolar half cycle f=5MHz, PRT=200μs V _{PP} /V _{NN} =+/-60V Current mode=4 See Fig.3
2	Delay time on outputs fall	t _{df(on)}	-	48	-	ns	
3	Delay time off outputs rise	t _{dr(off)}	-	48	-	ns	
4	Delay time off outputs fall	t _{df(off)}	-	48	-	ns	
5	t _{dr(on)} -t _{df(on)} Delay time matching	Δt _{delay(on)}	-	±1	±3	ns	
6	t _{dr(off)} -t _{df(off)} Delay time matching	Δt _{delay(off)}	-	±1	±3	ns	
7	Output frequency range	f _{OUT}	-	-	20	MHz	
8	Output rise time	t _r	-	18	-	ns	
9	Output fall time	t _f	-	18	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Delay jitter on rise or fall	t _{Jr} , t _{Jf}	-	20	-	ps	Bipolar CW, f=5MHz V _{PP} /V _{NN} =+/-5V, Current mode=1 See Fig.5
12	Enable time	t _{EN}	-	52	-	ns	EN fall edge to output burst
13	Disable time	t _{DIS}	-	78	-	ns	EN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.

HDL6V5583

3.2 FVSEL=0 (EXTERNAL floating voltage supplies)

3.2.1 Clock Mode (CLKEN=0)

DC Characteristics

Table 15 DC Characteristics (External FV, Clock mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FP}=V_{PP}-5V$, $V_{FN}=V_{NN}+5V$, $T_A=25^\circ C$, 220pF//1k Ω load, CLK=100MHz, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	P_{INX} , N_{INX} , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	μA	ATHP 50k Ω internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	P_{INX} , N_{INX} , CLK, ATHP
			-	66	-	μA	EN, CC1, CC0, CLKEN, FVSEL 50k Ω internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	1.0	-	mA	Quiescent current-1 EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$
5	V_{DD} current	I_{DDQD}	-	14	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.1	-	mA	
7	V_{PP} current	I_{PPQD}	-	0	-	mA	
8	V_{NN} current	I_{NNQD}	-	0	-	mA	
9	V_{FP} current	I_{FPQD}	-	0.02	-	mA	
10	V_{FN} current	I_{FNQD}	-	0.02	-	mA	
11	V_{LL} current	I_{LLQE}	-	1.1	-	mA	Quiescent current-2 EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$ $P_{INX}=1$, $N_{INX}=1$ (x=1~8)
12	V_{DD} current	I_{DDQE}	-	18	-	mA	
13	V_{SS} current	I_{SSQE}	-	5.0	-	mA	
14	V_{PP} current	I_{PPQE}	-	0	-	mA	
15	V_{NN} current	I_{NNQE}	-	0	-	mA	
16	V_{FP} current	I_{FPQE}	-	0.02	-	mA	
17	V_{FN} current	I_{FNQE}	-	0.02	-	mA	
18	V_{LL} current	I_{LLPW}	-	1.1	-	mA	Operating current-1 8-channel active Bipolar 1-cycle $f=5MHz$, PRT=200 μs $V_{PP}/V_{NN}=+/-60V$ EN=0, Current mode=4
19	V_{DD} current	I_{DDPW}	-	18	-	mA	
20	V_{SS} current	I_{SSPW}	-	5.1	-	mA	
21	V_{PP} current	I_{PPPW}	-	2.0	-	mA	
22	V_{NN} current	I_{NNPW}	-	2.0	-	mA	
23	V_{FP} current	I_{FPPW}	-	0.20	-	mA	
24	V_{FN} current	I_{FNPW}	-	0.20	-	mA	

HDL6V5583

Table 15 DC Characteristics (External FV, Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V _{LL} current	I _{LLCW4}	-	1.2	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
26	V _{DD} current	I _{DDCW4}	-	24	-	mA	
27	V _{SS} current	I _{SSCW4}	-	8.0	-	mA	
28	V _{PP} current	I _{PPCW4}	-	160	-	mA	
29	V _{NN} current	I _{NNCW4}	-	160	-	mA	
30	V _{FP} current	I _{FPCW4}	-	31	-	mA	
31	V _{FN} current	I _{FNCW4}	-	20	-	mA	
32	V _{LL} current	I _{LLCW3}	-	1.2	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
33	V _{DD} current	I _{DDCW3}	-	24	-	mA	
34	V _{SS} current	I _{SSCW3}	-	8.0	-	mA	
35	V _{PP} current	I _{PPCW3}	-	156	-	mA	
36	V _{NN} current	I _{NNCW3}	-	156	-	mA	
37	V _{FP} current	I _{FPCW3}	-	22	-	mA	
38	V _{FN} current	I _{FNCW3}	-	15	-	mA	
39	V _{LL} current	I _{LLCW2}	-	1.2	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
40	V _{DD} current	I _{DDCW2}	-	24	-	mA	
41	V _{SS} current	I _{SSCW2}	-	8.0	-	mA	
42	V _{PP} current	I _{PPCW2}	-	148	-	mA	
43	V _{NN} current	I _{NNCW2}	-	148	-	mA	
44	V _{FP} current	I _{FPCW2}	-	16	-	mA	
45	V _{FN} current	I _{FNCW2}	-	11	-	mA	
46	V _{LL} current	I _{LLCW1}	-	1.3	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
47	V _{DD} current	I _{DDCW1}	-	24	-	mA	
48	V _{SS} current	I _{SSCW1}	-	8.0	-	mA	
49	V _{PP} current	I _{PPCW1}	-	136	-	mA	
50	V _{NN} current	I _{NNCW1}	-	136	-	mA	
51	V _{FP} current	I _{FPCW1}	-	8.0	-	mA	
52	V _{FN} current	I _{FNCW1}	-	6.0	-	mA	

HDL6V5583

AC Characteristics

Table 16 AC Characteristics (External FV, Clock mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FP}=V_{PP}-5V$, $V_{FN}=V_{NN}+5V$, $T_A=25^\circ C$, $220pF/1k\Omega$ load, $CLK=100MHz$, $EN=0$, $ATHP=0$, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	f_{CLK}	-	100	-	MHz	See Fig.6
2	Duty cycle	D	40	50	60	%	$D=\tau/T$
3	Setup time	t_{SU}	-0.2	-	-	ns	
4	Hold time	t_{HOLD}	3.4	-	-	ns	
5	Delay time on outputs rise	$t_{dr(on)}$	-	53	-	ns	Bipolar half cycle
6	Delay time on outputs fall	$t_{df(on)}$	-	53	-	ns	$f=5MHz$, $PRT=200\mu s$
7	Delay time off outputs rise	$t_{dr(off)}$	-	53	-	ns	$V_{PP}/V_{NN}=+/-60V$
8	Delay time off outputs fall	$t_{df(off)}$	-	53	-	ns	Current mode=4
9	$ t_{dr(on)}-t_{df(on)} $ Delay time matching	$\Delta t_{delay(on)}$	-	± 1	± 3	ns	See Fig.3
10	$ t_{dr(off)}-t_{df(off)} $ Delay time matching	$\Delta t_{delay(off)}$	-	± 1	± 3	ns	
11	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 2-cycle
12	Output rise time	t_r	-	18	-	ns	$f=5MHz$, $PRT=200\mu s$
13	Output fall time	t_f	-	18	-	ns	$V_{PP}/V_{NN}=+/-60V$
14	Second harmonic distortion	$HD2$	-	-40	-	dBc	Current mode=4 See Fig.4
15	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	20	-	ps	Bipolar CW, $f=5MHz$ $V_{PP}/V_{NN}=+/-5V$, Current mode=1 See Fig.5
16	Enable time	t_{EN}	-	57	-	ns	EN fall edge to output burst
17	Disable time	t_{DIS}	-	83	-	ns	EN rise edge to output HiZ
18	Clock Enable time	t_{CLKEN}	-	57	-	ns	CLKEN fall edge to output burst
19	Clock Disable time	t_{CLKDIS}	-	83	-	ns	CLKEN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.

HDL6V5583

3.2.2 Transparent Mode (CLKEN=1)

DC Characteristics

Table 17 DC Characteristics (External FV, Transparent mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FP}=V_{PP}-5V$, $V_{FN}=V_{NN}+5V$, $T_A=25^\circ C$, 220pF//1kΩ load, CLK=0, ATHP=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	P_{INX} , N_{INX} , EN, CC1, CC0, CLK, CLKEN, FVSEL
			-	66	-	μA	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	P_{INX} , N_{INX} , CLK, ATHP
			-	66	-	μA	EN, CC1, CC0, CLKEN, FVSEL 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	66	-	μA	Quiescent current-1 EN=1(Disable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$
5	V_{DD} current	I_{DDQD}	-	1.1	-	mA	
6	V_{SS} current	I_{SSQD}	-	0.10	-	mA	
7	V_{PP} current	I_{PPQD}	-	0	-	mA	
8	V_{NN} current	I_{NNQD}	-	0	-	mA	
9	V_{FP} current	I_{FPQD}	-	0.02	-	mA	
10	V_{FN} current	I_{FNQD}	-	0.02	-	mA	
11	V_{LL} current	I_{LLQE}	-	134	-	μA	
12	V_{DD} current	I_{DDQE}	-	5.5	-	mA	Quiescent current-2 EN=0(Enable) Current mode=4 $V_{PP}/V_{NN}=+/-100V$ $P_{INX}=1$, $N_{INX}=1$ (x=1~8)
13	V_{SS} current	I_{SSQE}	-	5.0	-	mA	
14	V_{PP} current	I_{PPQE}	-	0	-	mA	
15	V_{NN} current	I_{NNQE}	-	0	-	mA	
16	V_{FP} current	I_{FPQE}	-	0.02	-	mA	
17	V_{FN} current	I_{FNQE}	-	0.02	-	mA	
18	V_{LL} current	I_{LLPW}	-	142	-	μA	Operating current-1 8-channel active Bipolar 1-cycle $f=5MHz$, PRT=200μs $V_{PP}/V_{NN}=+/-60V$ EN=0, Current mode=4
19	V_{DD} current	I_{DDPW}	-	5.6	-	mA	
20	V_{SS} current	I_{SSPW}	-	5.1	-	mA	
21	V_{PP} current	I_{PPPW}	-	2.0	-	mA	
22	V_{NN} current	I_{NNPW}	-	2.0	-	mA	
23	V_{FP} current	I_{FPPW}	-	0.20	-	mA	
24	V_{FN} current	I_{FNPW}	-	0.20	-	mA	

HDL6V5583

Table 17 DC Characteristics (External FV, Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V _{LL} current	I _{LLCW4}	-	0.60	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
26	V _{DD} current	I _{DDCW4}	-	13	-	mA	
27	V _{SS} current	I _{SSCW4}	-	8.0	-	mA	
28	V _{PP} current	I _{PPCW4}	-	160	-	mA	
29	V _{NN} current	I _{NNCW4}	-	160	-	mA	
30	V _{FP} current	I _{FPCW4}	-	31	-	mA	
31	V _{FN} current	I _{FNCW4}	-	20	-	mA	
32	V _{LL} current	I _{LLCW3}	-	0.65	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
33	V _{DD} current	I _{DDCW3}	-	13	-	mA	
34	V _{SS} current	I _{SSCW3}	-	8.0	-	mA	
35	V _{PP} current	I _{PPCW3}	-	156	-	mA	
36	V _{NN} current	I _{NNCW3}	-	156	-	mA	
37	V _{FP} current	I _{FPCW3}	-	22	-	mA	
38	V _{FN} current	I _{FNCW3}	-	15	-	mA	
39	V _{LL} current	I _{LLCW2}	-	0.65	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
40	V _{DD} current	I _{DDCW2}	-	13	-	mA	
41	V _{SS} current	I _{SSCW2}	-	8.0	-	mA	
42	V _{PP} current	I _{PPCW2}	-	148	-	mA	
43	V _{NN} current	I _{NNCW2}	-	148	-	mA	
44	V _{FP} current	I _{FPCW2}	-	16	-	mA	
45	V _{FN} current	I _{FNCW2}	-	11	-	mA	
46	V _{LL} current	I _{LLCW1}	-	0.70	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz, V _{PP} /V _{NN} =+/-5V EN=0
47	V _{DD} current	I _{DDCW1}	-	13	-	mA	
48	V _{SS} current	I _{SSCW1}	-	8	-	mA	
49	V _{PP} current	I _{PPCW1}	-	136	-	mA	
50	V _{NN} current	I _{NNCW1}	-	136	-	mA	
51	V _{FP} current	I _{FPCW1}	-	8.0	-	mA	
52	V _{FN} current	I _{FNCW1}	-	6.0	-	mA	

HDL6V5583

AC Characteristics

Table 18 AC Characteristics (External FV, Transparent mode)

$V_{LL}=3.3V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FP}=V_{PP}-5V$, $V_{FN}=V_{NN}+5V$, $T_A=25^\circ C$, $220pF//1k\Omega$ load, $CLK=0$, $EN=0$, $ATHP=0$, 8-channel active, unless otherwise specified.

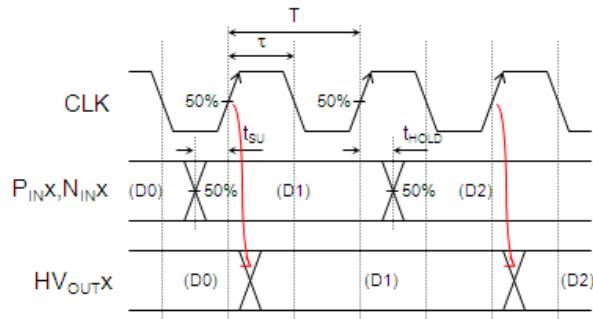
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	$t_{dr(on)}$	-	48	-	ns	Bipolar half cycle $f=5MHz$, $PRT=200\mu s$ $V_{PP}/V_{NN}=+/-60V$ Current mode=4 See Fig.3
2	Delay time on outputs fall	$t_{df(on)}$	-	48	-	ns	
3	Delay time off outputs rise	$t_{dr(off)}$	-	48	-	ns	
4	Delay time off outputs fall	$t_{df(off)}$	-	48	-	ns	
5	$ t_{dr(on)}-t_{df(on)} $ Delay time matching	$\Delta t_{delay(on)}$	-	± 1	± 3	ns	
6	$ t_{dr(off)}-t_{df(off)} $ Delay time matching	$\Delta t_{delay(off)}$	-	± 1	± 3	ns	
7	Output frequency range	f_{OUT}	-	-	20	MHz	
8	Output rise time	t_r	-	18	-	ns	
9	Output fall time	t_f	-	18	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	See Fig.4
11	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	20	-	ps	Bipolar CW, $f=5MHz$ $V_{PP}/V_{NN}=+/-5V$, Current mode=1 See Fig.5
12	Enable time	t_{EN}	-	52	-	ns	EN fall edge to output burst
13	Disable time	t_{DIS}	-	78	-	ns	EN rise edge to output HiZ

See Table 5 through 12 for the characteristics of Thermal Protection, and Devices.

HDL6V5583

4. Switching Time Diagram (EN=0)

Clock mode (CLKEN=0)



Transparent mode (CLKEN=1)

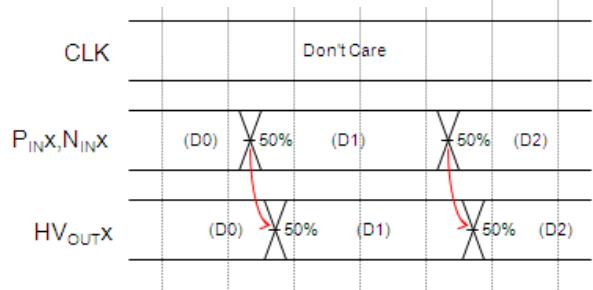


Fig. 3 Setup/hold time

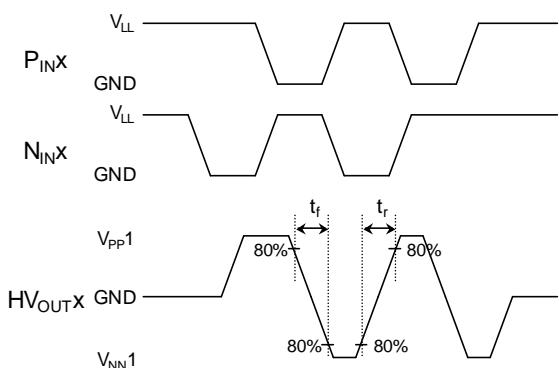


Fig. 5 Output rise/fall time

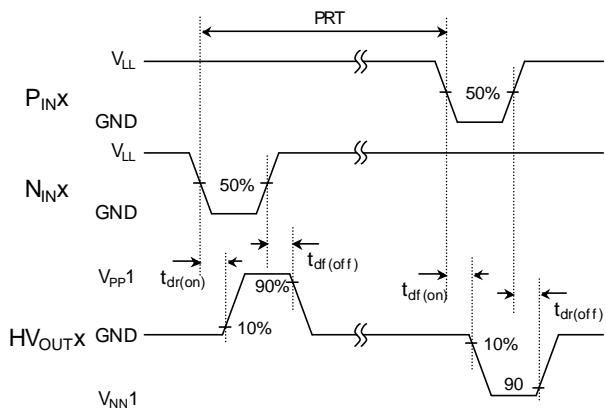


Fig. 4 Propagation delay time

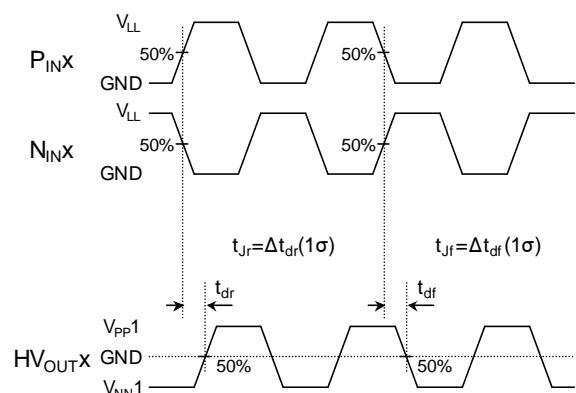


Fig. 6 Delay jitter on rise/fall

HDL6V5583

5. Truth Table

Table 19 Truth Table

Logic Inputs			HV MOSFET status					Output
EN	P _{INX}	N _{INX}	P _x	N _x	P _{xG}	N _{xG}	A _{SWx}	H _{VOUTX}
			+HV	-HV	GND	GND	GND	
0	0	0	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	1	OFF	ON	OFF	OFF	OFF	-HV
0	1	0	ON	OFF	OFF	OFF	OFF	+HV
0	1	1	OFF	OFF	ON	ON	ON	GND
1	X	X	OFF	OFF	OFF	OFF	OFF	HiZ

Note:

- x=1~8
- V_{PP} / V_{NN} = +/-HV
- 2-input / channel

6. Drive Current Mode Control

Table 20 Drive Current Mode Control Table

Current Mode	CC1	CC0	I _{OUT} [A] ^{*1}	
			P _x	N _x
1	0	0	0.45	0.45
2	0	1	0.9	0.9
3	1	0	1.35	1.35
4	1	1	1.8	1.8

Note:

*1) Output saturation current @ |V_{ds}|=100V

Recommended current mode is as follows:

- Current mode=4 for high-voltage, short pulse train operations
- Current mode=1~3 for low-voltage, long pulse train or continuous wave operations

HDL6V5583

7. Pin Configuration

Table 21 Pin Configuration

Pin#	Pin Name	I/O	Function
1	N _{IN} 2	I	Input logic control of the output of channel 2
2	P _{IN} 3	I	Input logic control of the output of channel 3
3	N _{IN} 3	I	Input logic control of the output of channel 3
4	P _{IN} 4	I	Input logic control of the output of channel 4
5	N _{IN} 4	I	Input logic control of the output of channel 4
6	V _{LL}	-	Positive voltage supply of low voltage interface (+1.8~5V)
7	CLK	I	Clock Input (100MHz)
8	GND	-	Drive power ground (0V)
9	P _{IN} 5	I	Input logic control of the output of channel 5
10	N _{IN} 5	I	Input logic control of the output of channel 5
11	P _{IN} 6	I	Input logic control of the output of channel 6
12	N _{IN} 6	I	Input logic control of the output of channel 6
13	P _{IN} 7	I	Input logic control of the output of channel 7
14	N _{IN} 7	I	Input logic control of the output of channel 7
15	P _{IN} 8	I	Input logic control of the output of channel 8
16	N _{IN} 8	I	Input logic control of the output of channel 8
17	EN	I	Control of drive output enable, 1=off, 0=on (50kΩ pull-up resistor embedded)
18	CLKEN	I	Control of clock enable, 1=clock disable, 0=clock enable (50kΩ pull-up resistor embedded)
19	NC	-	No connection.
20	ATHP	I	Control of active THP enable, 1=disable, 0=enable (50kΩ pull-down resistor embedded)
21	THP	O	Thermal protection output, open N-MOS drain
22	V _{SS}	-	Negative low voltage power supply (-5V)
23	V _{FP}	-	Built-in floating gate drive power supply for HV P-MOS @FVSEL=1 External floating gate drive power supply for HV P-MOS @FVSEL=0 (V _{PP} -5V)
24	V _{FN}	-	Built-in floating gate drive power supply for HV N-MOS @FVSEL=1 External floating gate drive power supply for HV N-MOS @FVSEL=0 (V _{NN} +5V)
25	V _{NN}	-	Negative high voltage power supply (-100 to 0V)
26	HV _{OUT} 8	O	High voltage output of channel 8

HDL6V5583

Table 21 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
27	V _{PP}	-	Positive high voltage power supply (0 to +100V)
28	HV _{OUT7}	O	High voltage output of channel 7
29	V _{NN}	-	Negative high voltage power supply (-100 to 0V)
30	HV _{OUT6}	O	High voltage output of channel 6
31	V _{PP}	-	Positive high voltage power supply (0 to +100V)
32	HV _{OUT5}	O	High voltage output of channel 5
33	GND	-	Drive power ground (0V)
34	HV _{OUT4}	O	High voltage output of channel 4
35	V _{PP}	-	Positive high voltage power supply (0 to +100V)
36	HV _{OUT3}	O	High voltage output of channel 3
37	V _{NN}	-	Negative high voltage power supply (-100 to 0V)
38	HV _{OUT2}	O	High voltage output of channel 2
39	V _{PP}	-	Positive high voltage power supply (0 to +100V)
40	HV _{OUT1}	O	High voltage output of channel 1
41	V _{NN}	-	Negative high voltage power supply (-100 to 0V)
42	V _{FN}	-	Built-in floating gate drive power supply for HV N-MOS @FVSEL=1 External floating gate drive power supply for HV N-MOS @FVSEL=0 (V _{NN} +5V)
43	V _{FP}	-	Built-in floating gate drive power supply for HV P-MOS @FVSEL=1 External floating gate drive power supply for HV P-MOS @FVSEL=0 (V _{PP} -5V)
44	V _{DD}	-	Positive low voltage power supply (+5V)
45	CC0	I	Control of the least significant bit for drive current mode (50kΩ pull-up resistor embedded)
46	CC1	I	Control of the most significant bit for drive current mode (50kΩ pull-up resistor embedded)
47	FVSEL	I	Control of floating gate drive power supply, 1=built-in, 0=external (50kΩ pull-up resistor embedded)
48	GND	-	Drive power ground (0V)
49	GND	-	Drive power ground (0V)
50	P _{IN1}	I	Input logic control of the output of channel 1
51	N _{IN1}	I	Input logic control of the output of channel 1
52	P _{IN2}	I	Input logic control of the output of channel 2

HDL6V5583

8. Package Outline

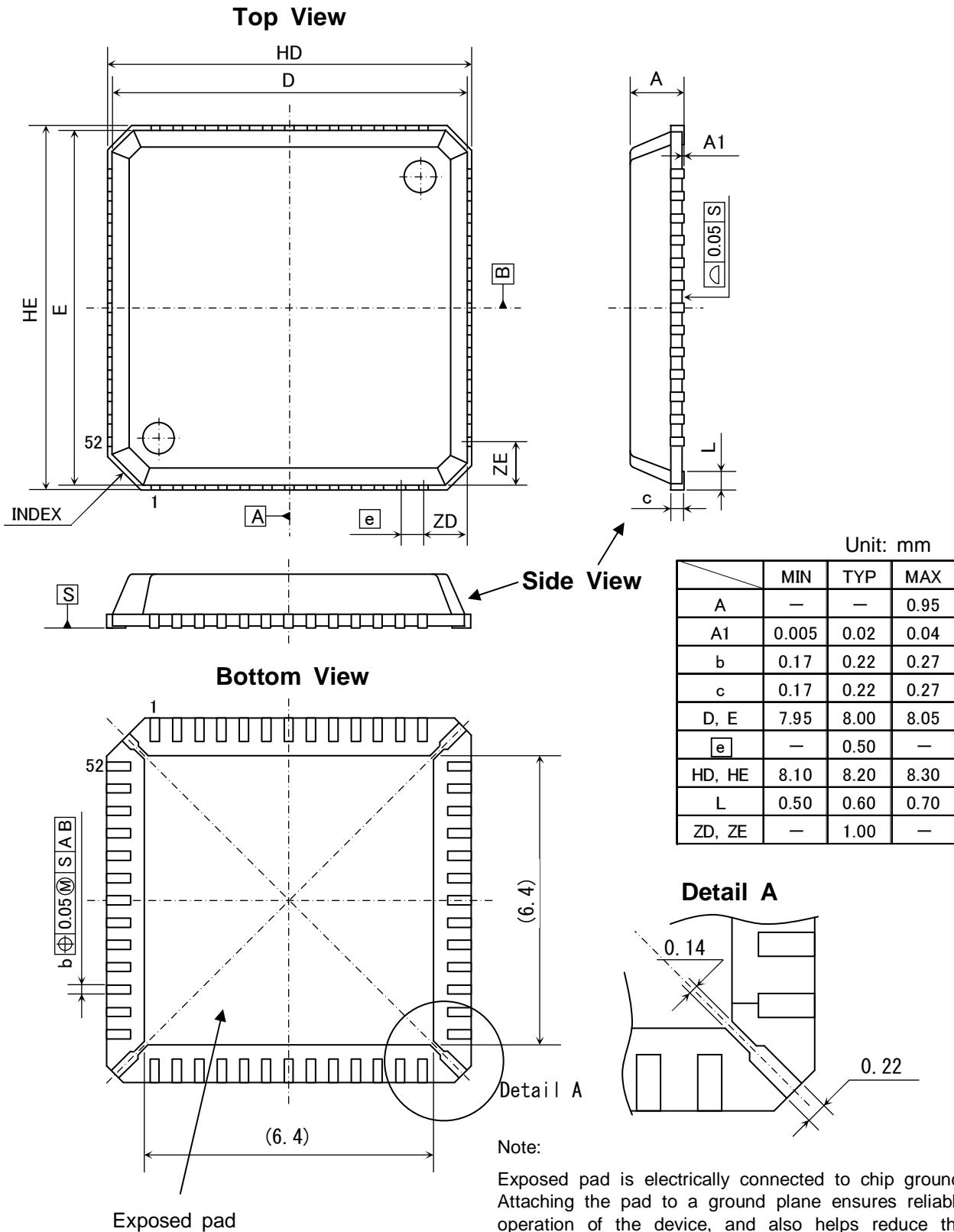


Fig.7 Package Outline (52-Lead QFN Package)

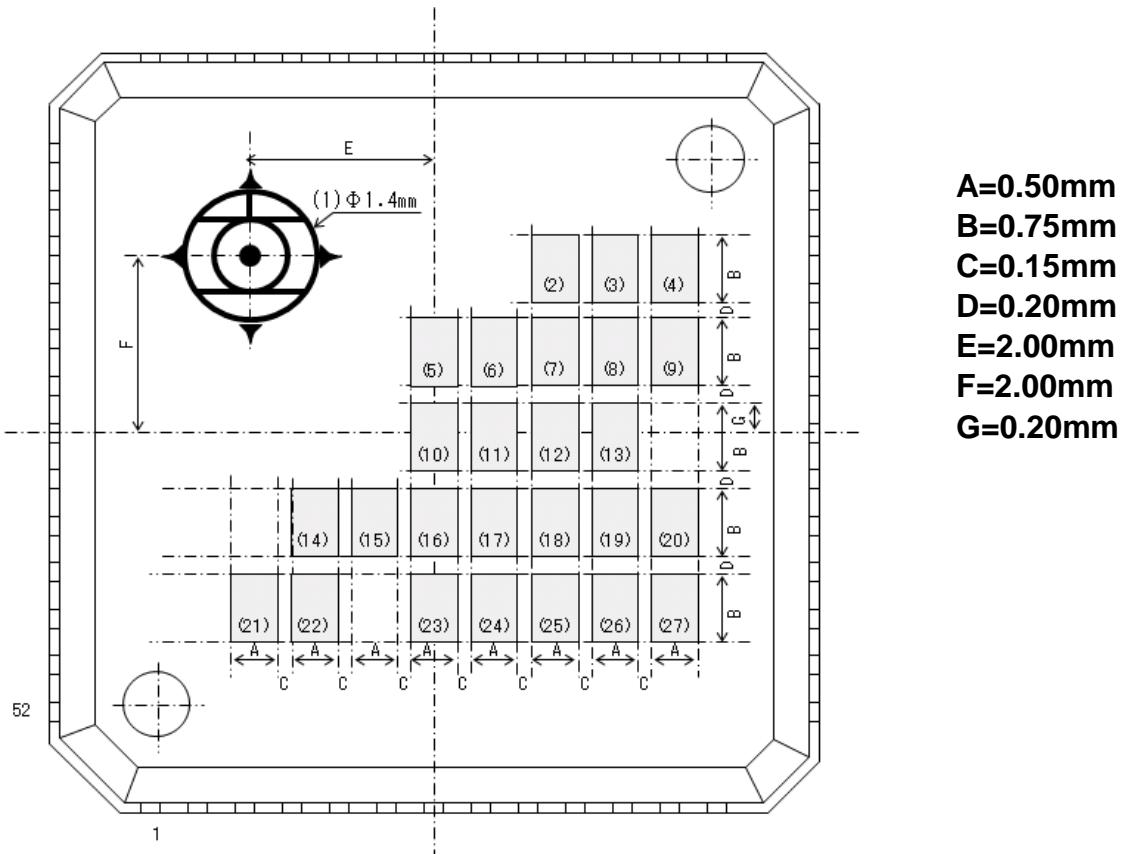
HITACHI

MDD-5583-1.0

Copyright (c)2010, Hitachi Ltd., Micro Device Division All rights reserved.

HDL6V5583

9. Package Marking



No.	Code
(1)	Company logo
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc " I ") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(13)	HDL6V5583 (product name)
(14)~(22)	Quality control code
(23)~(27)	Country of origin

Fig.8 Package Marking

HDL6V5583

10. Transport Media, Quantity

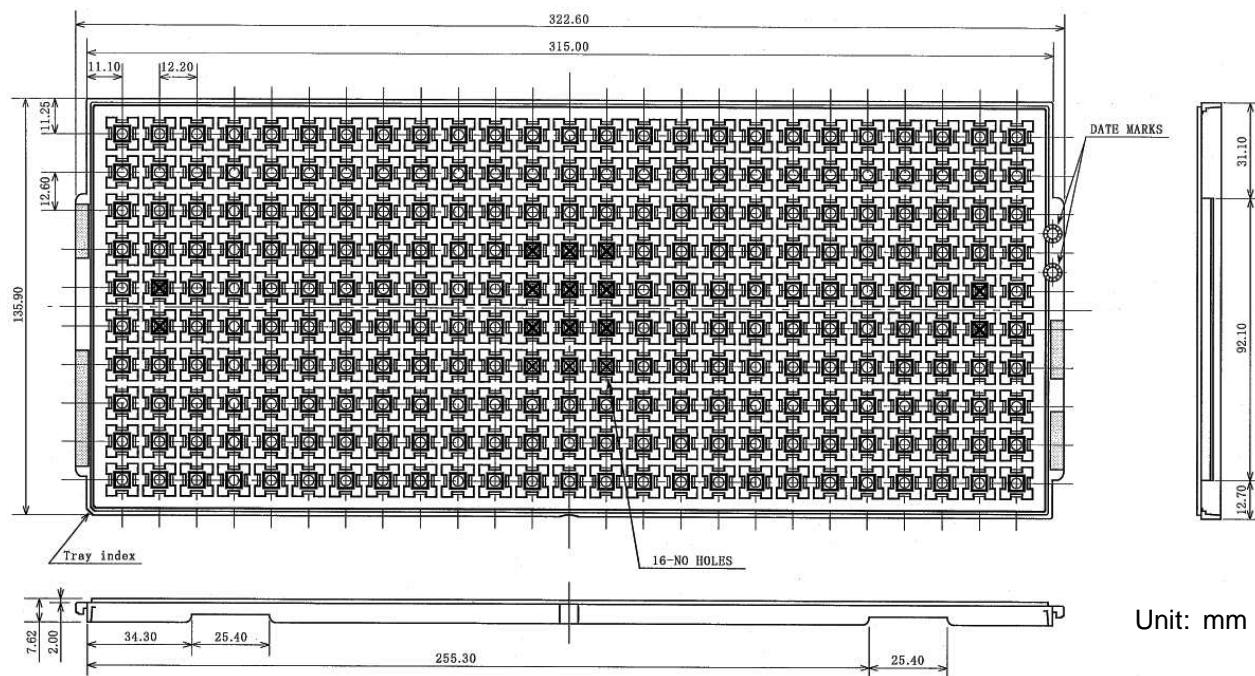


Fig.9 IC Tray Outline

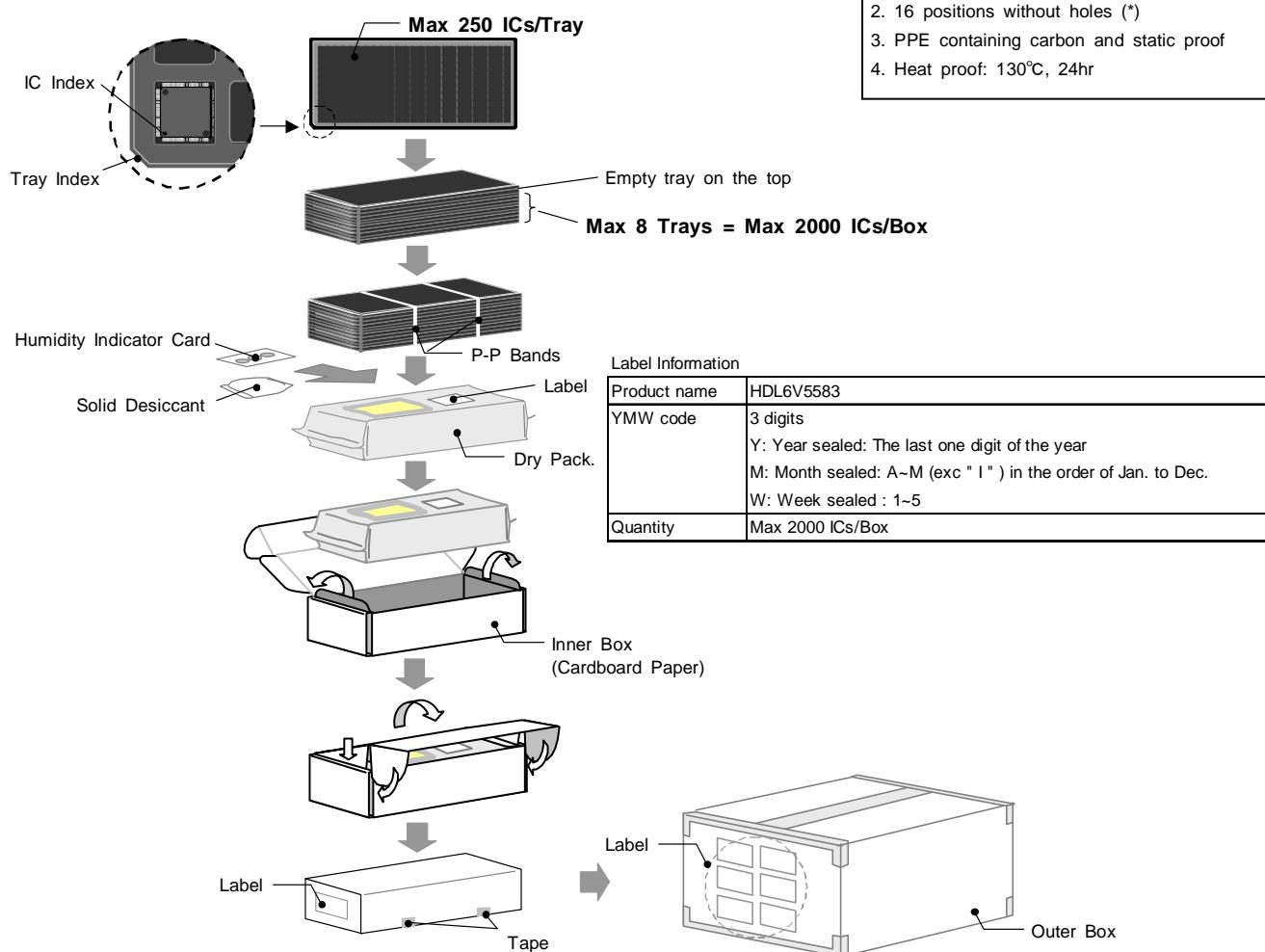


Fig.10 Transport Media, Quantity

HITACHI

 MDD-5583-1.0
 Copyright (c)2010, Hitachi Ltd., Micro Device Division All rights reserved.

HDL6V5583

11. Mounting, Storage

11.1 Mounting Pad Design Example

Unit: mm

HE	8.20
HD	8.20
e	0.50
b3	0.32 ± 0.05
L2	0.55 ± 0.05
L1	0.20 ± 0.05

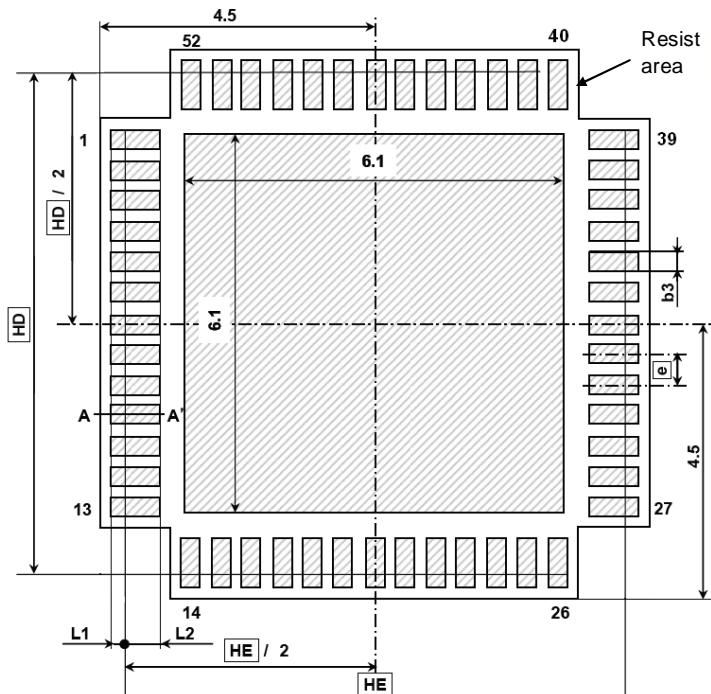


Fig.11 Mounting Pad Design Example

11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35 °C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 °C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking, or within 10 days of total exposure after the second dehumidification.

11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable. IR/Air reflow heating conditions are shown below.

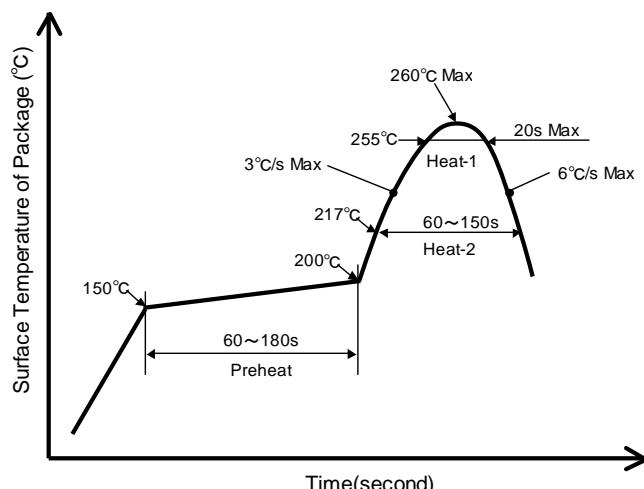


Fig.12 IR/Air Reflow Heating Conditions

HITACHI

MDD-5583-1.0

Copyright (c)2010, Hitachi Ltd., Micro Device Division All rights reserved.

HDL6V5583

12. Inspection

Hundred percent inspections shall be conducted on electrical characteristics.

13. Important Notice

- 13.1 Hitachi warrants performance of its hardware products (hereinafter called "products") to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.
- 13.2 Should any claim be made within one month of product delivery about products' failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.
- 13.3 Hitachi assumes no obligation or any way of compensation should any fault about customer products and applications using Hitachi products be found in marketplace. Only in such a case fault of Hitachi is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.
- 13.4 Hitachi reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.
- 13.5 In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user's units according to the Product Specification. Hitachi assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.
- 13.6 No license is granted by the Product Specification under any patents or other rights of any third party or Hitachi, Ltd.
- 13.7 The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of Hitachi, Ltd.
- 13.8 Resale of Hitachi products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. Hitachi is not responsible or liable for any such statements.
- 13.9 Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

HDL6V5583

14. Cautions

- 14.1 Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
 - 14.1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
 - 14.1.2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.
 - 14.1.3 Those who deal with products should be grounded through a large series impedance around $100\text{k}\Omega$ to $1\text{M}\Omega$.
 - 14.1.4 Prevent friction with other materials made with high polymer.
 - 14.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
 - 14.1.6 Avoid dealing with or storing products in an extremely arid environment.
- 14.2 "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
- 14.3 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
- 14.4 Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
- 14.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. Hitachi, Ltd. assumes no liability for applications assistance, customer product design, or performance.

HDL6V5583

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
04/28/10	0.0	-	-	Initially released as preliminary specification
12/10/10	1.0	1 2 3-4 5-15 22	Front Cover Absolute Max. Ratings App. Circuits Electrical Characteristics Package Marking	Removed Preliminary Added High voltage outputs Added precaution (external HV clamp diodes) Revised specification of DC and AC characteristics Revised package marking
-	-	-	-	-

NOTE: Page numbers in previous versions may differ from the ones in later revisions.