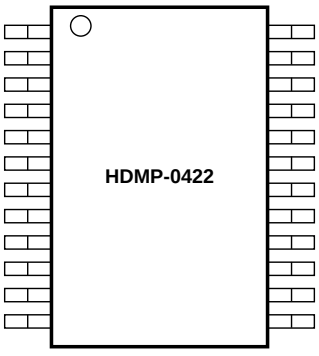
Agilent HDMP-0422
Single Port Bypass Circuit with CDR & Data Valid Detection Capability for Fibre Channel Arbitrated Loops
Data Sheet

Features
- **Supports 1.0625 GBd Fibre Channel operation**
- **Supports 1.25 GBd Gigabit Ethernet (GE) operation**
- **Single PBC/CDR in one package**
- **CDR location determined by choice of cable input/output**
- **Amplitude valid and data valid detection (Fibre channel rate only) on FM_NODE[0] input**
- **Equalizers on all inputs**
- **High-speed LVPECL I/O**
- **Buffered Line Logic (BLL) outputs (no external bias resistors required)**
- **0.46 W typical power at V_{CC} = 3.3 V**
- **24 Pin, low-cost SSOP package**

Applications
- **RAID, JBOD, BTS cabinets**
- **One 2:1 muxes**
- **One 1:2 buffers**
- **1 ≥ N Gigabit serial buffer**
- **N ≥ 1 Gigabit serial mux**



Description

The HDMP-0422 is a Single Port Bypass Circuit (PBC) with Clock and Data Recovery (CDR) capability included. This integrated circuit provides a low-cost, low-power physical-layer solution for Fibre Channel Arbitrated Loop (FC-AL) disk array configurations. By using a PBC such as the HDMP-0422, hard disks may be pulled out or swapped while other disks in the array are available to the system.

A PBC consists of multiple 2:1 multiplexers daisy chained along with a CDR. Each port has two modes of operation: "disk in loop" and "disk bypassed." When the "disk in loop" mode is selected, the loop goes into and out of the disk drive at that port. For example, data goes from the HDMP-0422's TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC's (e.g. an HDMP-1636A) Rx differential input pins. Data from the Disk Drive Transceiver IC's Tx differential outputs goes to the HDMP-0422's FM_NODE[n]± differential input pins. Figures 2 and 3 show connection diagrams for disk drive array applications.

When the "disk bypassed" mode is selected, the disk drive is either absent or non-functional and the loop bypasses the hard disk.

The "disk bypassed" mode is enabled by pulling the BYPASS[n]- pin low. Leave BYPASS[n]- floating to enable the "disk in loop" mode. HDMP-0422s may be cascaded with other members of the HDMP-04XX/HDMP-05XX family through the appropriate FM_NODE[n]± and TO_NODE[n]± pins to accommodate any number of hard disks (see Figure 4). The unused cells in the HDMP-0422 may be bypassed by using pulldown resistors on the BYPASS[n]- pins for these cells.

An HDMP-0422 may also be used as two 1:1 buffers, one with a CDR and one without. For example, an HDMP-0422 may be placed in front of a CMOS ASIC to clean the jitter of the outgoing signal (CDR path) and to better read the incoming signal (non-CDR paths). In addition, the HDMP-0422 may be configured as one 2:1 multiplexers or as one 1:2 buffers.

CAUTION: *As with all semiconductor ICs, it is advised that normal static precautionsb be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).*

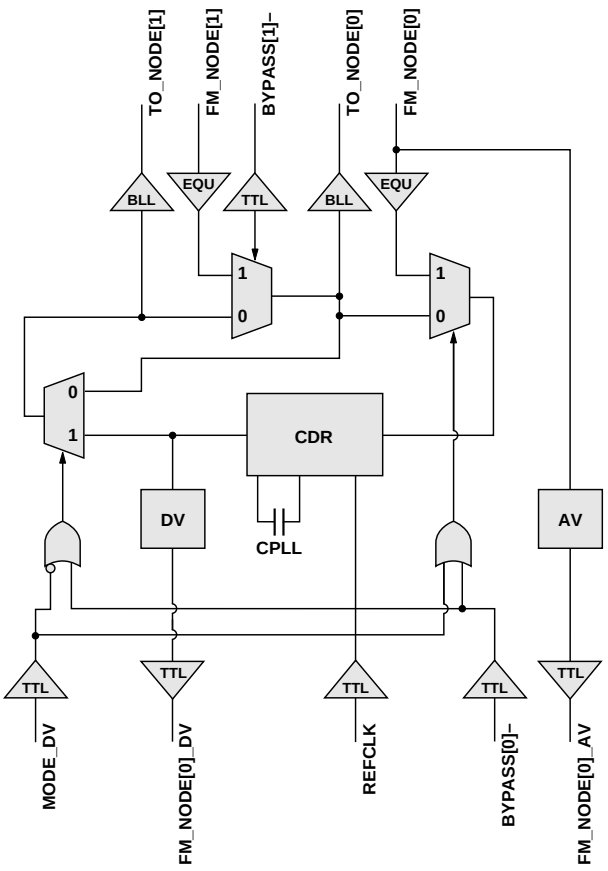


Figure 1. Block diagram of HDMP-0422.

The HDMP-0422 design allows for CDR placement at any location with respect to a hard disk slot. For example, if hard disk A is connected to PBC cell 1, while BYPASS[0]- is left to float high (see Figure 2), the CDR function will be performed before entering the hard disk at slot A. To obtain a CDR function after slot A (see Figure 3), connect hard disk A to PBC cell 0, while floating BYPASS[1]- high. Refer to Table 1 for both pin connections.

CDR

The Clock and Data Recovery (CDR) block is responsible for frequency and phase locking onto the incoming serial data stream and resampling the incoming data based on the recovered clock. An automatic locking feature allows the CDR to lock onto the input data stream without external training controls. It does this by continually frequency locking onto the 106.25 MHz reference clock (REFCLK) and then phase locking onto the input data stream. Once bit locked, the CDR generates a high-speed sampling clock. This clock is used to sample or repeat the incoming data to produce the CDR output. The CDR jitter specifications listed in this data sheet assume an input that has been 8B/10B encoded. The CDR will also lock onto data encoded using other algorithms as long as there is DC balance and a sufficient number of transitions.

REFCLK INPUT

The LVTTL REFCLK input provides a reference oscillator for frequency acquisition of the CDR. The REFCLK frequency should be within ± 100 ppm of one-tenth of the incoming data rate in baud (106.25 MHz ± 100 ppm for FC-AL running at 1.0625 GBd).

BLL OUTPUT

All TO_NODE[n]± high-speed differential outputs are driven by a Buffered Line Logic (BLL) circuit that has on-chip source termination, so no external bias resistors are required. The BLL Outputs on the HDMP-0422 are of equal strength and can drive lengthy FR-4 PCB trace.

Unused outputs should not be left unconnected. Ideally, unused outputs should have their differential pins shorted together with a short PCB trace. If longer traces or transmission lines are connected to the output pins, the lines should be differentially terminated with an appropriate

resistor. The value of the termination resistor should match the PCB trace differential impedance.

EQU INPUT

All FM_NODE[n]± high-speed differential inputs have an Equalization (EQU) buffer to offset the effects of skin loss and dispersion on PCBs. An external termination resistor is required across all high-speed inputs. The value of the termination resistor should match the PCB trace differential impedance. Alternatively, instead of a single resistor, two resistors in series, with an AC ground between them, can be connected differentially across the FM_NODE[n]± inputs. The latter configuration attenuates high-frequency common mode noise.

BYPASS[n]- INPUT

The active low BYPASS[n]- inputs control the data flow through the HDMP-0422. All BYPASS pins are LVTTL and contain internal pull-up circuitry. To bypass a port, the appropriate BYPASS[n]- pin should be connected to GND through a 1 kΩ resistor. Otherwise, the BYPASS[n]- inputs should be left to float, as the internal pull-up circuitry will force them high.

FM_NODE[0]_DV OUTPUT

The Data Valid (DV) block detects if the incoming data at FM_NODE[0]± is valid Fibre Channel data. The DV block checks for sufficient K28.5+ characters (per Fibre Channel framing rules) and for run length violations (per 8B/10B encoding) on the data coming out of the CDR.

The FM_NODE[0]_DV output is pulled low if a run length violation (RLV) occurs, or if there are no commas detected (NCD) over a specific time interval. It is pulled high if no errors are detected.

A RLV error is defined as any consecutive sequence of 1s or 0s greater than five in the serial bit stream. An NCD error indicates the absence of the seven-bit pattern (0011111) present in the positive disparity comma (K28.5+) character. A K28.5+ character should occur at the beginning of every Fibre Channel frame of 2148 bytes (or 21480 serial bits), as well as many times within and between frames. If this seven-bit pattern is not found within a 215 bit (~31 µs) interval, an NCD error is generated. A counter within the chip tracks the 2^{15} bit intervals.

Any RLV and NCD errors are stored during the 2^{15} bit interval. The FM_NODE[0]_DV output is pulled low at the start of the 2^{15} bit interval after errors are detected. Once low, FM_NODE[0]_DV remains in that state until an entire 2^{15} bit interval has no RLV or NCD errors. At the start of the 2^{15} bit interval subsequent to no RLV or NCD errors being detected, FM_NODE[0]_DV is pulled high.

MODE_DV INPUT

The active high Data Valid Mode input selects Fibre Channel data checking of the FM_NODE[0]± inputs. This is accomplished by having MODE_DV override the BYPASS[0]- control (see Figure 1), thereby forcing the data into the CDR to come from the FM_NODE[0]± inputs. The MODE_DV pin is an LVTTL input and contains internal pull-up circuitry. To select Data Valid Mode, float MODE_DV high. Otherwise, MODE_DV should be connected to GND through a 1 kΩ resistor.

When MODE_DV is high, the user is able to use the BYPASS[0]- input to bypass invalid Fibre Channel data from the rest of the loop. For example, if FM_NODE[0]_DV is connected to the BYPASS[0]- input, data from the CDR will only be routed to TO_NODE[1]± if the data has no RLV or NCD errors. If the DV block detects errors, the signal at TO_NODE[0]± will be routed to the TO_NODE[1]± outputs (see Figure 5).

FM_NODE[0]_AV OUTPUT

The Amplitude Valid (AV) block detects if the incoming data on FM_NODE[0]± is valid by examining the differential amplitude of that input. The incoming data is considered valid, and FM_NODE[0]_AV is driven high, as long as the amplitude is greater than 400 mV (differential peak-to-peak). FM_NODE[0]_AV is driven low as long as the amplitude of the input signal is less than 100 mV (differential peak-to-peak). When the amplitude of the input signal is between 100-400 mV (differential peak-to-peak), the FM_NODE[0]_AV output is undefined.

Table 1. Pin Connection Diagram to Achieve Desired CDR Location
(see Figures 2, 3)

Hard Disks	A	A
Connection to PBC cells	1	0
CDR position (x)	xA	Ax
Cell connected to Cable	0	1

x denotes CDR position with respect to hard disks.

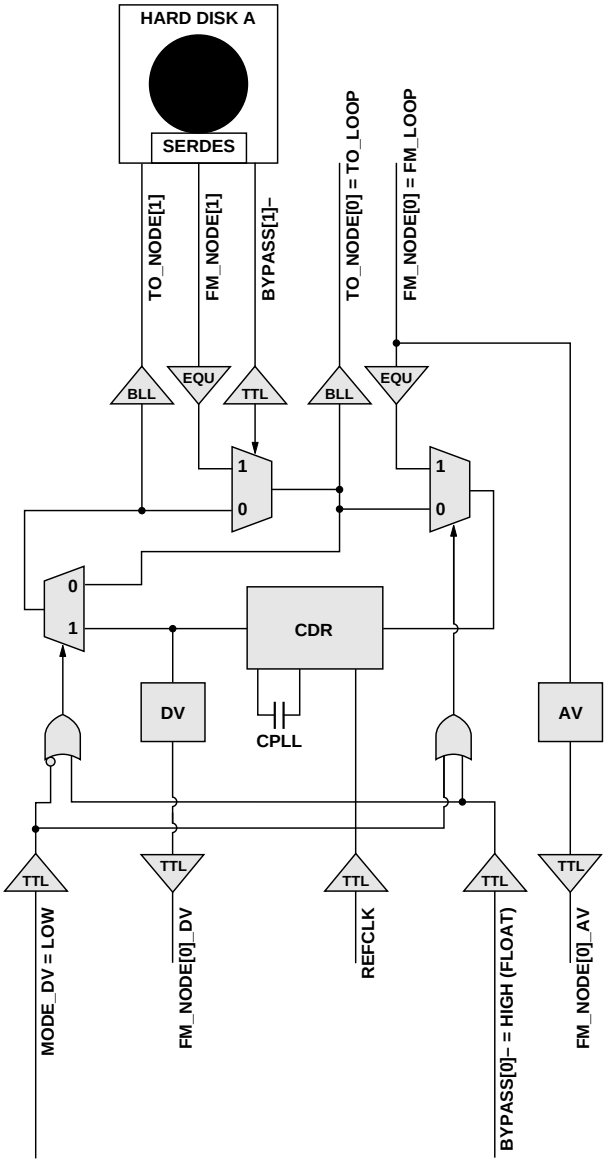


Figure 2. Connection diagram for CDR at first cell.

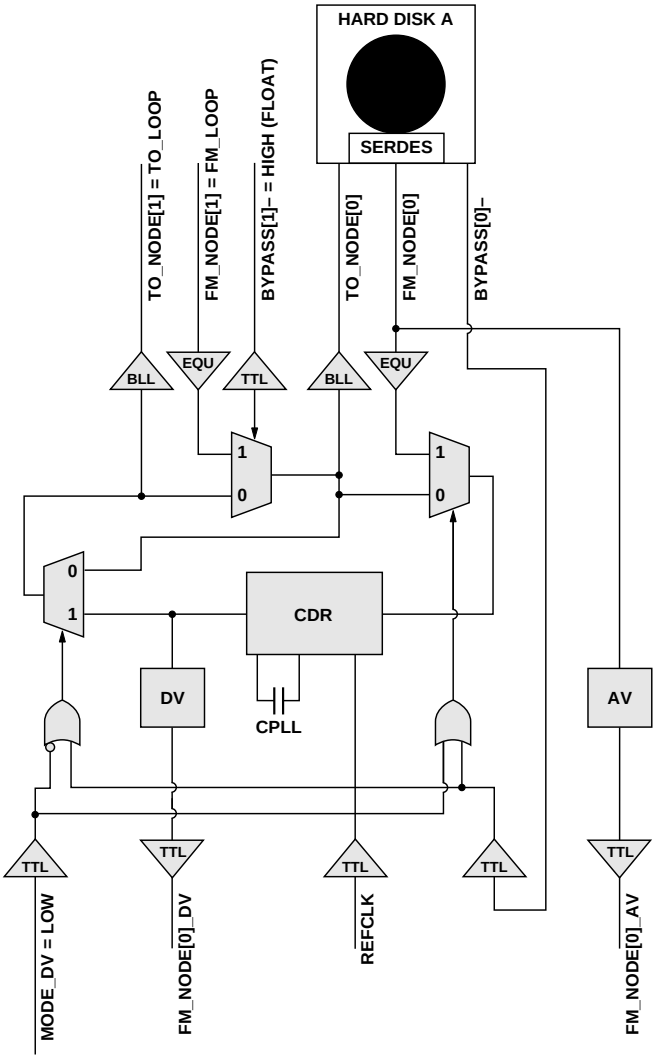


Figure 3. Connection diagram for CDR at last cell.

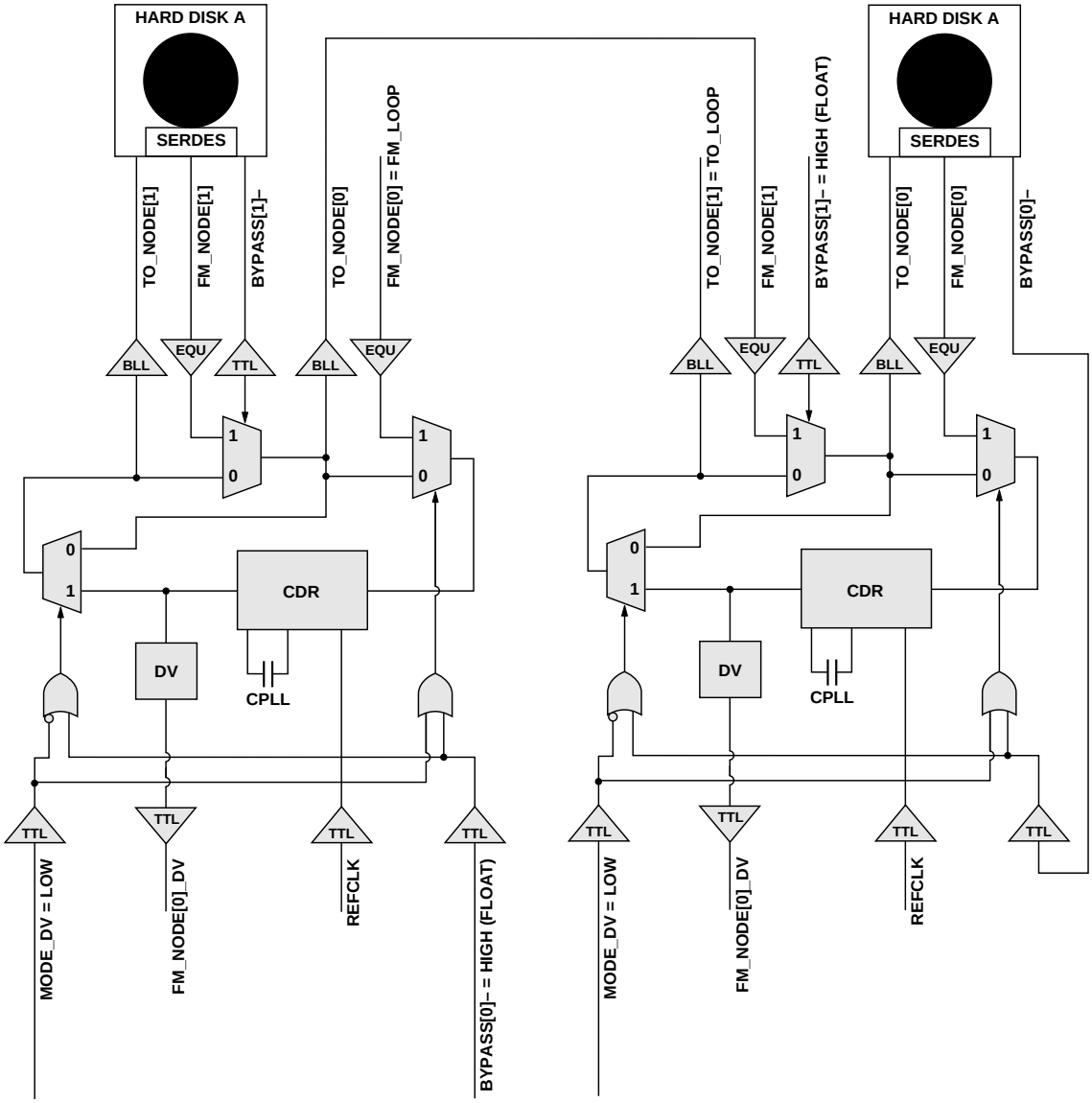


Figure 4. Connection diagram for multiple HDMP-0422s.

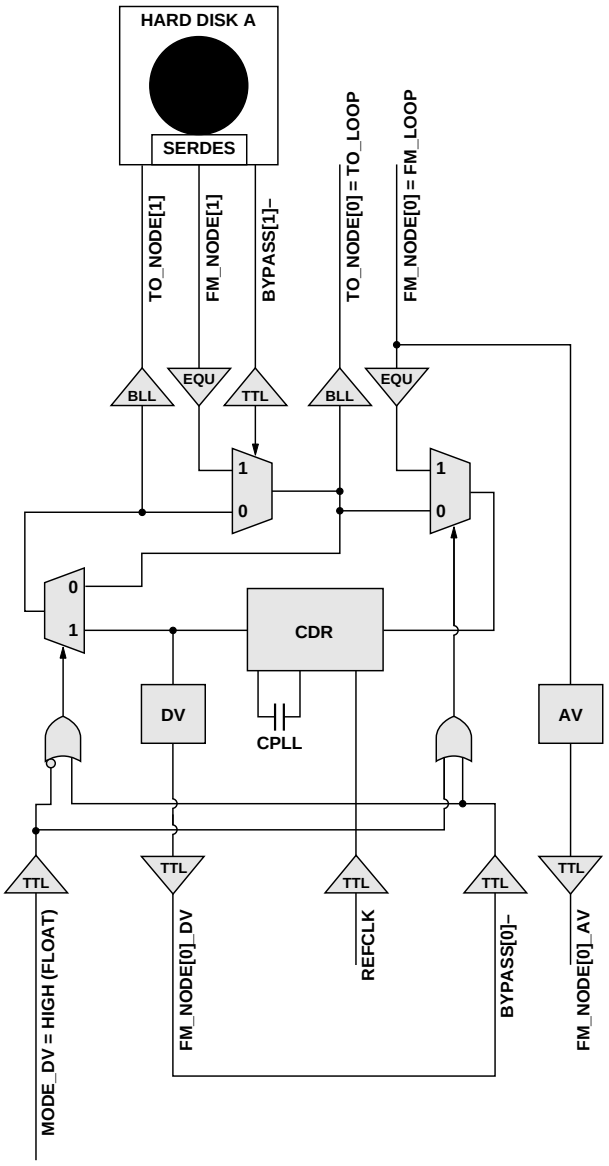


Figure 5. Connection diagram for bypassing invalid Fibre Channel data.

I/O Type Definitions

I/O Type	Definition
I-LVTTL	LVTTL Input
O-LVTTL	LVTTL Output
HS_OUT	High Speed Output, LVPECL compatible
HS_IN	High Speed Input
C	External Circuit Node
S	Power Supply or Ground

Pin Definitions

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+ TO_NODE[0]- TO_NODE[1]+ TO_NODE[1]-	20 21 05 04	HS_OUT	**Serial Data Outputs:** High-speed outputs to a hard disk drive or to a cable.
FM_NODE[0]+ FM_NODE[0]- FM_NODE[1]+ FM_NODE[1]-	23 24 02 01	HS_IN	**Serial Data Inputs:** High-speed inputs from a hard disk drive or from a cable.
BYPASS[0]- BYPASS[1]-	17 08	I-LVTTL	**Bypass Inputs:** For "disk bypassed" mode, connect BYPASS[n]- to GND through a 1 kΩ resistor. For "disk in loop" mode, float HIGH.
REFCLK	14	I-LVTTL	**Reference Clock:** A user-supplied clock reference used for frequency acquisition in the Clock and Data Recovery (CDR) circuit.
CPLL1 CPLL0	12 13	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal Clock and Data Recovery (CDR) circuit must be connected across the CPLL1 and CPLL0 pins. Recommended value is 0.1 μF.
FM_NODE[0]_DV	09	O-LVTTL	**Data Valid:** Indicates Fibre Channel compliant data on FM_NODE[n] ± inputs when HIGH. Indicates either a run length violation or a no comma detected error when LOW.
MODE_DV	11	I-LVTTL	**Data Valid Mode:** To allow data valid detection, float MODE_DV HIGH. Otherwise, connect to GND through a 1 kΩ resistor.
FM_NODE[0]_AV	16	O-LVTTL	**Amplitude Valid:** Indicates acceptable signal amplitude on the FM_NODE[n]± inputs. If (FM_NODE[n]+ – FM_NODE[n]-) >= 400 mV peak-to-peak, FM_NODE[0]_AV = 1 If 400 mV > (FM_NODE[n]+ – FM_NODE[n]-) > 100 mV, FM_NODE[0]_AV = undefined If 100 mV >= (FM_NODE[n]+ – FM_NODE[n]-), FM_NODE[0]_AV = 0
GND	06 07 18 19	S	**Ground:** Normally 0 V. See Figure 13 for Recommended Power Supply Filtering.
$V_{CC}A$	15	S	**Analog Power Supply:** Normally 3.3 V. Used to provide a clean supply to the Clock and Data Recovery (CDR) circuit. See Figure 13 for Recommended Power Supply Filtering.
$V_{CC}HS[0]$ $V_{CC}HS[1]$	22 03	S S	**High Speed Supply:** Normally 3.3 V. Used only for high-speed outputs (TO_NODE[n]). See Figure 13 for Recommended Power Supply Filtering.
V_{CC}	10	S	**Logic Power Supply:** Normally 3.3 V. Used for internal logic. See Figure 13 for Recommended Power Supply Filtering.

Absolute Maximum Ratings

T_A = 25ºC, except as specified. Operation in excess of any of these conditions may result in permanent damage to this device. Continuous operation at these minimum or maximum ratings is not recommended.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.5	4.0
$V_{IN,LVTTL}$	LVTTL Input Voltage	V	–0.5	V_{CC} + 0.5[1]
V_{IN,HS_IN}	HS_IN Input Voltage (Differential)	mV	200	2000
$I_{O,LVTTL}$	LVTTL Output Sink/Source Current	mA		±13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125

Note:

1. Must remain less than or equal to absolute maximum V_{CC} voltage of 4.0 V.

DC Electrical Specifications

V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	V	2.0		
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	V			0.8
$V_{OH,LVTTL}$	LVTTL Output High Voltage Range, I_{OH} = -400 µA	V	2.2		V_{CC}
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA			40
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA			–600
I_{CC}	Total Supply Current, T_A = 25°C	mA		140	

AC Electrical Specifications

V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Min.	Typ.	Max.
T_{LOOP_LAT}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	ns		3.0	
T_{CELL_LAT}	Per Cell Latency from FM_NODE[1] to TO_NODE[0]	ns		2.0	
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	ns		2.0	
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	ns		2.0	
$t_{r,LVTTLout}$	Output TTL Rise Time, 0.8 V to 2.0 V, 10 pF Load	ns		1.7	3.3
$t_{f,LVTTLout}$	Output TLL Fall Time, 2.0 V to 0.8 V, 10 pF Load	ns		1.7	2.4
t_{rs,HS_OUT}	HS_OUT Single-Ended Rise Time, 20% to 80%	ps		200	300
t_{fs,HS_OUT}	HS_OUT Single-Ended Fall Time, 20% to 80%	ps		200	300
t_{rd,HS_OUT}	HS_OUT Differential Rise Time, 20% to 80%	ps		200	300
t_{fd,HS_OUT}	HS_OUT Differential Fall Time, 20% to 80%	ps		200	300
V_{IP,HS_IN}	HS_IN Required Pk-Pk Differential Input Voltage	mV	200	1200	2000
V_{OP,HS_OUT}	HS_OUT Pk-Pk Differential Output Voltage (Z0 = 75 Ω, Figure 10)	mV	1100	1400	2000

Guaranteed Operating Rates

V_{CC} = 3.15 V to 3.45 V.

FC Serial Clock Rate (MBd)		GE Serial Clock Rate (MBd)	
Min.	**Max.**	**Min.**	**Max.**
1,040	1,080	1,240	1,260

CDR Reference Clock Requirements

V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Min.	Typ.	Max.
f	Nominal Frequency (Fibre Channel)	MHz		106.25	
f	Nominal Frequency (Gigabit Ethernet)	MHz		125	
F_{tol}	Frequency Tolerance	ppm	–100		+100
Symm	Symmetry (Duty Cycle)	%	40		60

Locking Characteristics

V_{CC} = 3.15 V to 3.45 V.

Parameter	Units	Max.
Bit Sync Time (phase lock)	bits	2500
Frequency Lock at Powerup	µs	500

Output Jitter Characteristics

V_{CC} = 3.15 V to 3.45 V.

Symbol	Parameter	Units	Typ.	Max.
RJ[1]	Random Jitter at TO_NODE pins (1 sigma rms)	ps	5	
DJ[1]	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	20	

Note:

1. Please refer to Figures 7 and 8 for jitter measurement setup information.

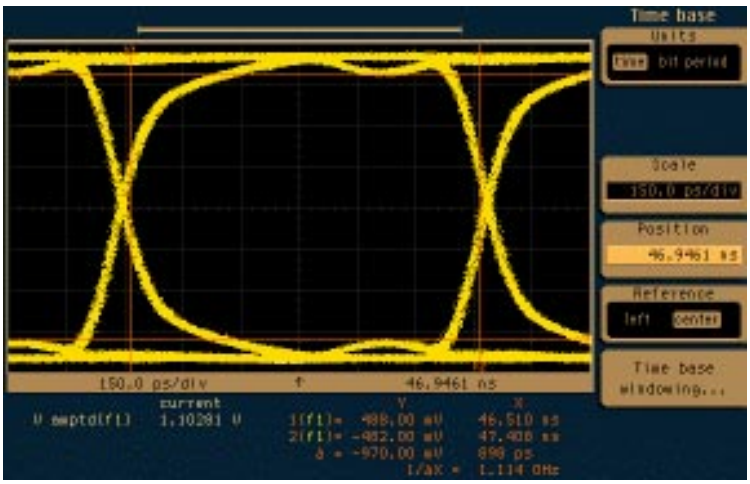


Figure 6. Eye diagram of TO_NODE[1]± high speed differential output (50 Ω termination).

Note: Measurement taken with a 2^7-1 PRBS input to FM_NODE[0]±

Jitter Measurement Configurations

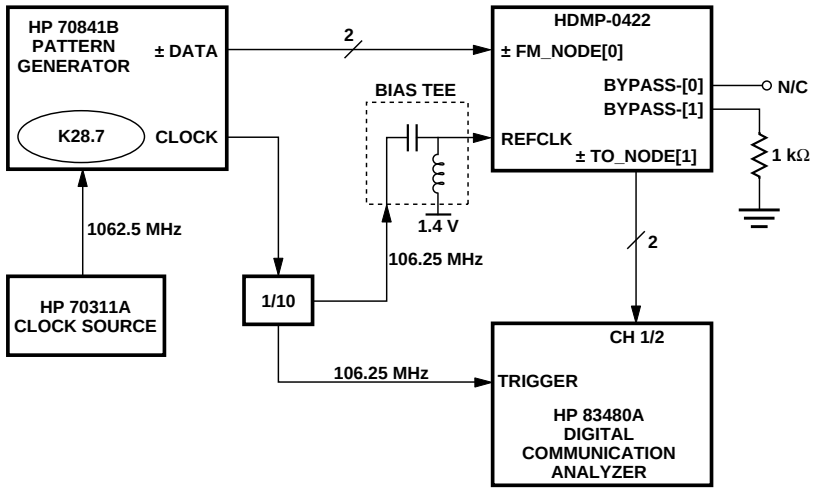


Figure 7. Setup for measurement of Random Jitter.

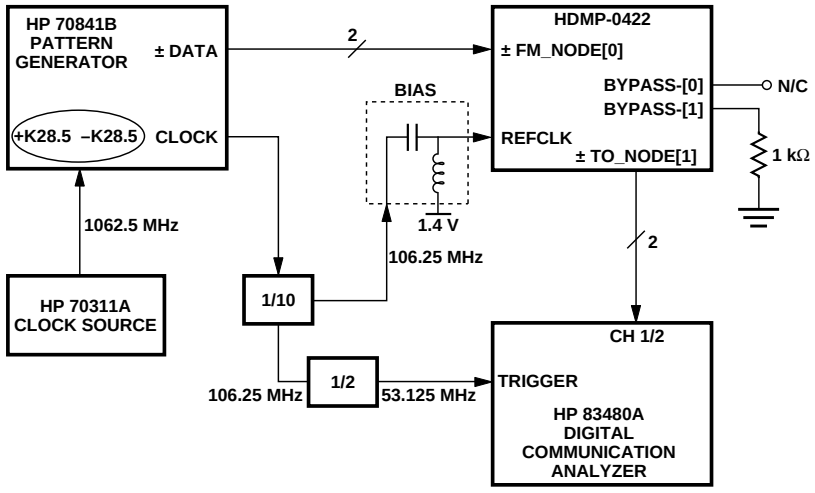


Figure 8. Setup for measurement of Deterministic Jitter.

Simplified I/O Cells

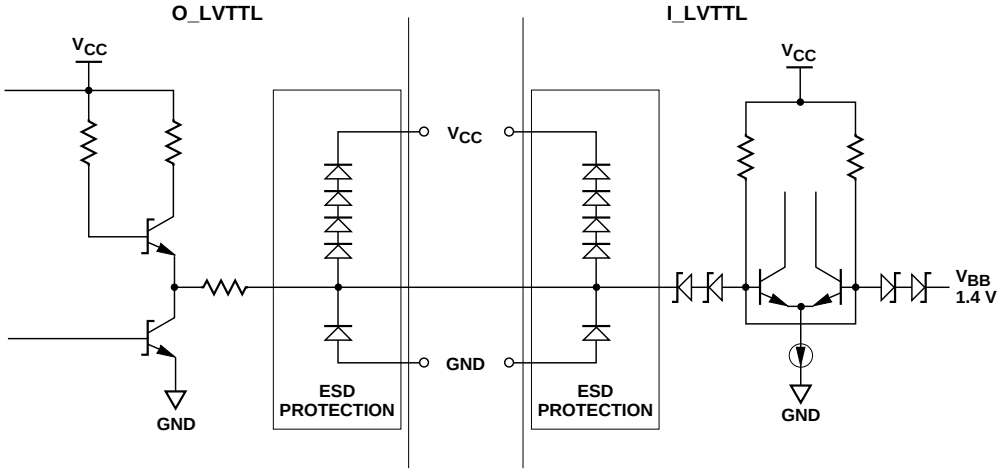
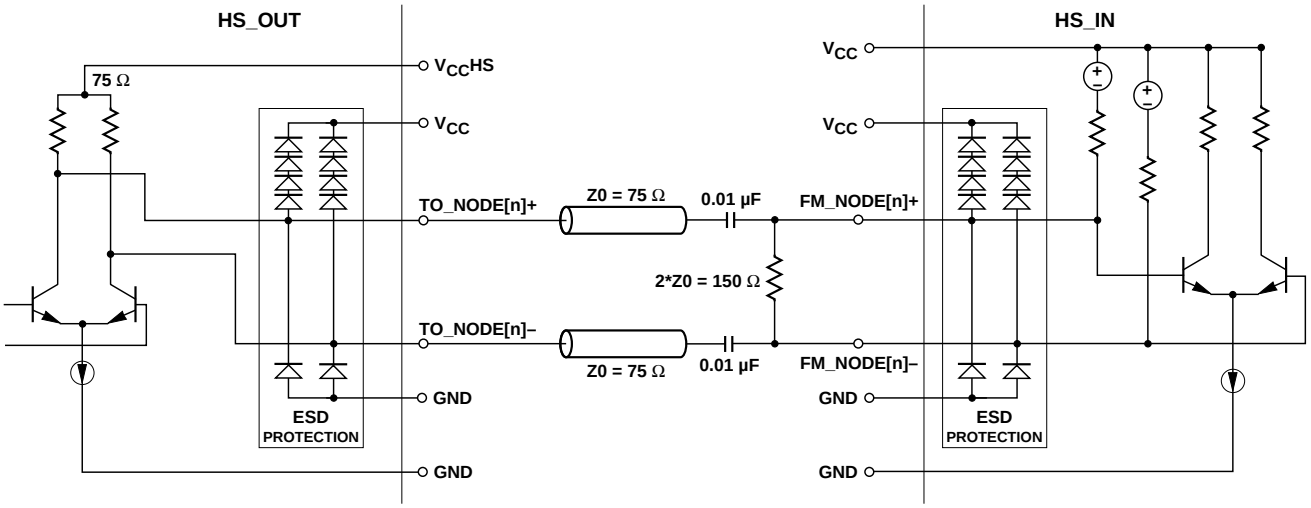


Figure 9. O-LVTTL and I-LVTTL simplified circuit schematic.



NOTE:
1. FM_NODE[n] INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.

Figure 10. HS_OUT and HS_IN simplified circuit schematic.

Package Information

Power Dissipation and Thermal Resistance. V_{CC} = 3.15 V to 3.45 V.

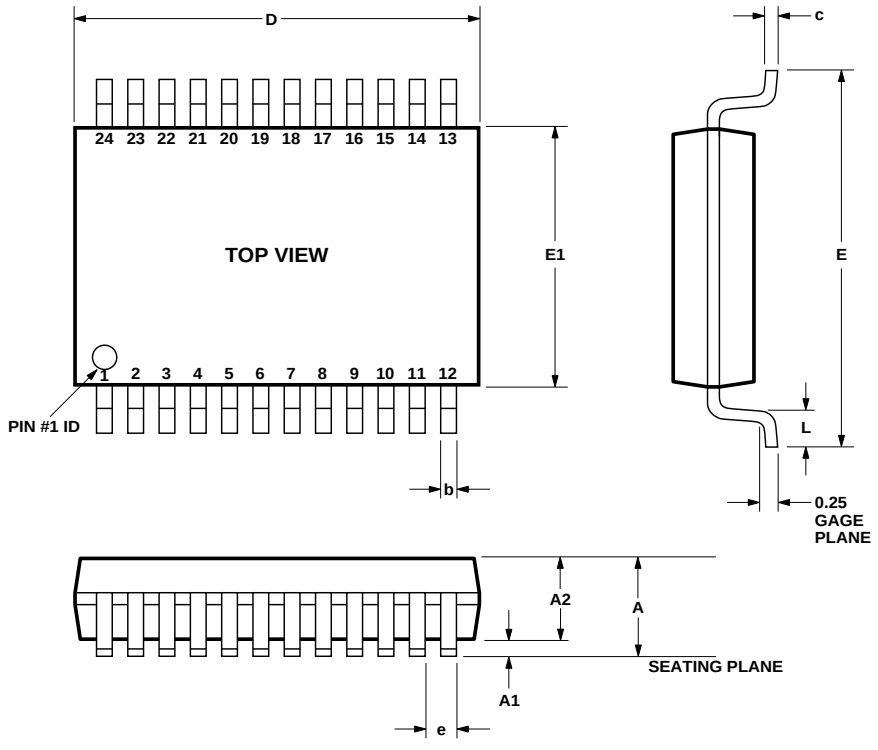
Symbol	Parameter	Units	Typ.	Max.
P_D	Power Dissipation	mW	460	
Θ_{jc}[1]	Thermal Resistance, Junction to Case	°C/W	14	

Note:

1. Based on independent package testing by Agilent. Θ_{ja} for this device is 57°C/W. Θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following equation: $T_j = T_C + (\Theta_{ja} \times P_D)$, where T_C is the case temperature measured on the top center of the package and P_D is the power being dissipated.

Item	Details
Package Material	Plastic Shrink Small Outline (SSOP) Per JESD Pub 95, MO-150, Var AG
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	200-800 micro-inches
Lead Skew	0.15 mm max
Lead Coplanarity (Seating Plane)	0.10 mm max

Mechanical Dimensions

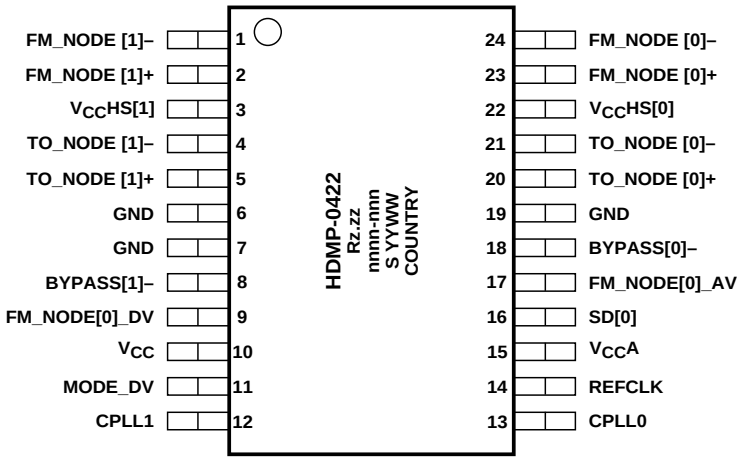


DIMENSION	E1	D	E	b	e	L	c	A2	A1	A
HDMP-0422	5.30	8.20	7.80	0.22/ 0.38	0.65	0.90	0.09/ 0.20	1.75	0.05/ 0.25	2.13
TOLERANCE	±0.30	±0.30	±0.40	MIN./ MAX.	BSC	+0.13/ –0.27	MIN./ MAX.	±0.13	MIN./ MAX.	MAX.

ALL DIMENSIONS ARE IN MILLIMETERS

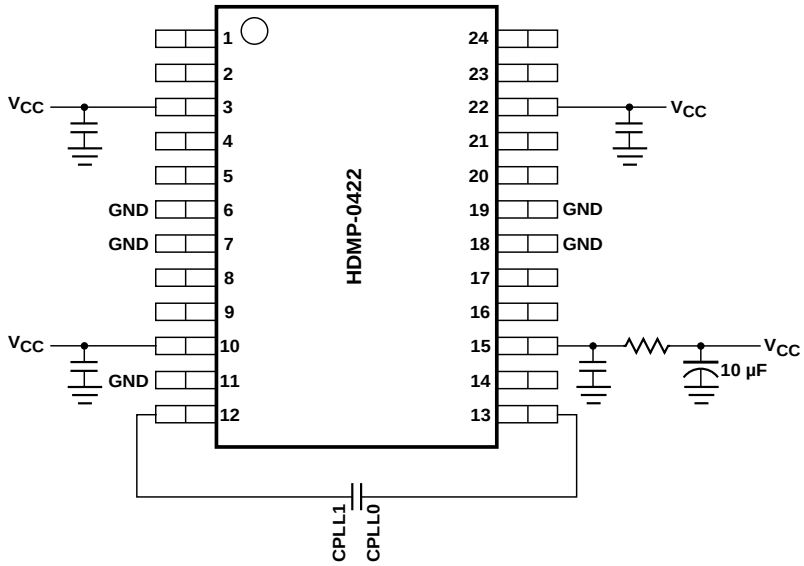
Figure 11. HDMP-0422 package drawing.

Pin Diagram and Recommended Supply Filtering



nnnn-nnn = WAFER LOT – BUILD NUMBER
Rz.zz = DIE REVISION
S = SUPPLIER CODE
YYWW = DATE CODE (*YY* = YEAR, *WW* = WORK WEEK)
COUNTRY = COUNTRY OF MANUFACTURE

Figure 12. HDMP-0422 package layout and marking, top view.



CAPACITORS = 0.1 µF, RESISTOR = 10 Ω (EXCEPT WHERE NOTED).

Figure 13. Recommended power supply filtering.

www.agilent.com/semiconductors

For product information and a complete list of distributors, please go to our web site.

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Data subject to change.

Obsoletes 5988-8561EN

June 17, 2003

5988-9759EN

Agilent Technologies