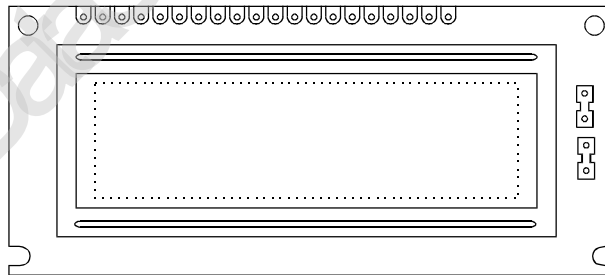


**HANTRONIX**

**PRODUCT SPECIFICATION**

**HDM32GS12-1**

122 x 32 GRAPHICS  
LCD DISPLAY MODULE



<b>HANTRONIX, INC.</b> 10080 BUBB RD. CUPERTINO, CA 95014	Q.A.:	REV.:	<b>HDM32GS12-1</b>	SHEET 1 OF 7
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■ Absolute Maximum Ratings

Parameter	Symbol	Rated Values	Unit
Supply voltage(1)	VSS	-8.0~-0.3	V
Supply voltage(2)	V5	-16.5~0.3	V
Supply voltage(3)	V1,V4,V2,V3	V5~0.3	V
Input voltage	V1	VSS-0.3~0.3	V
Output voltage	VO	VSS-0.3±0.03	V
Permissible loss	PD	250	m v
Operating temperature	T <sub>opr</sub>	0~+50	°C
Storage temperature	T <sub>sth</sub>	-20~+60	°C
Solder temperature	T <sub>ol</sub>	260 °C for ~ 3s	—

■ Pin Description

Pin Name	Function
DB0~DB7	Data input
A0	Selects display data or instructions. HIGH:Display data. LOW:instructions.
RES	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH:68-port MPU interface. LOW:80-port MPU interface.
CS	Chip Select input. LOW:Active level sensing.
E (RD)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/W (WR)	Read/Write Select signal when a 68-port MPU is connected. HIGH:Read Select LOW:Write Select (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input(only effective with external clock types).
VDD	5V power supply.
VSS	0V power supply (GND level).
VO	VO=-5V contrast adjustment.

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**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

(VDD=0V, Ta=-20to75°C)

Parameter	Symbol	Condition	Applicable Terminals	Min	Typ	Max	Unit		
Operating voltage (1)*1	Recommended operation	VSS	VSS	-5.5	-5.0	-4.5	V		
	Potential operation			-7.0	—	-2.4			
Operating voltage (2)	Recommended operation	V5	V5	-13.0	—	-3.5	V		
	Potential operation			-13.0	—	—			
	Potential operation	V1, V2	V1, V2	0.6×V5	—	VDD			
	Potential operation	V3, V4	V3, V4	V5	—	0.4×VDD			
HIGH input voltage	VIHT		A0, D0~D7, E, R/W, CS pins	VSS+2.0	—	VDD	V		
	VIHC		CL, FR, M/S, RES pins	0.2×VSS	—	VDD			
LOW input voltage	VILT		A0, D0~D7, E, R/W, CS pins	VSS	—	VSS+0.8	V		
	TILC		CL, FR, M/S, RES pins	VSS	—	0.8×VSS			
HIGH output voltage	VOHT	IOH=-3.0 mA	D0~D7 pins	VSS+2.4	—	—	V		
	VOHC1	IOH=-2.0 mA	FR pins	VSS+2.4	—	—			
	VOHC2	IOH=-120 μA	OSC2	0.2×VSS	—	—			
LOW output voltage	VOLT	IOL=3.0 mA	D0~D7, FR pins	—	—	VSS+0.4	V		
	VOLC1	IOL=2.0 mA	FR pins	—	—	VSS+0.4			
	VOLC2	IOL=120 μA	OSC2	—	—	0.8×VSS			
Input leak current	ILI		A0, E, R/W, CS, CL, RES, M/S pins	-1.0	—	1.0	μA		
Output leak current	ILO	Applicable when FR is in a high-impedance state	D0~D7, FR pins	-3.0	—	3.0			
LCD driver ON resistance	RON	Ta=25°C	V5=-5.0V	SEG0~60	—	5.0	7.5	kΩ	
		V5=-3.5V	COM0~15	—	10.0	50.0			
Static current consumption	IDDO	CS=CL=VDD		—	0.05	1.0	μA		
Active current consumption	External CLK	IDD(1)	During display	VDD	IcL=2kHz	—		2.0	5.0
	Oscillator				Ri=1MΩ	—		9.5	15.0
					IcL=18kHz	—		5.0	10.0
	IDD(2)	During access t <sub>acc</sub> =200kHz			—	300	500		
Input terminal capacity	CIN	Ta=25°C, f=1MHz	All input terminals	—	5.0	8.0	pF		
Oscillating frequency	fosc	Ri=1.0MΩ±2%, VSS=-5.0V		15	18	21	kHz		
		Ri=1.0MΩ±2%, VSS=-3.0V		11	16	21			
Reset time	TR		RES	1.0	—	1000	μs		

\* 1 A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

**AC Characteristics**

○ Read/Write timing for the 80-port MPU

(Ta=-20to75°C, VSS=-5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
Address hold time	A0, CS	tAH8	CL=100pF	10	—	—	ns
Address set-up time		tAW8		20	—	—	ns
System cycle time	WR, RD	tCYC8		1000	—	—	ns
Control pulse width		tCC		200	—	—	ns
Data set-up time	D0toD7	tDS8		80	—	—	ns
Data hold time		tDH8		10	—	—	ns
RD access time		tACC8		—	—	90	ns
Output disable time		tOH8		10	—	60	ns

\* 2 The ratings when VSS=-3.0V are approximately 100% higher than when VSS=-5.0V.

○ Read/Write timing for the 68-port MPU

(Ta=-20to75°C, VSS=-5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
System cycle time	A0, CS	tCYC6 *3	CL=100pF	1000	—	—	ns
Address set-up time		tAW6		20	—	—	ns
Address hold time	tAH6	10		—	—	ns	
Data set-up time	D0toD7	tDS6		80	—	—	ns
Data hold time		tDH6		10	—	—	ns
Output disable time		tOH6		10	—	60	ns
Access time		tACC6		—	—	90	ns
Enable pulse width	READ	E		teW	100	—	—
	WRITE		80		—	—	ns

\* 3 t<sub>cyC6</sub> indicates the cycle during which CS/E are HIGH; it does not indicate the cycle of the E signal.

\* 4 The ratings when VSS=-3.0V are approximately 100% higher than when VSS=-5.0V.

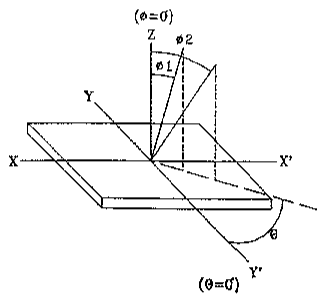
■ Optical Characteristics  
1. STN TYPE

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	$\phi 2 - \phi 1$	$K=1.4$	40	—	—	deg.	*1,*2
Contrast Ratio	K	$\phi = 10^\circ$ $\theta = 0^\circ$	—	3	—	—	*3
Response Time(Rise)	tr	$\phi = 10^\circ$ $\theta = 0^\circ$	—	150	250	ms	*4
Response Time(Fall)	tf	$\phi = 10^\circ$ $\theta = 0^\circ$	—	200	300	ms	*4

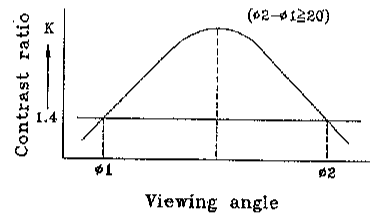
2. TN TYPE

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	$\phi 2 - \phi 1$	$K=1.4$	60	—	—	deg.	*1,*2
Contrast Ratio	K	$\phi = 25^\circ$ $\theta = 0^\circ$	—	3	—	—	*3
Response Time(Rise)	tr	$\phi = 25^\circ$ $\theta = 0^\circ$	—	80	120	ms	*4
Response Time(Fall)	tf	$\phi = 25^\circ$ $\theta = 0^\circ$	—	60	90	ms	*4

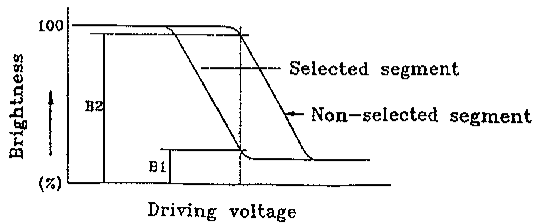
\*1. Definition of  $\phi$  AND  $\theta$



\*2. Contrast vs viewing angle

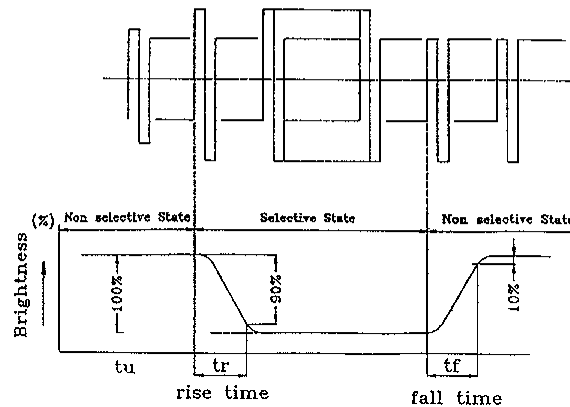


\*3. definition of contrast ratio



$$K = \frac{\text{Brightness of non-selected segment}(B2)}{\text{Brightness of selected segment}(B1)}$$

\*4. Definition of optical response



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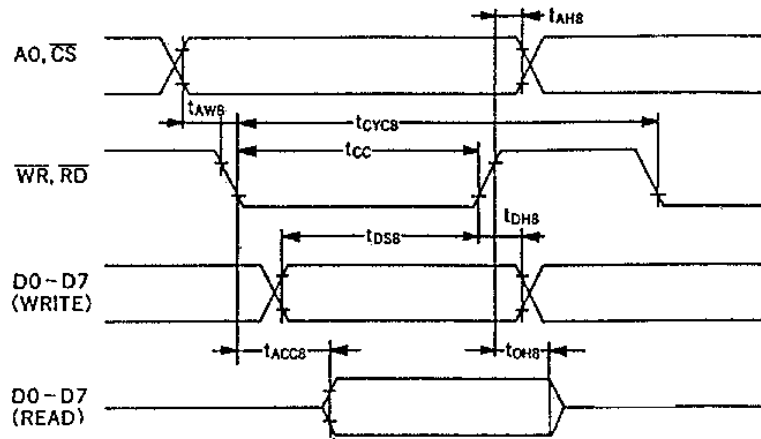
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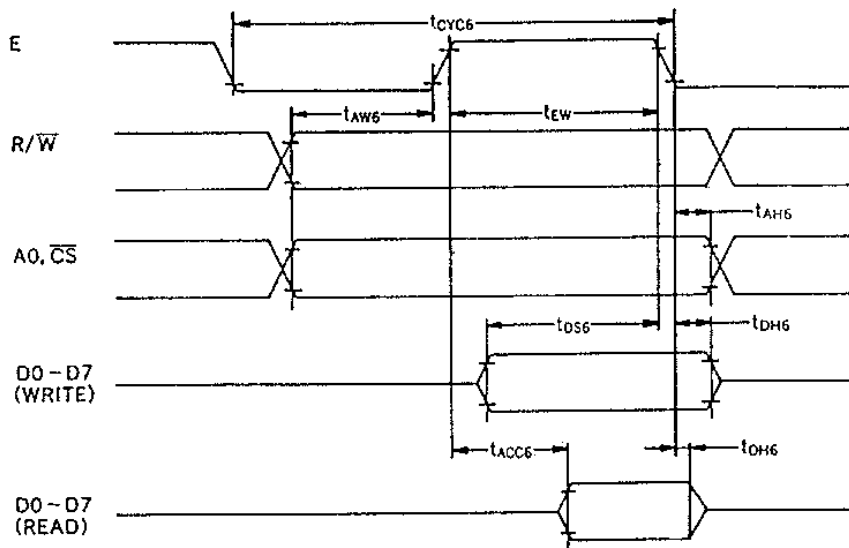
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● Timing Chart

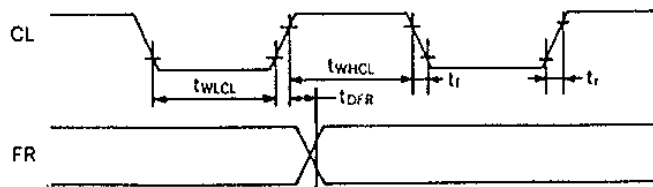
○ Read/Write timing for the 80-port MPU



○ Read/Write timing for the 68-port MPU



○ Control timing for 80-port/68-port display



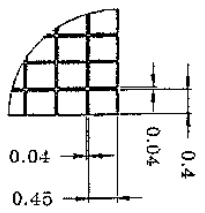
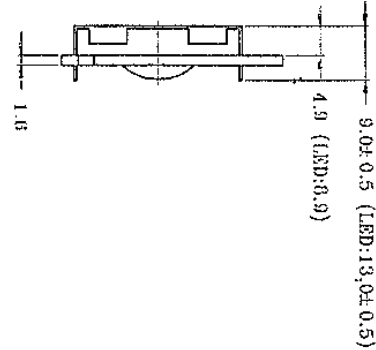
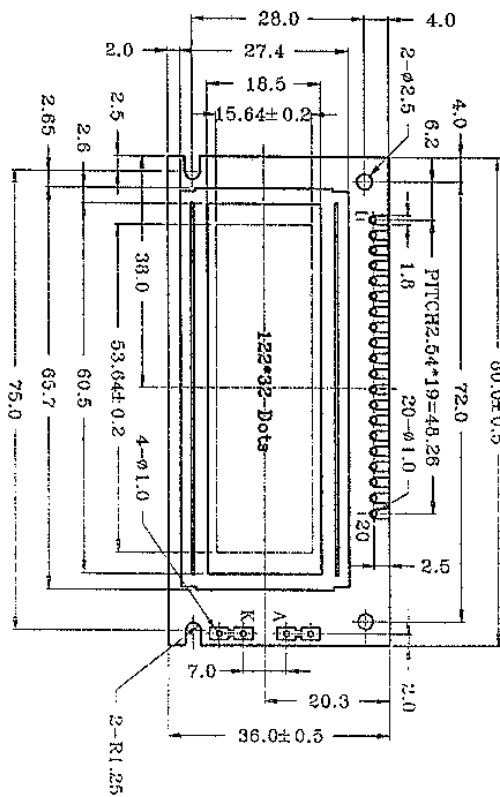
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■ DISPLAY COMMANDS

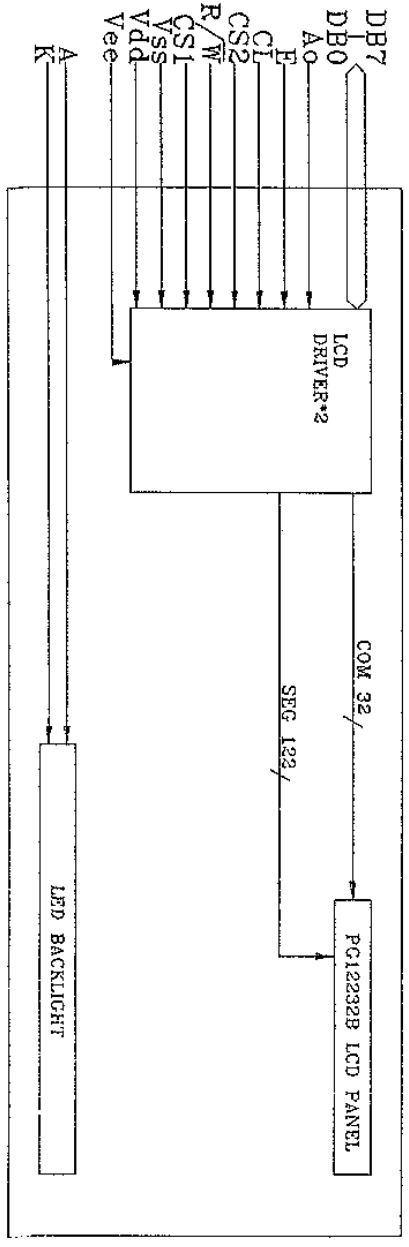
(Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU.)

Command	RDWR A0	D7 D6 D5 D4 D3 D2 D1 D0	Function
1 Display ON/OFF	1 0 0	1 0 1 0 1 1 1 0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *7
2 Display START Line	1 0 0	1 1 0	Display START address (0~31) Determines the line of RAM data to be displayed at the display's top line (COM0).
3 Page Address Set	1 0 0	1 0 1 1 1 0	Page (0~3) Sets the page of the Display RAM in the page address register.
4 Column (Segment) Address Set	1 0 0	0	Column address (0~79) Sets the column address of the Display RAM in the column address register.
5 Status Read	0 1 0	BUSY ACC ON/OFF RESET	0 0 0 0 Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6 Write Display Data	1 0 1	Write Data	Writes the data on the data bus to RAM
7 Read Display Data	0 1 1	Read Data	Reads data from the Display RAM onto the data bus.
8 ADC Select	1 0 0	1 0 1 0 0 0 0 0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9 Static Drive ON/OFF	1 0 0	1 0 1 0 0 1 0 0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *7 0: Normal display operation
10 Duty Select	1 0 0	1 0 1 0 1 0 0 0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11 Read Modify Write	1 0 0	1 1 1 0 0 0 0 0	Increments the column address counter by one only when display data is written but not when it is read.
12 End	1 0 0	1 1 1 0 1 1 1 0	Cancels the Ready Modify Write mode.
13 Reset	1 0 0	1 1 1 0 0 0 1 0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

\*7. Power Save mode is entered by selecting static drive in Display OFF status.



SCALE:10/1



The tolerance unless classified ±0.3mm

UNIT:mm

PIN NO.	SIGNAL
1	VSS
2	VDD
3	VeE
4	AO
5	CS1
6	CS2
7	CL
8	/RQCD
9	/RQND
10	DB0
11	DB1
12	DB2
13	DB3
14	DB4
15	DB5
16	DB6
17	DB7
18	RES
19	A
20	K