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1. General Description

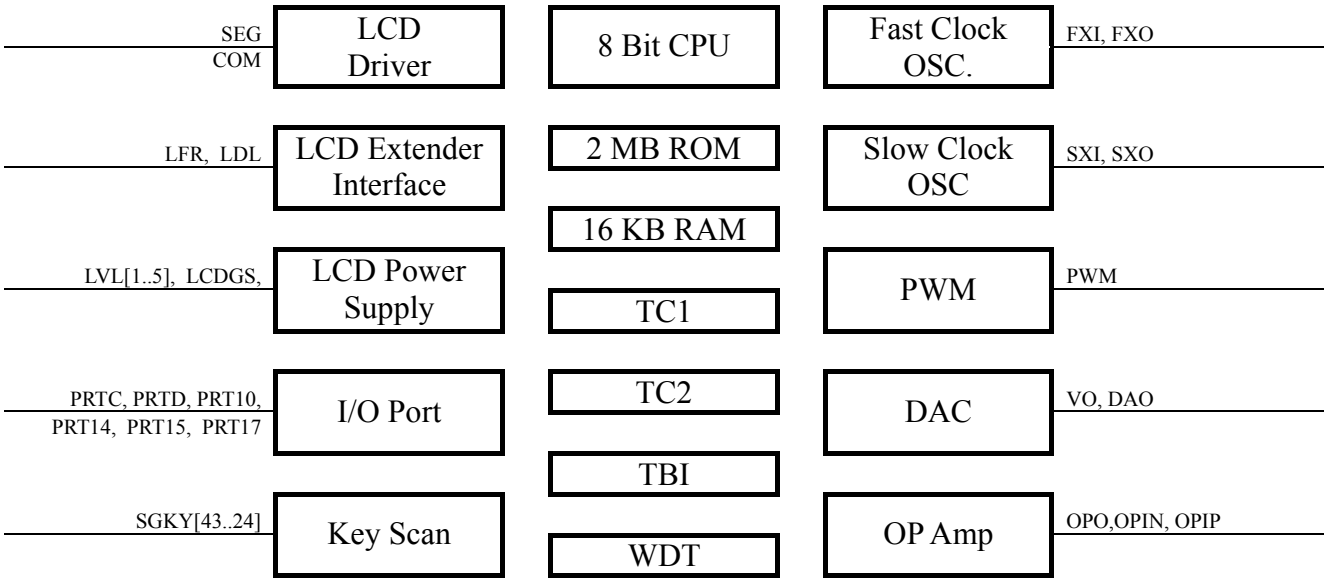
HE847701 is a member of 8-bit Micro-controller series developed by King Billion Electronics. Four LCD driver configurations, 32 COM x 128 SEG, 48 COM x 112 SEG, 64 COM x 96 SEG or 80 COM x 80 SEG are available by mask option. 24 LCD segment driver pins multiplexed with I/O pins to provide flexibility of wide variety of combinations to suit the needs of applications. The built-in LCD power supply is equipped with voltage charge-pump circuit to generate the high voltage required by the high duty LCD driver, bias voltage generating circuit and input voltage regulator circuit to supply stable LCD display effect over the wide battery life. The built-in OP comparator can be used with (light, voice, temperature, humility) sensor and used as battery low detection. 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 2M ROM Size can be used in the storage of speech, graphic, text, etc. It is ideal for applications such as Translator, Data Bank, Educational Toy, Digital Voice Recording System, etc.

The instruction set of HE80000 series is easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks to execute. The processing power is enough to most of battery operation system.

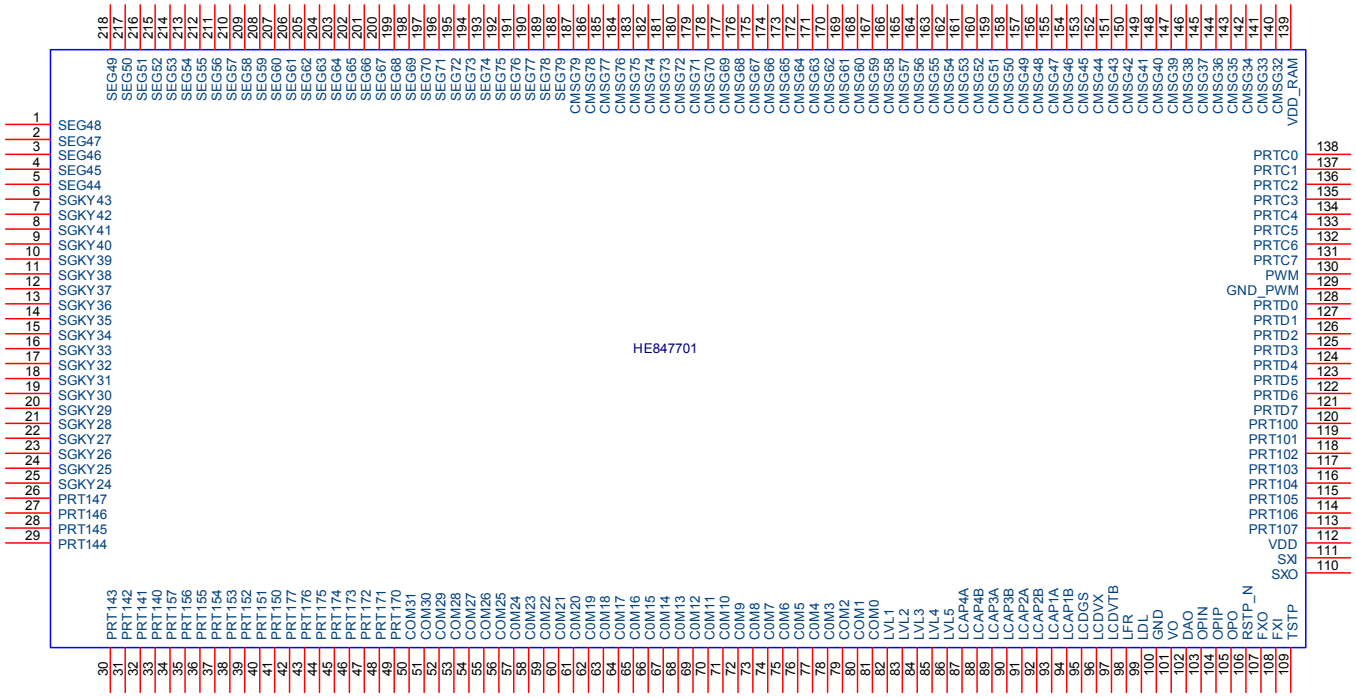
2. Features

- ✓ Operation Voltage: 2.4V ~ 3.6V
- ✓ System Clock: DC ~ 8 MHz @ VDD=3.6V and VDD－VDD_RAM ≦0.3Volt.
  DC ~ 6 MHz @ VDD=2.4V and VDD－VDD_RAM ≦0.3Volt.
- ✓ Internal ROM: 2M Bytes (256 KB Program ROM + 1792 KB Data ROM)
- ✓ Internal RAM: 16K Bytes
- ✓ Dual Clock System: Fast clock: 32768 ~ 8M Hz (No Internal Clock)
  Slow clock: 32768 Hz
- ✓ Operation modes: Fast, Slow, Idle and Sleep modes.
- ✓ 24 ~ 48 bit bi-directional general purpose I/O port with push-pull or Open-Drain output type selectable for each I/O pin by mask option. 24 of them are multiplexed with LCD segment pins.
- ✓ Built-in 4x20 hardware keyboard scan circuit (multiplexed with LCD SEG pin) helps to reduce the pin counts as well as the firmware effort.
- ✓ Voltage Detector with two detecting thresholds.
- ✓ Four LCD configurations: 32 COM x 128 SEG, 48 COM x 112 SEG, 64 COM x 96 SEG or 80 COM x 80 SEG. All of LCD configurations are B TYPE.
- ✓ Built-in LCD power supply with input voltage regulator, voltage charge pump and bias voltage generating circuit.
- ✓ One 7-bit current-type DAC output.
- ✓ Single-ended Pulse Width Modulation circuit for alternative voice output.
- ✓ Built-in OP comparator.
- ✓ Two 16-bit timers and one Time-Base timer.
- ✓ Watch Dog Timer to prevent deadlock condition.
- ✓ Two external interrupts and three internal timer interrupts.
- ✓ Instruction set: 32 instructions with 4 addressing mode.

3. Functional Block Diagram



4. Pin Description



Pin Name	Pin #	I/O	Description
SEG[79..44]	188~218, 1 ~ 5	O	LCD segment SEG[79..44] driver outputs.
SGKY[43..24]	6 ~ 25	O	LCD segments share pads with key scan out SCNO[19..0]. The key scan function of these pins can be disabled by mask option clearing MO_LCDKEY to '0', then SGKY[43..24] function as LCD segment driver only. Setting MO_LCDKEY to '1'

Pin Name	Pin #	I/O	Description
			will turn on the key scan function.
PRT14[7..0]	26 ~ 33	B/O	8-bit bi-directional I/O port 14 is shared with LCD segment pads SEG[23..16]. The function of the pad can be selected individually by mask options MO_LIO14[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_14PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT15[7..0]	34 ~ 41	B/O	8-bit bi-directional I/O port 15 is shared with LCD segment pads SEG[16..8]. The function of the pad can be selected individually by mask options MO_LIO15[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_15PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT17[7..0]	42 ~ 49	B/O	8-bit bi-directional I/O port 17 is shared with LCD segment pads SEG[7..0]. The function of the pad can be selected individually by mask options MO_LIO17[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_17PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
COM[31..0]	50 ~ 81	O	LCD COMMON Driver pads.
LVL1	82	B	LCD Bias Voltage 1
LVL2	83	B	LCD Bias Voltage 2
LVL3	84	B	LCD Bias Voltage 3
LVL4	85	B	LCD Bias Voltage 4
LVL5	86	B	LCD Bias Voltage 5
LCAP4A	87	B	Charge Pump Capacitor Pin
LCAP4B	88	B	Charge Pump Capacitor Pin.
LCAP3A	89	B	Charge Pump Capacitor Pin
LCAP3B	90	B	Charge Pump Capacitor Pin
LCAP2A	91	B	Charge Pump Capacitor Pin
LCAP2B	92	B	Charge Pump Capacitor Pin
LCAP1A	93	B	Charge Pump Capacitor Pin
LCAP1B	94	B	Charge Pump Capacitor Pin
LCDGS	95	B	LCD Voltage setting. Adjust Resistor between LCDGS and LVL2 to set LVL5.
LCDVX	96	B	Charge Pump Capacitor Pin
LCDVTB	97	B	Charge Pump Capacitor Pin
LFR	98	O	LCD frame signal for interfacing with LCD segment extender KD80.
LDL	99	O	LCD data load pin for interfacing with LCD segment extender KD80.
GND	100	P	Power ground Input.
VO	101	O	DAC Voice Output. Set the bit 1 and clear the bit 0 of VOC (DA = ‘1’ and OP = ‘0’) register to turn on DAC with VO output.
DAO	102	O	Alternate output of DAC. Set both bit 1 and bit 0 of VOC register (DA = ‘1’ and OP = ‘1’) to turn on DAC with DAO output as well as OP comparator.
OPIN	103	I	Inverting input of OP Amp. Set the bit 0 of VOC register (OP = ‘1’) to turn on OP comparator.
OPIP	104	I	Non-inverting input of OP Amp.
OPO	105	O	Output of OP Amp.
RSTP_N	106	I	System Reset input pin. Level trigger, active low on this pin will put the chip in reset state.

Pin Name	Pin #	I/O	Description
FXO, FXI	107, 108	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL ('0' for RC type and '1' for crystal type). For RC type oscillator, one resistor need to be connected between FXI and GND. For crystal oscillator, one crystal need to be placed between FXI and FXO. Please refer to application circuit for details.
TSTP_P	109	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	110, 111	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose '0' for RC type and '1' for crystal oscillator.
VDD	112	P	Positive power Input. 0.1 µF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
PRT10[7..0]	113~120	B	8-bit bi-directional I/O port 10. The output type of I/O pad can be selected by mask option MO_10PP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O pad as input pad, "1" must be outputted before reading.
PRTD[7..0]	121~128	B	8-bit bi-directional I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be as external interrupt sources.
GND_PWM	129	O	Dedicated Ground for PWM output.
PWM	130	O	The PWM output can drive speaker or buzzer directly. Set the bit2 of VOC register as one to turn on PWM. Using VDD & PWM to drive output device.
PRTC[7..0]	131 ~ 138	B	8-bit bi-directional I/O port C. PRTC[7:4] is shared with Key Scan Dedicated Input SCNI[3:0]. The Key Scan function can be disabled by clearing MO_LCDKEY mask option to '0'. The output type of I/O pad can also be selected by mask option MO_CPP[7..0] ('1' for push-pull and '0' for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, '1' must be outputted before reading the pin.
VDD_RAM	139	P	Dedicated power input for RAM
CMSG[32..79]	140~187	O	COM[32..79] pads are shared with SEG[127..80] outputs. The functions of the pads to be COM drivers or SEG drivers can be selected by mask option MO_COM[0]. Please refer to LCD driver configuration for details.

I: Input, O: Output, B: Bidirectional, P: Power.

5. Pad Location

Die Size: X= 9460 µm, Y=4150 µm, and substrate is connected to GND.

Pin No.	Pin name	X Coord.	Y-Coord.	Pin No.	Pin name	X Coord.	Y-Coord.
1	SEG[48]	-4652.4	1615.02	110	SXO	4637.6	-1693.22
2	SEG[47]	-4652.4	1500.02	111	SXI	4637.6	-1578.22
3	SEG[46]	-4652.4	1385.02	112	VDD	4637.6	-1458.22
4	SEG[45]	-4652.4	1270.02	113	PRT10[7]	4637.6	-1343.22
5	SEG[44]	-4652.4	1155.02	114	PRT10[6]	4637.6	-1228.22
6	SGKY[43]	-4652.4	1040.02	115	PRT10[5]	4637.6	-1113.22
7	SGKY[42]	-4652.4	925.02	116	PRT10[4]	4637.6	-998.22
8	SGKY[41]	-4652.4	810.02	117	PRT10[3]	4637.6	-883.22
9	SGKY[40]	-4652.4	695.02	118	PRT10[2]	4637.6	-768.22
10	SGKY[39]	-4652.4	580.02	119	PRT10[1]	4637.6	-653.22
11	SGKY[38]	-4652.4	465.02	120	PRT10[0]	4637.6	-538.22
12	SGKY[37]	-4652.4	350.02	121	PRTD[7]	4637.6	-423.22
13	SGKY[36]	-4652.4	235.02	122	PRTD[6]	4637.6	-308.22
14	SGKY[35]	-4652.4	120.02	123	PRTD[5]	4637.6	-193.22
15	SGKY[34]	-4652.4	5.02	124	PRTD[4]	4637.6	-78.22
16	SGKY[33]	-4652.4	-109.98	125	PRTD[3]	4637.6	36.79
17	SGKY[32]	-4652.4	-224.98	126	PRTD[2]	4637.6	151.79
18	SGKY[31]	-4652.4	-339.98	127	PRTD[1]	4637.6	266.79
19	SGKY[30]	-4652.4	-454.98	128	PRTD[0]	4637.6	381.79
20	SGKY[29]	-4652.4	-569.98	129	GND_PWM	4637.6	496.79
21	SGKY[28]	-4652.4	-684.98	130	PWM	4637.6	621.74
22	SGKY[27]	-4652.4	-799.98	131	PRTC[7]	4637.6	744.24
23	SGKY[26]	-4652.4	-914.98	132	PRTC[6]	4637.6	859.24
24	SGKY[25]	-4652.4	-1029.98	133	PRTC[5]	4637.6	974.24
25	SGKY[24]	-4652.4	-1144.98	134	PRTC[4]	4637.6	1089.24

Pin No.	Pin name	X Coord.	Y-Coord.	Pin No.	Pin name	X Coord.	Y-Coord.
26	PRT14[7]	-4652.4	-1259.98	135	PRTC[3]	4637.6	1204.24
27	PRT14[6]	-4652.4	-1374.98	136	PRTC[2]	4637.6	1319.24
28	PRT14[5]	-4652.4	-1489.98	137	PRTC[1]	4637.6	1434.24
29	PRT14[4]	-4652.4	-1604.98	138	PRTC[0]	4637.6	1549.24
30	PRT14[3]	-4505.17	-1997.5	139	VDD_RAM	4630.6	1997.5
31	PRT14[2]	-4390.17	-1997.5	140	CMSG[32]	4477.6	1997.5
32	PRT14[1]	-4259.9	-1997.5	141	CMSG[33]	4362.6	1997.5
33	PRT14[0]	-4144.9	-1997.5	142	CMSG[34]	4247.6	1997.5
34	PRT15[7]	-4029.9	-1997.5	143	CMSG[35]	4132.6	1997.5
35	PRT15[6]	-3914.9	-1997.5	144	CMSG[36]	4017.6	1997.5
36	PRT15[5]	-3799.9	-1997.5	145	CMSG[37]	3902.6	1997.5
37	PRT15[4]	-3684.9	-1997.5	146	CMSG[38]	3787.6	1997.5
38	PRT15[3]	-3569.9	-1997.5	147	CMSG[39]	3672.6	1997.5
39	PRT15[2]	-3454.9	-1997.5	148	CMSG[40]	3557.6	1997.5
40	PRT15[1]	-3339.9	-1997.5	149	CMSG[41]	3442.6	1997.5
41	PRT15[0]	-3224.9	-1997.5	150	CMSG[42]	3327.6	1997.5
42	PRT17[7]	-3109.9	-1997.5	151	CMSG[43]	3212.6	1997.5
43	PRT17[6]	-2994.9	-1997.5	152	CMSG[44]	3097.6	1997.5
44	PRT17[5]	-2879.9	-1997.5	153	CMSG[45]	2982.6	1997.5
45	PRT17[4]	-2764.9	-1997.5	154	CMSG[46]	2867.6	1997.5
46	PRT17[3]	-2649.9	-1997.5	155	CMSG[47]	2752.6	1997.5
47	PRT17[2]	-2534.9	-1997.5	156	CMSG[48]	2637.6	1997.5
48	PRT17[1]	-2419.9	-1997.5	157	CMSG[49]	2522.6	1997.5
49	PRT17[0]	-2304.9	-1997.5	158	CMSG[50]	2407.6	1997.5
50	COM[31]	-2189.9	-1997.5	159	CMSG[51]	2292.6	1997.5
51	COM[30]	-2074.9	-1997.5	160	CMSG[52]	2177.6	1997.5
52	COM[29]	-1959.9	-1997.5	161	CMSG[53]	2062.6	1997.5
53	COM[28]	-1844.9	-1997.5	162	CMSG[54]	1947.6	1997.5
54	COM[27]	-1729.9	-1997.5	163	CMSG[55]	1832.6	1997.5
55	COM[26]	-1614.9	-1997.5	164	CMSG[56]	1717.6	1997.5
56	COM[25]	-1499.9	-1997.5	165	CMSG[57]	1602.6	1997.5
57	COM[24]	-1384.9	-1997.5	166	CMSG[58]	1487.6	1997.5
58	COM[23]	-1269.9	-1997.5	167	CMSG[59]	1372.6	1997.5
59	COM[22]	-1154.9	-1997.5	168	CMSG[60]	1257.6	1997.5
60	COM[21]	-1039.9	-1997.5	169	CMSG[61]	1142.6	1997.5
61	COM[20]	-924.9	-1997.5	170	CMSG[62]	1027.6	1997.5
62	COM[19]	-809.9	-1997.5	171	CMSG[63]	912.6	1997.5
63	COM[18]	-694.9	-1997.5	172	CMSG[64]	797.6	1997.5
64	COM[17]	-579.9	-1997.5	173	CMSG[65]	682.6	1997.5
65	COM[16]	-444.9	-1997.5	174	CMSG[66]	567.6	1997.5
66	COM[15]	-329.9	-1997.5	175	CMSG[67]	452.6	1997.5
67	COM[14]	-214.9	-1997.5	176	CMSG[68]	337.6	1997.5
68	COM[13]	-99.9	-1997.5	177	CMSG[69]	222.6	1997.5
69	COM[12]	15.1	-1997.5	178	CMSG[70]	107.6	1997.5
70	COM[11]	130.1	-1997.5	179	CMSG[71]	-7.4	1997.5
71	COM[10]	245.1	-1997.5	180	CMSG[72]	-122.4	1997.5
72	COM[9]	360.1	-1997.5	181	CMSG[73]	-237.4	1997.5
73	COM[8]	475.1	-1997.5	182	CMSG[74]	-352.4	1997.5
74	COM[7]	590.1	-1997.5	183	CMSG[75]	-467.4	1997.5
75	COM[6]	705.1	-1997.5	184	CMSG[76]	-602.4	1997.5
76	COM[5]	820.1	-1997.5	185	CMSG[77]	-717.4	1997.5

Pin No.	Pin name	X Coord.	Y-Coord.	Pin No.	Pin name	X Coord.	Y-Coord.
77	COM[4]	935.1	-1997.5	186	CMSG[78]	-832.4	1997.5
78	COM[3]	1050.1	-1997.5	187	CMSG[79]	-947.4	1997.5
79	COM[2]	1165.1	-1997.5	188	SEG[79]	-1062.4	1997.5
80	COM[1]	1280.1	-1997.5	189	SEG[78]	-1177.4	1997.5
81	COM[0]	1395.1	-1997.5	190	SEG[77]	-1292.4	1997.5
82	LVL1	1510.1	-1997.5	191	SEG[76]	-1407.4	1997.5
83	LVL2	1625.1	-1997.5	192	SEG[75]	-1522.4	1997.5
84	LVL3	1740.1	-1997.5	193	SEG[74]	-1637.4	1997.5
85	LVL4	1855.1	-1997.5	194	SEG[73]	-1752.4	1997.5
86	LVL5	1970.1	-1997.5	195	SEG[72]	-1867.4	1997.5
87	LCAP4A	2085.1	-1997.5	196	SEG[71]	-1982.4	1997.5
88	LCAP4B	2200.1	-1997.5	197	SEG[70]	-2097.4	1997.5
89	LCAP3A	2315.1	-1997.5	198	SEG[69]	-2212.4	1997.5
90	LCAP3B	2430.1	-1997.5	199	SEG[68]	-2327.4	1997.5
91	LCAP2A	2545.1	-1997.5	200	SEG[67]	-2442.4	1997.5
92	LCAP2B	2660.1	-1997.5	201	SEG[66]	-2557.4	1997.5
93	LCAP1A	2775.1	-1997.5	202	SEG[65]	-2672.4	1997.5
94	LCAP1B	2890.1	-1997.5	203	SEG[64]	-2787.4	1997.5
95	LCDGS	3005.1	-1997.5	204	SEG[63]	-2902.4	1997.5
96	LCDVX	3120.1	-1997.5	205	SEG[62]	-3017.4	1997.5
97	LCDVTB	3235.1	-1997.5	206	SEG[61]	-3132.4	1997.5
98	LFR	3352.34	-1997.5	207	SEG[60]	-3247.4	1997.5
99	LDL	3467.34	-1997.5	208	SEG[59]	-3362.4	1997.5
100	GND:G	3585.1	-1997.5	209	SEG[58]	-3477.4	1997.5
101	VO	3700.1	-1997.5	210	SEG[57]	-3592.4	1997.5
102	DAO	3815.1	-1997.5	211	SEG[56]	-3707.4	1997.5
103	OPIN	3930.1	-1997.5	212	SEG[55]	-3822.4	1997.5
104	OPIP	4045.1	-1997.5	213	SEG[54]	-3937.4	1997.5
105	OPO	4160.1	-1997.5	214	SEG[53]	-4052.4	1997.5
106	RSTP_N	4275.1	-1997.5	215	SEG[52]	-4167.4	1997.5
107	FXO	4390.1	-1997.5	216	SEG[51]	-4282.4	1997.5
108	FXI	4505.1	-1997.5	217	SEG[50]	-4397.4	1997.5
109	TSTP_P	4620.1	-1997.5	218	SEG[49]	-4512.4	1997.5

6. LCD RAM Map

There are 4 LCD configurations as determined by mask option MO_COM[1..0]. The functions of CMSG[79..32] are different in each configuration as listed in the following table.

MO_COM[1..0]	Configuration	CMSG[79..64]	CMSG[63..48]	CMSG[47..32]
00	32 x 128	SEG[80..95]	SEG[96..111]	SEG[112..127]
01	48 x 112	SEG[80..95]	SEG[96..111]	COM[47..32]
10	64 x 96	SEG[80..95]	COM[63..48]	COM[47..32]
11	80 x 80	COM[79..64]	COM[63..48]	COM[47..32]

COMXSEG	32X128	48X112	64X96	80X80
CMSG32	SEG127	COM32	COM32	COM32
CMSG33	SEG126	COM33	COM33	COM33
CMSG34	SEG125	COM34	COM34	COM34
CMSG35	SEG124	COM35	COM35	COM35
CMSG36	SEG123	COM36	COM36	COM36
CMSG37	SEG122	COM37	COM37	COM37
CMSG38	SEG121	COM38	COM38	COM38
CMSG39	SEG120	COM39	COM39	COM39
CMSG40	SEG119	COM40	COM40	COM40
CMSG41	SEG118	COM41	COM41	COM41
CMSG42	SEG117	COM42	COM42	COM42
CMSG43	SEG116	COM43	COM43	COM43
CMSG44	SEG115	COM44	COM44	COM44
CMSG45	SEG114	COM45	COM45	COM45
CMSG46	SEG113	COM46	COM46	COM46
CMSG47	SEG112	COM47	COM47	COM47
CMSG48	SEG111	SEG111	COM48	COM48
CMSG49	SEG110	SEG110	COM49	COM49
CMSG50	SEG109	SEG109	COM50	COM50
CMSG51	SEG108	SEG108	COM51	COM51
CMSG52	SEG107	SEG107	COM52	COM52
CMSG53	SEG106	SEG106	COM53	COM53
CMSG54	SEG105	SEG105	COM54	COM54
CMSG55	SEG104	SEG104	COM55	COM55
CMSG56	SEG103	SEG103	COM56	COM56
CMSG57	SEG102	SEG102	COM57	COM57
CMSG58	SEG101	SEG101	COM58	COM58
CMSG59	SEG100	SEG100	COM59	COM59
CMSG60	SEG99	SEG99	COM60	COM60
CMSG61	SEG98	SEG98	COM61	COM61
CMSG62	SEG97	SEG97	COM62	COM62
CMSG63	SEG96	SEG96	COM63	COM63
CMSG64	SEG95	SEG95	SEG95	COM64
CMSG65	SEG94	SEG94	SEG94	COM65
CMSG66	SEG93	SEG93	SEG93	COM66
CMSG67	SEG92	SEG92	SEG92	COM67
CMSG68	SEG91	SEG91	SEG91	COM68
CMSG69	SEG90	SEG90	SEG90	COM69
CMSG70	SEG89	SEG89	SEG89	COM70
CMSG71	SEG88	SEG88	SEG88	COM71
CMSG72	SEG87	SEG87	SEG87	COM72
CMSG73	SEG86	SEG86	SEG86	COM73
CMSG74	SEG85	SEG85	SEG85	COM74
CMSG75	SEG84	SEG84	SEG84	COM75
CMSG76	SEG83	SEG83	SEG83	COM76
CMSG77	SEG82	SEG82	SEG82	COM77
CMSG78	SEG81	SEG81	SEG81	COM78
CMSG79	SEG80	SEG80	SEG80	COM79

The RAM Maps of all four different LCD configurations are as the following:

32 COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	7E0H	7C0H	7A0H	780H	760H	740H	720H	700H
COM1	7E1H	7C1H	7A1H	781H	761H	741H	721H	701H
:	:	:	:	:	:	:	:	:
COM15	7EFH	7CFH	7AFH	78FH	76FH	74FH	72FH	70FH
COM16	7F0H	7D0H	7B0H	790H	770H	750H	730H	710H
:	:	:	:	:	:	:	:	:
COM30	7FEH	7DEH	7BEH	79EH	77EH	75EH	73EH	71EH
COM31	7FFH	7DFH	7BFH	79FH	77FH	75FH	73FH	71FH
Page 6	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]	SEG [103:96]	SEG [111:104]	SEG [119:112]	SEG [127:120]
COM0	6E0H	6C0H	6A0H	680H	660H	640H	620H	600H
COM1	6E1H	6C1H	6A1H	681H	661H	641H	621H	601H
:	:	:	:	:	:	:	:	:
COM15	6EFH	6CFH	6AFH	68FH	66FH	64FH	62FH	60FH
COM16	6F0H	6D0H	6B0H	690H	670H	650H	630H	610H

:	:	:	:	:	:	:	:	:
COM30	6FEH	6DEH	6BEH	69EH	67EH	65EH	63EH	61EH
COM31	6FFH	6DFH	6BFH	69FH	67FH	65FH	63FH	61FH

48 COM:

Page 7,6	SEG[7:0]	SEG[15:8]	SEG[23:16]	SEG[31:24]	SEG[39:32]	SEG[47:40]	SEG[55:48]
COM0	7C0H	780H	740H	700H	6C0H	680H	640H
COM1	7C1H	781H	741H	701H	6C1H	681H	641h
:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH	64FH
COM16	7D0H	790H	750H	710H	6D0H	690H	650H
:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH	65FH
COM32	7E0H	7A0H	760H	720H	6E0H	6A0H	660H
:	:	:	:	:	:	:	:
COM46	7EEH	7AEH	76EH	72EH	6EEH	6AEH	66EH
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH	66FH

Page 6, 5, 4	SEG [63:56]	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]	SEG [103:96]	SEG [111:104]
COM0	600H	5C0H	580H	540H	500H	4C0H	480H
COM1	601H	5C1H	581H	541h	501H	4C1H	481H
:	:	:	:	:	:	:	:
COM15	60FH	5CFH	58FH	54FH	50FH	4CFH	48FH
COM16	610H	5D0H	590H	550H	510H	4D0H	490H
:	:	:	:	:	:	:	:
COM31	61FH	5DFH	59FH	55FH	51FH	4DFH	49FH
COM32	620H	5E0H	5A0H	560H	520H	4E0H	4A0H
:	:	:	:	:	:	:	:
COM46	62EH	5EEH	5AEH	56EH	52EH	4EEH	4AEH
COM47	62FH	5EFH	5AFH	56FH	52FH	4EFH	4AFH

64 COM:

Page 7,6	SEG[7:0]	SEG[15:8]	SEG[23:16]	SEG[31:24]	SEG[39:32]	SEG[47:40]
COM0	7C0H	780H	740H	700H	6C0H	680H
COM1	7C1H	781H	741H	701H	6C1H	681H
:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH
COM16	7D0H	790H	750H	710H	6D0H	690H
:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH
COM32	7E0H	7A0H	760H	720H	6E0H	6A0H
:	:	:	:	:	:	:
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH
COM48	7F0H	7B0H	770H	730H	6F0H	6B0H
:	:	:	:	:	:	:
COM62	7FEH	7BEH	77EH	73EH	6FEH	6BEH
COM63	7FFH	7BFH	77FH	73FH	6FFH	6BFH

Page 6, 5	SEG[55:48]	SEG[63:56]	SEG[71:64]	SEG[79:72]	SEG[87:80]	SEG[95:88]
COM0	640H	600H	5C0H	580H	540H	500H
COM1	641H	601H	5C1H	581H	541H	501H
:	:	:	:	:	:	:
COM15	64FH	60FH	5CFH	58FH	54FH	50FH
COM16	650H	610H	5D0H	590H	550H	510H
:	:	:	:	:	:	:
COM31	65FH	61FH	5DFH	59FH	55FH	51FH
COM32	660H	620H	5E0H	5A0H	560H	520H
:	:	:	:	:	:	:
COM47	66FH	62FH	5EFH	5AFH	56FH	52FH
COM48	670H	630H	5F0H	5B0H	570H	530H
:	:	:	:	:	:	:
COM62	67EH	63EH	5FEH	5BEH	57EH	53EH
COM63	67FH	63FH	5FFH	5BFH	57FH	53FH

80 COM:

Page 7:3	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]
COM0	780H	700H	680H	600H	580H	500H	480H	400H	380H	300H
COM1	781H	701H	681H	601H	581H	501H	481H	401H	381H	301H
:	:	:	:	:	:	:	:	:	:	:
COM15	78FH	70FH	68FH	60FH	58FH	50FH	48FH	40FH	38FH	30FH
COM16	790H	710H	690H	610H	590H	510H	490H	410H	390H	310H
:	:	:	:	:	:	:	:	:	:	:
COM31	79FH	71FH	69FH	61FH	59FH	51FH	49FH	41FH	39FH	31FH
COM32	7A0H	720H	6A0H	620H	5A0H	520H	4A0H	420H	3A0H	320H
:	:	:	:	:	:	:	:	:	:	:
COM47	7AFH	72FH	6AFH	62FH	5AFH	52FH	4AFH	42FH	3AFH	32FH
COM48	7B0H	730H	6B0H	630H	5B0H	530H	4B0H	430H	3B0H	330H
:	:	:	:	:	:	:	:	:	:	:
COM62	7BFH	73FH	6BFH	63FH	5BFH	53FH	4BFH	43FH	3BFH	33FH
COM63	7C0H	740H	6C0H	640H	5C0H	540H	4C0H	440H	3C0H	340H
:	:	:	:	:	:	:	:	:	:	:
COM78	7CEH	74EH	6CEH	64EH	5CEH	54EH	4CEH	44EH	3CEH	34EH
COM79	7CFH	74FH	6CFH	64FH	5CFH	54FH	4CFH	44FH	3CFH	34FH

7. LCD Power Supply

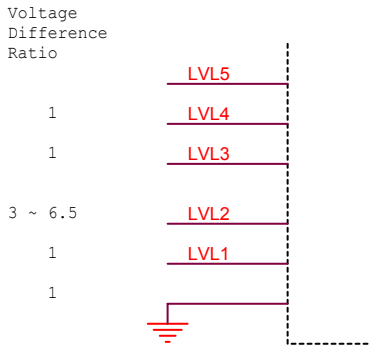
The built-in LCD power supply is equipped with input voltage regulator, voltage charge pump and bias voltage generating circuit with active buffer instead of passive resistor voltage dividing network. The input voltage is regulated to LVL2 using the internally generated reference voltage. LVL2 can be adjusted by resistor between LCDGS and LVL2.

LVL2 adjustment guideline: First, the level of VDD must be 0.3 volt higher than LVL2 even at the end of battery life for the regulator to function properly. For example, if the VDD is expected to drop to 2.2 volts when battery is low, then the level of LVL2 can only be set at 1.9 volts max.

Voltage charge pump: The LVL2 is then pumped to LVL5 based on the bias setting of MO_LBSR[3..0]. The formula for LVL5 is:

LVL5 = LVL2 / 2 x (1/Bias)

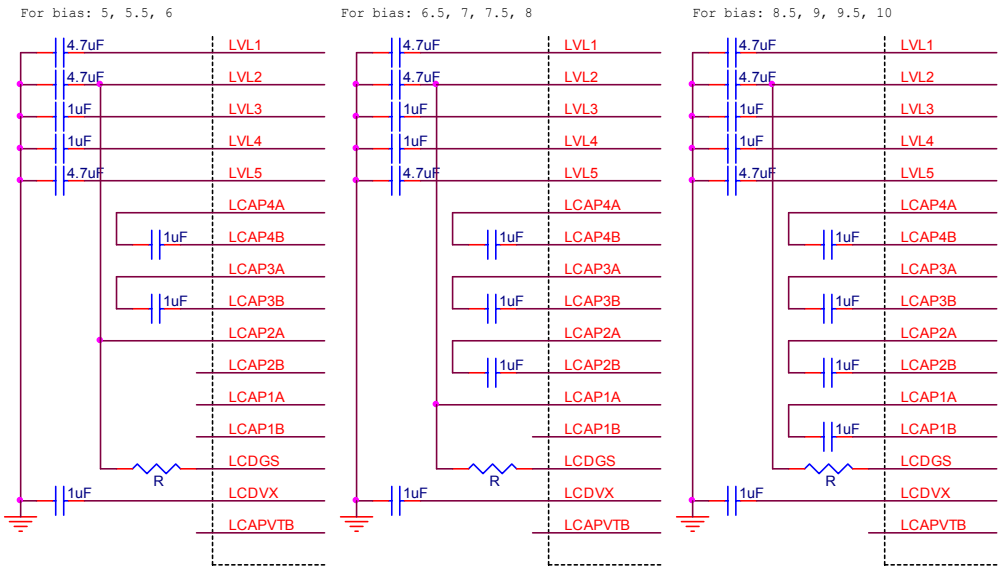
The potential difference between bias voltages LVL1 ~ LVL5 is determined by the bias settings, too.



For example, if the bias setting is 1/7 bias and LVL2 is 2 volts, the LVL5 will be pumped to 7 volts when the load is light.

	Bias	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
Min. VDD	LVL2	LVL5 = LCD Panel Operating Voltage										
2.70	2.40	6.00	6.60	7.20	7.80	8.40						
2.60	2.30	5.75	6.33	6.90	7.48	8.05						
2.50	2.20	5.50	6.05	6.60	7.15	7.70	8.25					
2.40	2.10	5.25	5.78	6.30	6.83	7.35	7.88	8.40				
2.30	2.00	5.00	5.50	6.00	6.50	7.00	7.50	8.00	8.50			
2.20	1.90	4.75	5.23	5.70	6.18	6.65	7.13	7.60	8.08	8.55		
2.10	1.80	4.50	4.95	5.40	5.85	6.30	6.75	7.20	7.65	8.10	8.55	
2.00	1.70	4.25	4.68	5.10	5.53	5.95	6.38	6.80	7.23	7.65	8.08	8.5

Please note that external connections of charge pump capacitors must be made according to the bias setting, too. Please use the following figure as reference when designing application circuit and LVL5 must be lower than 8.5 volts to prevent chip from breaking down.



Different duties require different bias settings. There is some theoretical correspondence between the Duty and Bias Setting. However, it is better to use it as starting point and adjust it with real LCD panel connected to it to determine the final setting. The theoretic relationship between the duty and bias setting as following:

Duty Cycle	Normal Bias	Alternative Bias
32 duty	1/7	1/7.5
48 duty	1/8	1/7.5, 1/8.5
64 duty	1/9	1/8.5, 1/9.5
80 duty	1/10	1/9.5, 1/10.5

The bias setting is made by mask option MO_LBSR[3..0].

MO_LBSR[3:0]	Bias Setting
0000	undefined
0001	1/5
0010	1/5.5
0011	1/6
0100	1/6.5
0101	1/7
0110	1/7.5
0111	1/8
1000	1/8.5
1001	1/9
1010	1/9.5
1011	1/10
1100	1/10.5
1101	1/11
1110	1/11.5
1111	1/12

7.1. LCDC Control register

The gray scale of the LCD driver can be adjusted by GRAY field of LCD. The LCD panel can be blanked by setting the BLANK field of LCDC register. LCD driver can be totally turned off by clearing LCDE bit of LCDC.

LCDC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	-	-	-	GRAY			BLANK	LCDE
Reset	-	-	-	-	-	-	1	0

Field	Value	Function
GRAY	000	LCD is darkest.
	111	LCD is lightest.
BLANK	0	normal display
	1	LCD display blanked. The COM signals of LCD driver output inactive levels (LVL4 and LVL1) while SEG signals output normal display patterns.
LCDE	0	LCD driver disabled, LCD driver has no output signal.
	1	LCD driver Enabled

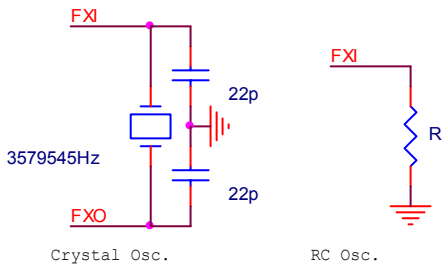
Please note that LCD driver must be turned off before the MCU goes into sleep mode. In other words, user must clear the bit 0 (LCDE bit) of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please note that LCD driver uses slow clock as clock source. The LCD display would not display normally if it worked in Fast clock only mode as the LCD refresh action would be too fast.

8. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. So that system designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.



The RC oscillator has a built-in capacitor. An external resistor is needed to connect from FXI to GND to determine the oscillation frequency. The capacitance of internal RC oscillator is selected by mask option MO_RCAP[2..0].

MO_RCAP[2..0]	Internal RC Cap. OSC. (pF)
000	2
001	4
010	7
011	14
100	20
101	40
110	50
111	60

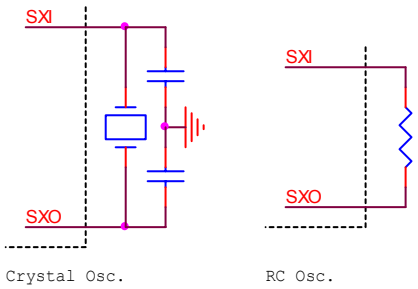
The following table shows the combinations of R and C, and the resulting frequency. Please note that oscillation frequency in the table only represents oscillation frequencies of certain samples. The actual oscillation frequency may vary up to ±15% from lot to lot due to process parameter variations. User must take this into consideration when using this chip in applications.

Ring Oscillator Frequency Table

R(K ohm)\C (pF)	40	20	14	7	4	2	
30.20	0.8	1.5	2.0	3.0	4.0	5.0	MHz
19.92	1.2	2.2	2.8	4.4	5.6	7.0	MHz
9.98	2.3	4.0	5.1	7.5	9.4	11.4	MHz

Two types of oscillator, crystal and RC, can be used as slow clock by mask option MO_SXTAL. If used for time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	R/C oscillator
1	Crystal oscillator



With two clock sources available, the system can switch among operation modes of Fast, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	W	W	W	W
Reset	0	-	-	0	-	-	-	-

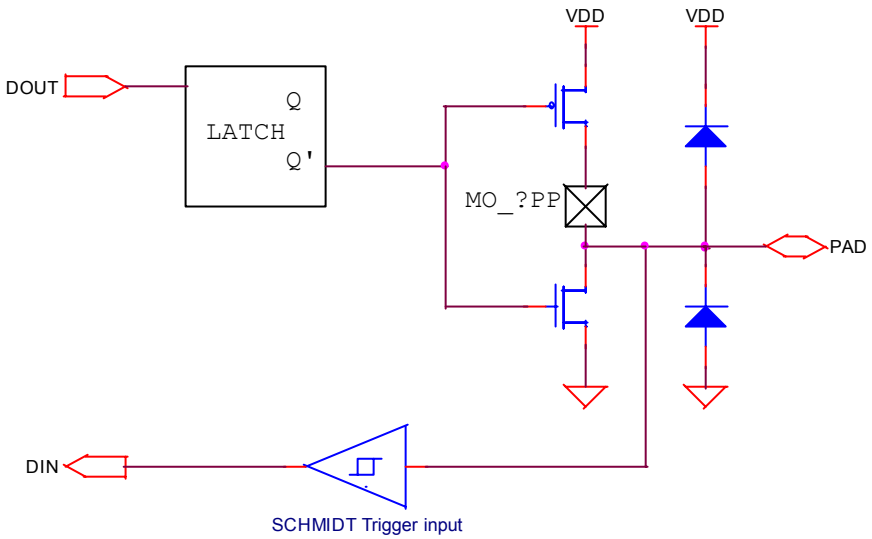
If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

9. General Purpose I/O

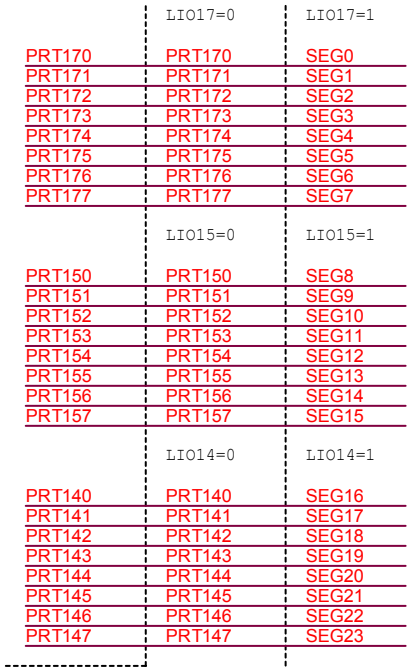
There are three dedicated general purpose I/O port, PRTC, PRTD and PRT10, while PRT14, PRT15 and PRT17 are multiplexed with LCD segment driver pins. All the I/O Ports are bi-directional and of non-tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. Hysteresis level of Schmidt trigger is 1/3*VDD.



As pads of PRT14, PRT15 and PRT17 are shared with LCD segment driver, the function of the pads is determined by mask options.



Following table is the setting for MO_LIO?[...] and MO_?PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO?[…]	MO_?PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

xx: Displayable, but may have abnormal leakage current, do not use.

10. Key Scan Circuit

The built-in 4x20 hardware keyboard scan circuit helps to reduce the pin counts where application requires large key matrix and high LCD pixel count as well as the firmware effort. As key-scan pins are shared with LCD segment and PRTC4 ~ PRTC7 pins, it is advisable to put resistors between segment pins and key matrix to avoid shorting the segment pins when two or more keys in the same row are pressed simultaneously. Two key can be detected simultaneously and the first detected key code is stored in KEY0 register and the second in KEY1 register respectively. The key code for each key location is listed in the following table.

Key Loc	SCNI0	SCNI1	SCNI2	SCNI3
SCNO0	0x80	0xA0	0xC0	0xE0
SCNO1	0x81	0xA1	0xC1	0xE1

SCNO2	0x82	0xA2	0xC2	0xE2
SCNO3	0x83	0xA3	0xC3	0xE3
SCNO4	0x84	0xA4	0xC4	0xE4
SCNO5	0x85	0xA5	0xC5	0xE5
SCNO6	0x86	0xA6	0xC6	0xE6
SCNO7	0x87	0xA7	0xC7	0xE7
SCNO8	0x88	0xA8	0xC8	0xE8
SCNO9	0x89	0xA9	0xC9	0xE9
SCNO10	0x8A	0xAA	0xCA	0xEA
SCNO11	0x8B	0xAB	0xCB	0xEB
SCNO12	0x8C	0xAC	0xCC	0xEC
SCNO13	0x8D	0xAD	0xCD	0xED
SCNO14	0x8E	0xAE	0xCE	0xEE
SCNO15	0x8F	0xAF	0xCF	0xEF
SCNO16	0x90	0xB0	0xD0	0xF0
SCNO17	0x91	0xB1	0xD1	0xF1
SCNO18	0x92	0xB2	0xD2	0xF2
SCNO19	0x93	0xB3	0xD3	0xF3

KEY0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x22	R	Row Index		Column Index				

KEY1	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x23	R	Row Index		Column Index				

The bit 7 of KEY0 and KEY1 is repeat indicator when the same key is scanned for the second time, the R bit will be cleared to indicate the key is not released yet.

The key-scan function can be turned on/off by mask option MO_LCDKEY.

MO_LCDKEY	SGKY[43..24] Function
0	as SEG only
1	as SEG as well as KEY_SCAN

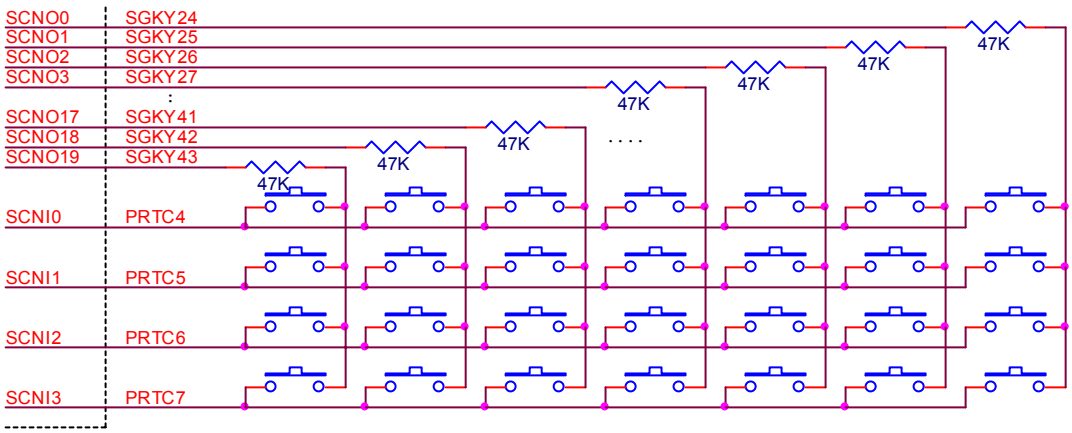
The pulse width of key-scan signal can be selected by mask options MO_SNCK[1..0].

MO_SNCK[1..0]	Key Scan Pulse Width
00	0.5 sck
01	1 sck
10	1.5 sck
11	2 sck

The strength of key-scan signal can also be selected by mask options MO_SNCK[1..0].

MO_SCDRV[1..0]	Key Scan Signal Strength
00	weakest
01	
10	

11	strongest

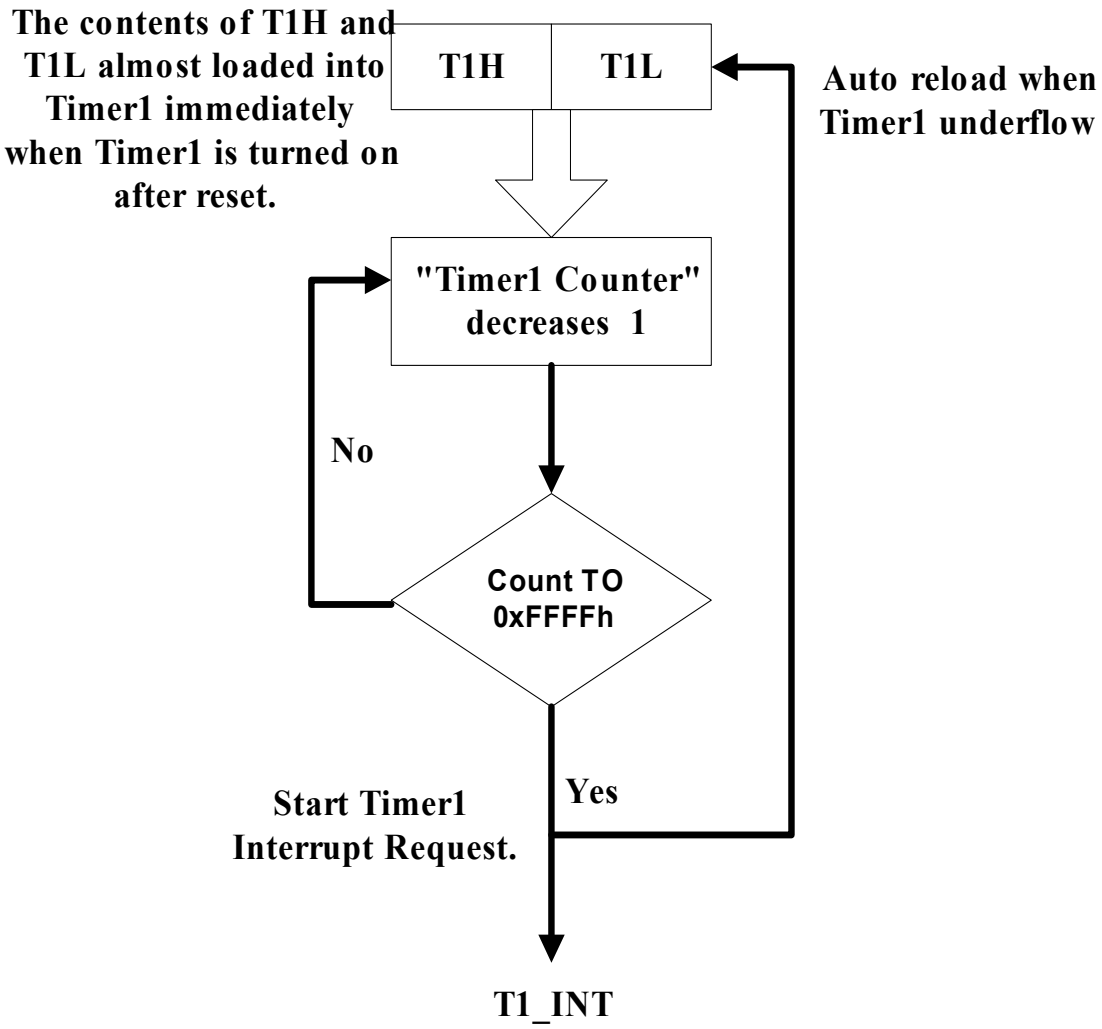


11. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

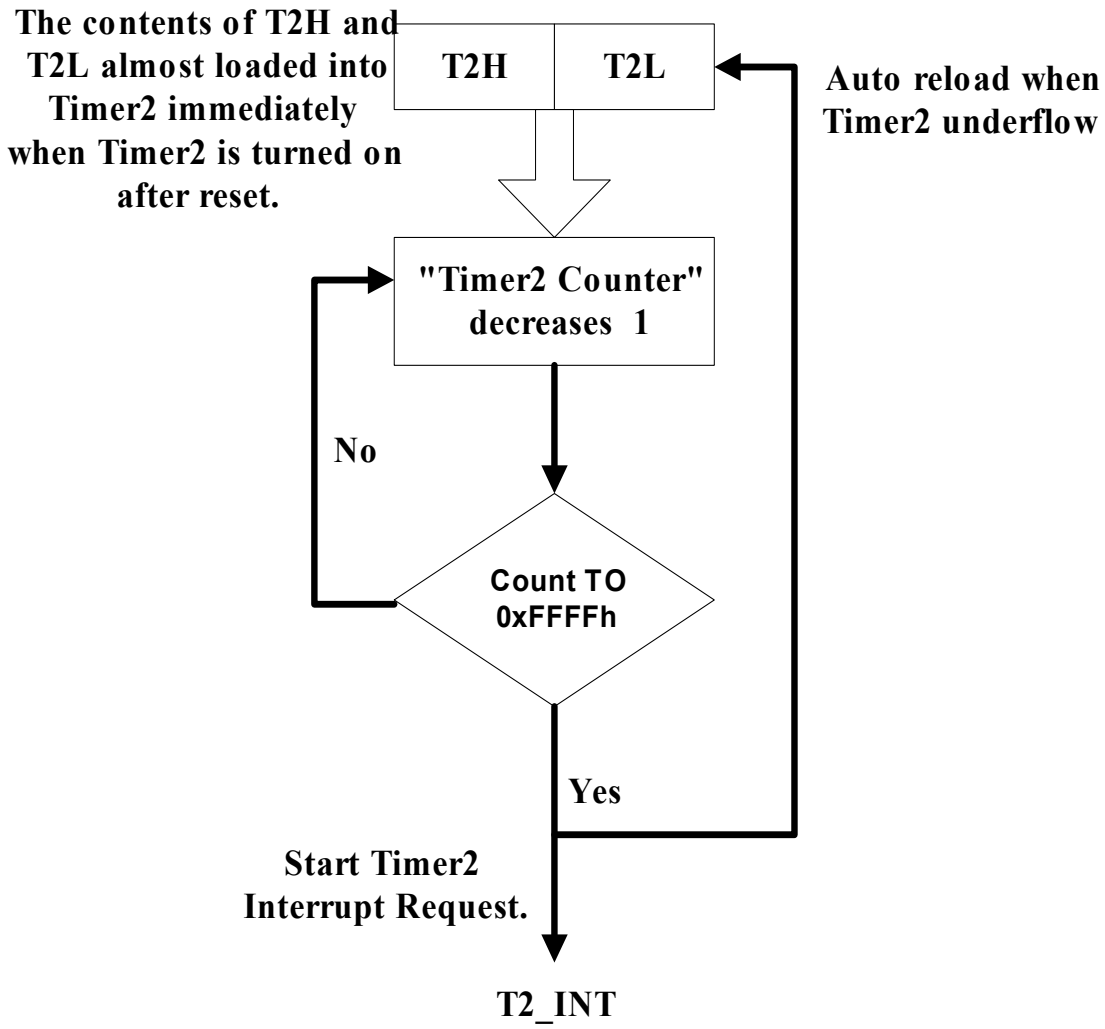
12. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded

with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.



The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.

13. Time Base Interrupt

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	W	W	W	W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

14. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution. WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

To use WDT function, “CLRWDT” instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the

program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

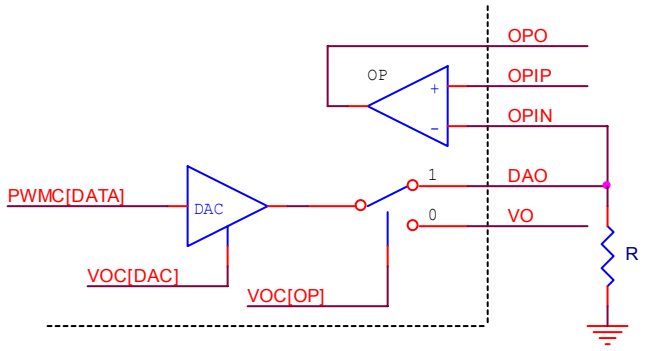
WDT is the enabling signal generated by calculating 32768-clock overflow. Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source. WDT function can be generated in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

15. Digital-to-Analog Converter

The Digital-to-Analog converter (DAC) converts the 7-bit unsigned speech data written to PWMC to proportional current output.

PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA & PWM Data	0	DA and PWM output value						
Control	1	PWM O/P driver			-	-	-	PWME

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.



The DAC is enabled by DAC bit of VOC register. Please note that the DAC bit of VOC register will be automatically cleared when the system enter Idle or Sleep mode. So it needs to be set again when returning to Normal mode.

VOC

VOC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Initial	-	-	-	-	-	0	0	0
	-	-	-	-	-	PWM	DAC	OP

Bit	Name	Value	Function description
1	DAC	1	DA Enable

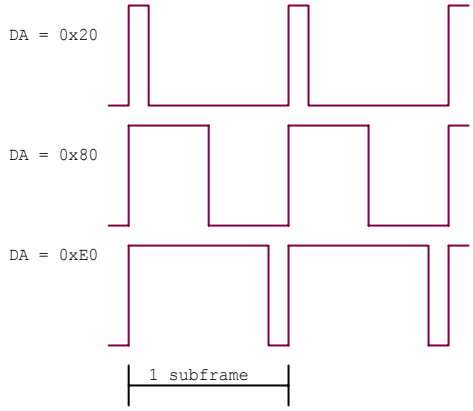
		0	DA Disable

The output current of the DAC is programmable by mask option MO_DACISEL:

MO_DACISEL[1:0]	DAC output current
00	0.375 mA
01	0.75 mA
10	1.5 mA
11	3 mA

16. Pulse-Width Modulation

The pulse-width modulator (PWM) converts 7-bit unsigned speech data written to PWMC data register to proportional duty cycle of PWM output. PWM module shares the PWMC data register with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the DA value.



The PWM bit of VOC register controls register to enable the circuit and output driver. When PWM bit of VOC is ‘0’, PWME bit and output drivers settings are both cleared. To use PWM for voice output, PWM bit has to be set to ‘1’ first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of PWMC command register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into Sleep mode or Idle mode, it will automatically turn off all voice outputs by clearing VOC[2..1] to ”00”. To activate voice output again when returning to Normal Mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register PWMC[6..4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

PWMC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

17. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 4.0V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

18. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 3.6V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =3.0V
		6MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

19. AC/DC Characteristics

Testing Condition : TEMP=25℃, VDD=3V±10%

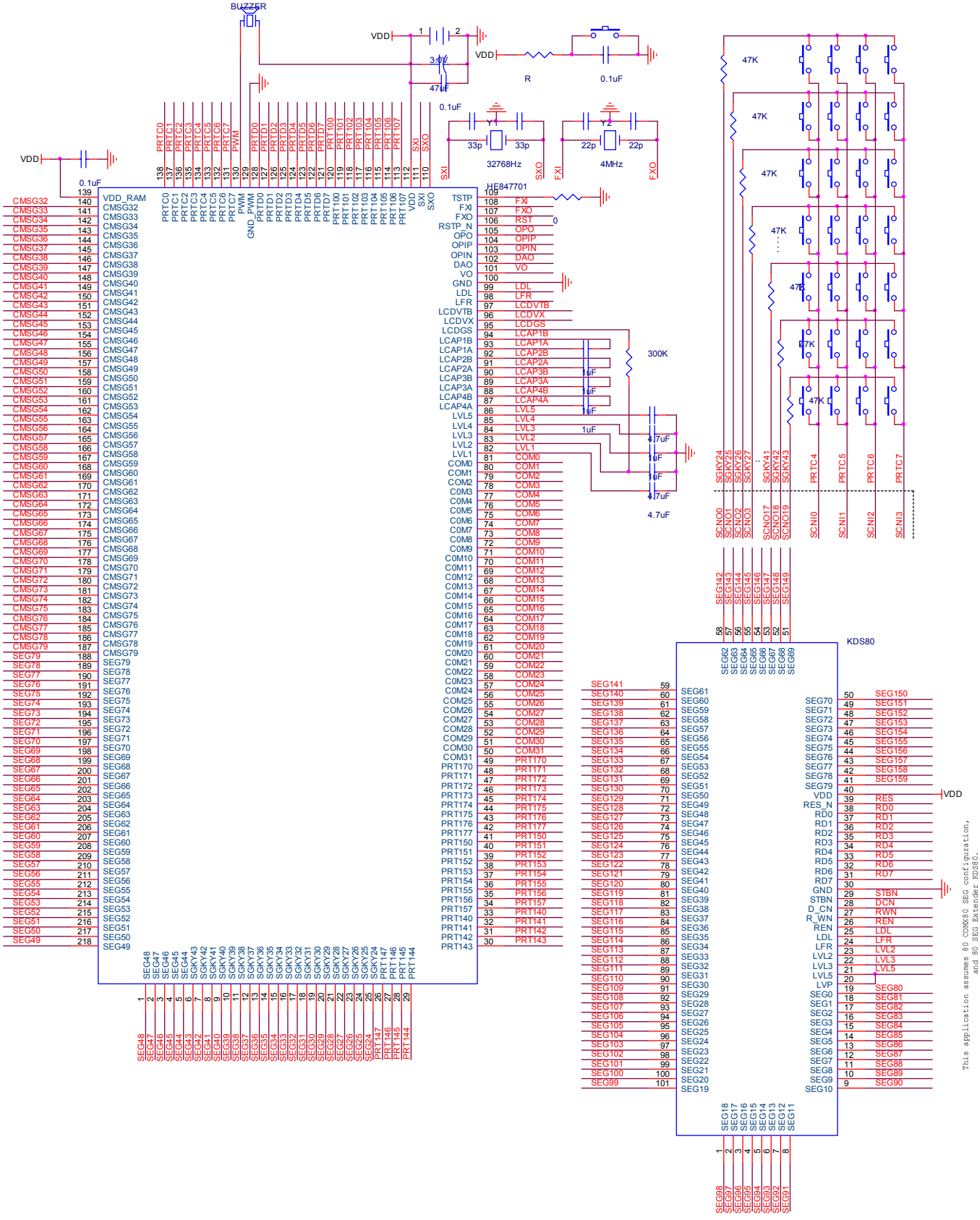
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Power consumption						
Normal mode current	I_{FAST}		1	1.5	mA	2M external R/C fast clock
Slow mode Current	I_{SLOW}		15	25	µA	32768 Hz slow clock with LCD disabled
Idle mode Current	I_{IDLE}		10	20	µA	32768 Hz slow clock with LCD disabled
Sleep mode Current	I_{SLEEP}			1	µA	
Additional Current if LCD ON	I_{LCD}		150	220	µA	1/7 bias, no load on SEG and COM pins
I/O specification						
Input High Voltage	V_{IH}	0.8			VDD	Input Pins
Input Low Voltage	V_{IL}			0.2	VDD	Input Pins
Input Hysteresis Width	V_{HYS}		1/3		VDD	I/O, RSTP_N Threshold = 2/3xVDD

						(Input from low to high), Threshold = 1/3xVDD (Input from high to low)
Output Source Current	I_{OH}	50			µA	Output drive high[*1], V_{OL}=2.0V
Output Sink Current	I_{OL1}	1.0			mA	Output drive low, V_{OL}=0.4V
Input Low Current	I_{IL1}		20		µA	RSTP_N, V_{IL} = GND, Pull high Internally
Input Low Current	I_{IL2}		100		µA	I/O, V_{IL}=GND, if pull high Internally by user
PWM and DAC						
PWM Output Current	I_{PWM}	10	14		mA	PWM [*2] With 32Ω Loading
		6	8		mA	With 64Ω Loading
		4	5		mA	With 100Ω Loading
DAC Output Current	I_{oVO}	2.5	3		mA	VO, DAO@ VDD=3V,VO=0~2V, Data = 7F

Notes:

1. The "Output Source Current" specification is applicable only to the Push-Pull I/O type.
2. This specification indicates only one PWM driving capability, and there are totally five built-in drivers, user can multiply the actual number of driver to get the actual current. (I_{PWM} x N; where N = 0, 1, 2, 3, 4, 5)

20. Application Circuit



21. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate accessing delay with ICE. So 5us delay should be added by firmware.
2. LCD driving circuit must be turned off before MCU goes into sleep mode.
3. Please bond the TSTP_P, RSTP_N and PRTD[7:0] with test points on PCB, which can be soldered and probed. Connect TSTP_P pin with zero ohm resistor to GND (or copper wire which can be cut easily on PCB) for good ESD protection. So that IC testing can be done on PCB, if necessary, by removing the 0-ohm resistor and driving TSTP_P pin to high.
4. LV5 must small than 8.5 Volt. Otherwise IC may breakdown.
5. Users must call the library "swap_page" in the file swappage.asm of AN029. The real IC register is different from ICE4.x or ICE5.x. This subroutine make sure that users can run on both real IC and ICE for page swapping. The program of swappage.asm as following:

```
.area       swapping_variable(data)
    _mapreg1::          .ds         1 ;store page register(R1Bh)
    _mapreg2::          .ds         1 ;store page register(R1Ch)

    .area       swapping_page(code,pag0)
        ;=======================================================
    ;swap page function
    ;=======================================================


    swap_page::
        lda   #10h
        sta   _mapreg1
        lda   #00h              ; P1E_O[2]    <--0      to enable Port R1Fh
        sta   r_iceco           ; R_ICECO is write only
        lda   _mapreg2
        sta   r_iced
        lda   _mapreg2
        anda#0fh
        ora   #20h      ;Mapping _mapreg2 low nibble to Logical segment2
    ;   sta   r1Ch
        sta   r_ps1
        lda   _mapreg2
```

```
        rorc
        rorc
        rorc
        rorc
        anda#0fh        ;Mapping _mapreg2 high nibble to Logical segment3
        ora  #30h
;       sta  r_ps1
        sta  r1Ch
        ret
```

22. Updated Record

Version	Date	Revision Description
1.0	2003/7/14	New Released
1.01	2003/11/5	Remove the LVD function
1.02	2004/1/16	Add the die size
1.03	2004/3/26	Correct application circuit errors