HITACHI COLOR IMAGING DEVICE

HE 98221

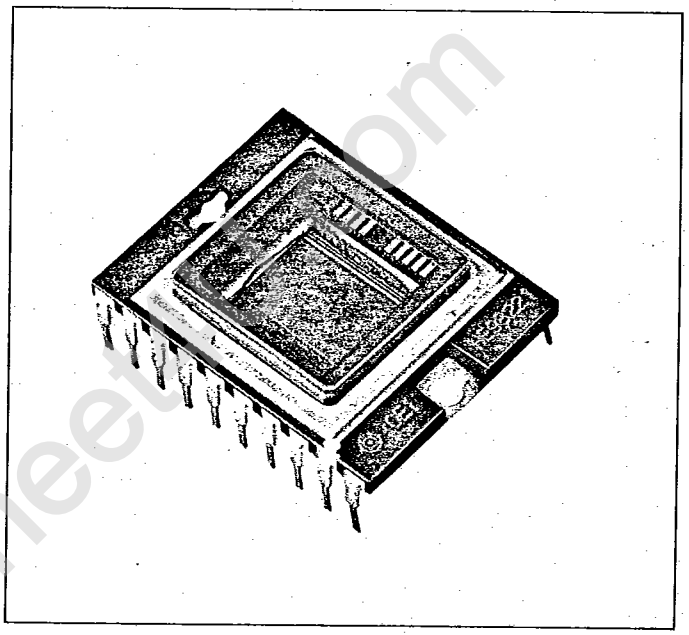
TENTATIVE DATA

HITACHI

The HE98221 is a MOS type imaging device. It contains n-p-n structure 384 x 485 picture elements with an on-chip color filter.

The size of the picture elements is 23μm (H) x 13.5μm (V). It provides horizontal resolution of 280 TV lines and vertical resolution of 350 TV lines.

This device is packaged in a 20-pin dual in-line package with an optical glass window.



■ Features

- 384 x 485 picture elements on a single chip.
- Resolution . . . . . 280 TV lines (horizontal)
  350 TV lines (vertical)
- Low voltage power supply requirements . . . . . below 7V.
- Low power dissipation . . . . 60 mW typical.
- No blooming
- On-chip color filter
- Hermetically sealed package
- Sensing area . . . . . 8.8 mm (H) x 6.6 mm (V)

■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Value	Unit
Operating temperature range		Topr	−10~60	°C
Storage temperature range		Tstg	−30~70	°C
Terminal voltage	Pin No. 1		0.0~9.0	V
	Pin No. 2		0.0~V_V	V
	Pin No. (*)		0.0~9.0	V
	Pin No. 10,15		0.0~0.7	V
Exposure value			500,000	1x · hour
Surface illumination			10,000	1x

Pin No. (*) : 3,4, 5, 6, 7, 8, 11, 12, 13, 14, 16, 17, 18, 19, 20

Note1: Operational temperature should be the temperature at the time when the horizontal and vertical shift registers operate, and when the picture signal is obtained.

2: Terminal voltage should be the value when Pin No. 9 is GND.

3: If the conditions of $V_{s1}=V_V$, $V_{s2}=V_V$, $V_{s3}=V_V$, $V_{s4}=V_V$ and $V_{SUB}\geqq V_V$ are not satisfied, voltage should not be applied.

4: If the condition of $V_{SUB}\geqq 6.5V$ is not satisfied, voltage should not be applied.

5: When the undershoot of pulse becomes less than 0.0V at Pin No. 20 (HIN), limit it within the range of the footnote of the pulse waveform standard table on page 6.

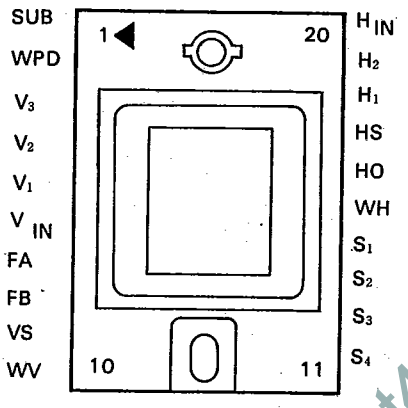


Fig. 1 Pin arrangement

Note: The information contained herein is tentative and way be changed without prior notice. It is therefore advisable to contact Hitachi before processing with the design of equipment in corporating this product.

■Recommended Operating Conditions

Pin No.	Pin name	Conditions (typical)
1	SUB	7.0 V
2	WPD	0.8 V
3 4 5 6 7 8	V_3 V_2 V_1 V_{IN} FA FB	Clock high level (ϕ_H) 7.0 V Clock low level (ϕ_L) 0.25 V (ϕ_L>0V)
9	VS	Ground 0.0 V
10	WV	Initial high level 0.65 V Initial low level 0.0 V
11 12	S_4 S_3	2.5 V
13 14	S_2 S_1	3.5 V
15	WH	Initial high level 0.65 V Initial low level 0.0 V
16	$H\bar{O}$	0.0 V
17	HS	0.0 V
18 19 20	H_1 H_2 H_{IN}	Clock high level (ϕ_H) 7.0 V Clock low level (ϕ_L) 0.25 V (ϕ_L>0 V)

■ Clock Characteristics (T_a=25°C)

Item		Symbol	Pin No.	min.	typ.	max.	unit
Field change clock	High level	V_{FAH} V_{FBH}	7, 8	6.65	7.0	7.35	V
	Low level	V_{FAL} V_{FBL}	7, 8	0	0.25	0.35	V
Vertical S.R. input clock	High level	V_{VINH}	6	6.65	7.0	7.35	V
	Low level	V_{VINL}	6	0	0.25	0.35	V
Horizontal S.R. input clock	High level	V_{HINH}	20	6.65	7.0	7.35	V
	Low level	V_{HINL}	20	0	0.25	0.35	V
Vertical S.R. transfer clock	High level	$V_{V1H,V2H,V3H}$	3,4,5	6.65	7.0	7.35	V
	Low level	$V_{V1L,V2L,V3L}$	3,4,5	0	0.25	0.35	V
Horizontal S.R. transfer clock	High level	$V_{B1H, B2H}$	18, 19	6.65	7.0	7.35	V
	Low level	$V_{H1L, H2L}$	18, 19	0	0.25	0.35	V
Initial pulse	High level	V_{WHH}, V_{WVH}	15	0.60	0.65	0.70	V
	Low level	V_{WHL}, V_{WVL}	15	0	0.0	0.05	V
Horizontal S.R. transfer clock frequency		f_{H1}, H_2	—	—	15.73	—	kHz
Horizontal S.R. input clock frequency		f_{HIN}	—	—	15.73	—	kHz
Vertical S.R. transfer clock frequency		f_{V1}, V_2, V_3	—	—	15.73	—	kHz
Vertical S.R. input clock frequency		f_{VIN}	—	—	60	—	Hz
Field change clock frequency		$f_{FA, FB}$	—	—	30	—	Hz

■ Capacitance (T_a =25°C, f=1MHz)

Item	Symbol	Test condition	typ.	max.	unit
S.R. transfer gate capacitance	$C_{H1, H2, H3}$	V=0 V	60	90	pF
	$C_{V1, V2}$	V=0 V	35	50	pF
S.R. input gate capacitance	$C_{HIN, VIN}$	V=0 V	10	15	pF
Field change gate capacitance	$C_{FA, FB}$	V=0 V	35	50	pF
Well capacitance	$C_{WV, WH}$	V=0 V	600	900	pF
Video output capacitance	$C_{S1, S2}$	V=2.7V, V_{SUB}=7V	15	28	pF
	$C_{S3, S4}$	V=1.7V, V_{SUB}=7V	17	30	pF

■ Electrical Characteristics (T_a =25°C)

Item		Symbol	Test condition	min.	typ.	max.	unit
Saturation signal current		$I_{W\ Sat}$	V_V=3.5V, L≃1.2L Sat	0.28	0.40		μAp-p
Sensitivity	(Yellow channel)	S_1	V_V=3.5V	1.55	2.15		nAp-p/lx
	(White channel)	S_2	V_V=3.5V	1.85	2.40		nAp-p/lx
	(Green channel)	S_3	V_V=2.5V	0.6	1.0		nAp-p/lx
	(Cyan channel)	S_4	V_V=2.5V	0.7	1.18		nAp-p/lx
Signal Uniformity	(Yellow signal)	SU_Y				±15	%
	(Red signal)	SU_R				±15	%
	(Blue signal)	SU_B				±20	%
Horizontal Resolution		R_H			280		TV lines
Vertical Resolution		R_V			350		TV lines
Gamma		γ			1		
Dark current		Id	V_V=3V, Ta=25°C			10	nA
Power dissipation		P			60	100	mW
Input sink current		I_{LI}	V_{SUB}=7.0 V Maximum rating voltage			10	μA

■ Application Circuit for HE98221

Block diagram of an application circuit is shown in Fig. 2. Fig. 3 shows a circuit configuration of FPN suppression circuit.

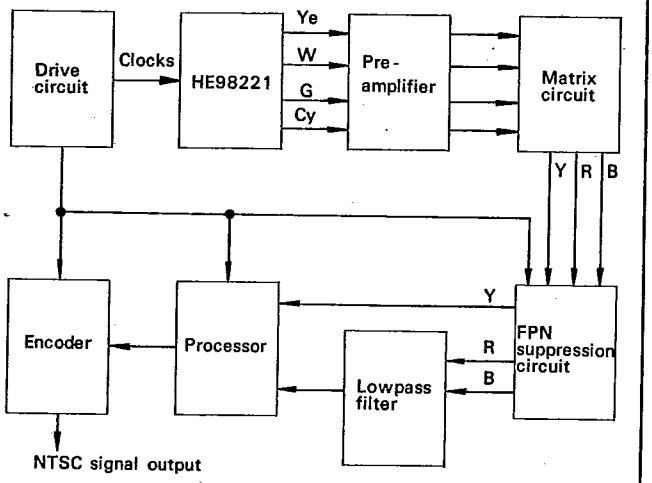


Fig. 2 Block diagram of an application circuit for HE98221

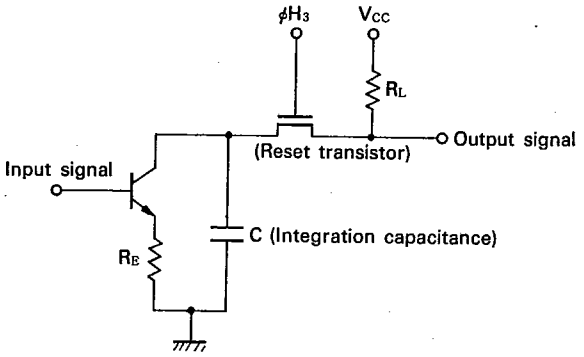


Fig. 3 Circuit configuration of FPN suppression circuit

■ Timing Sequence at Power On

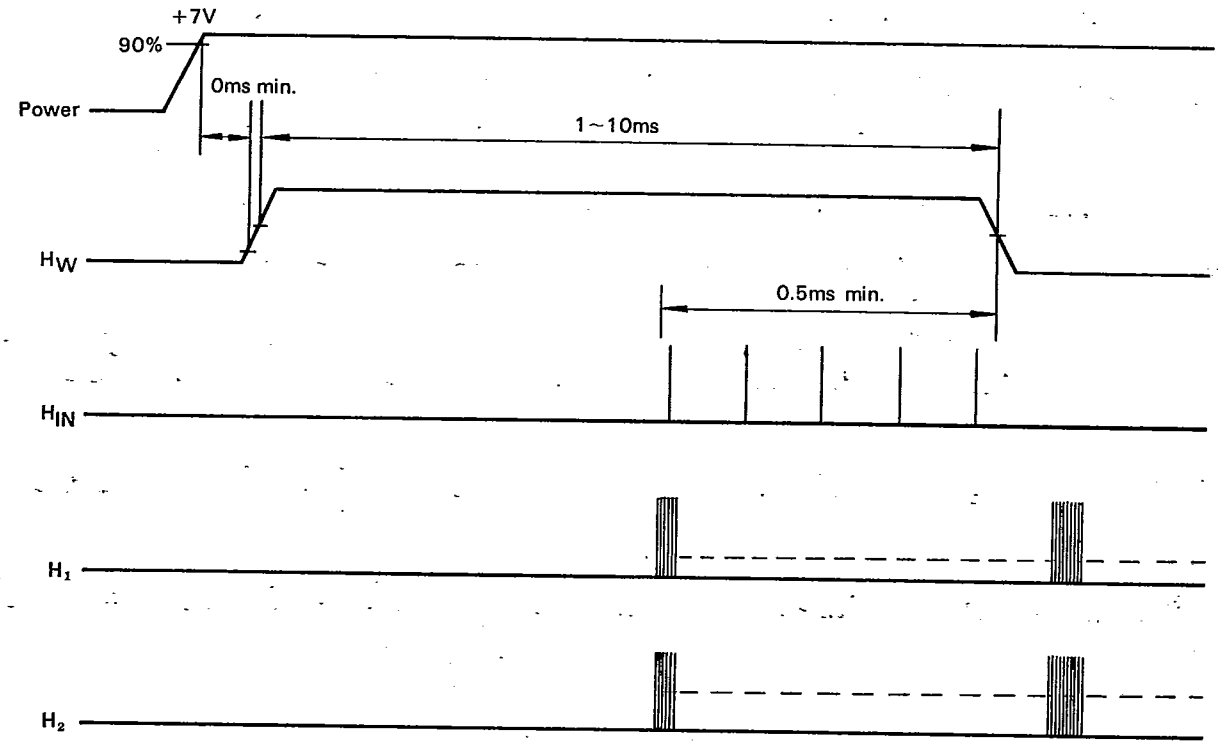
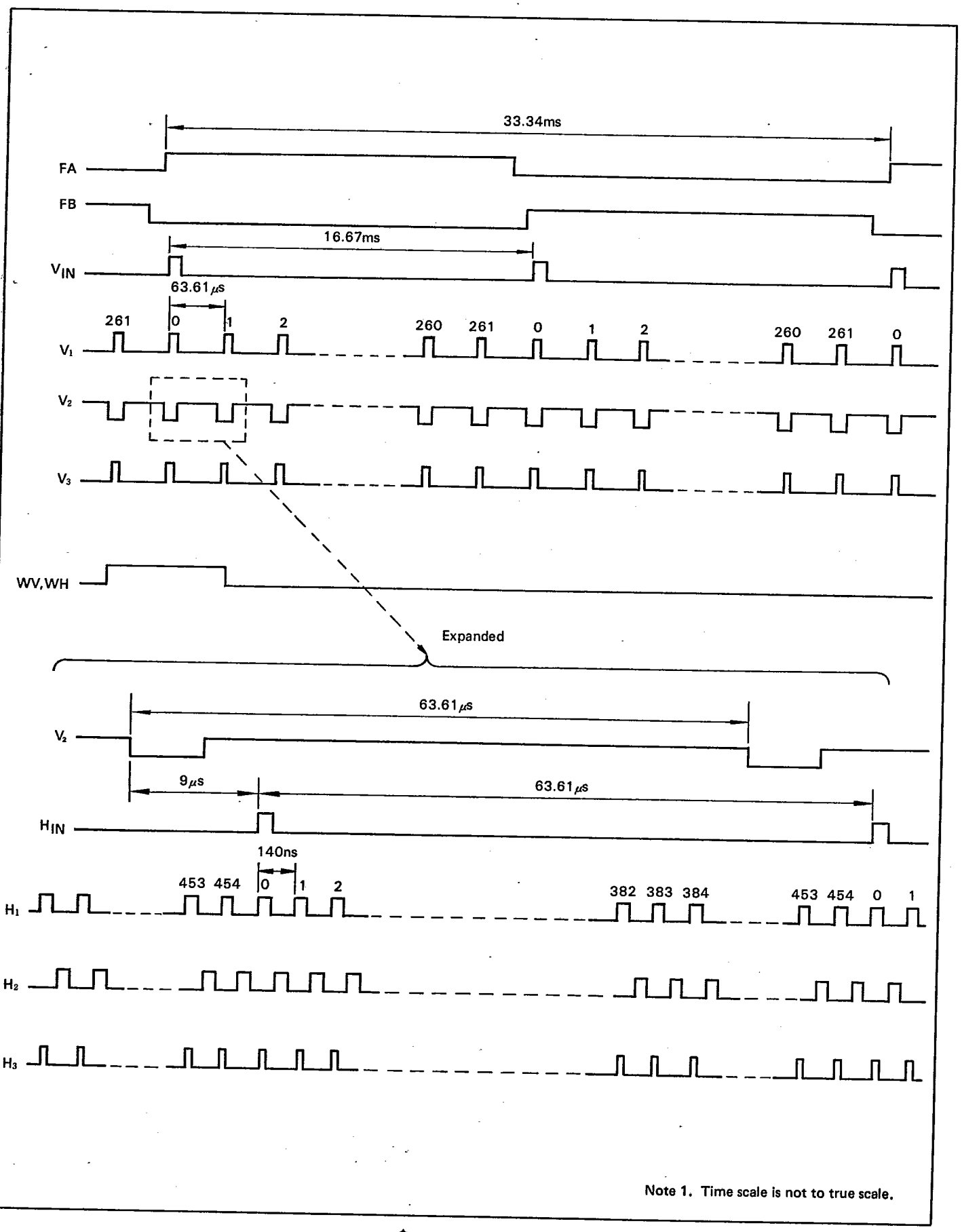


Fig. 4 Timing sequence at power on

■ Timing Pulses



Note 1. Time scale is not to true scale.

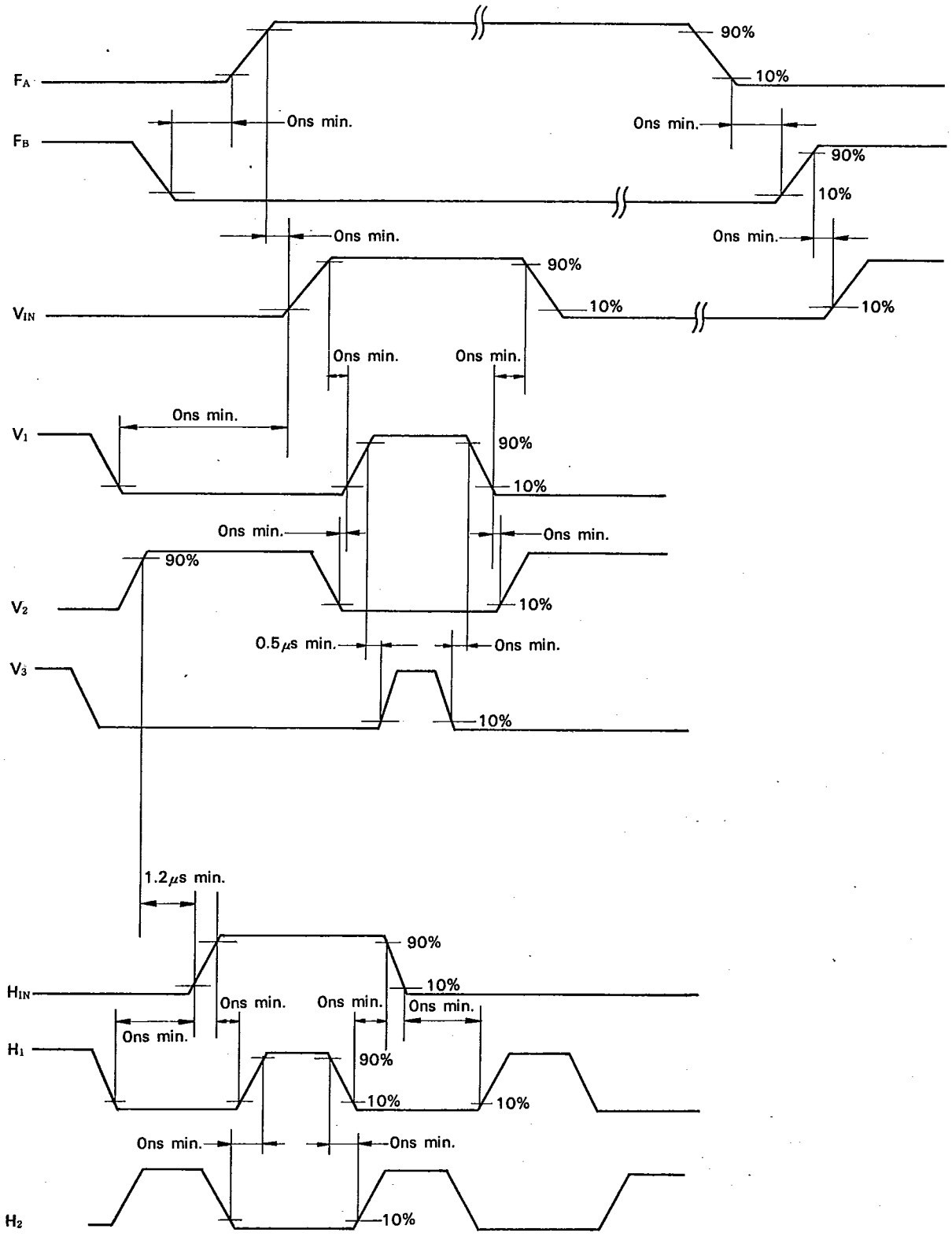


Fig. 5 Timing pulses

■ Typical Spectral Response Characteristics

Fig. 6 shows a typical spectral response of HE98221. Ye, W, G, CY stand for yellow color signal, white color signal, green color signal, and cyan color signal, respectively.

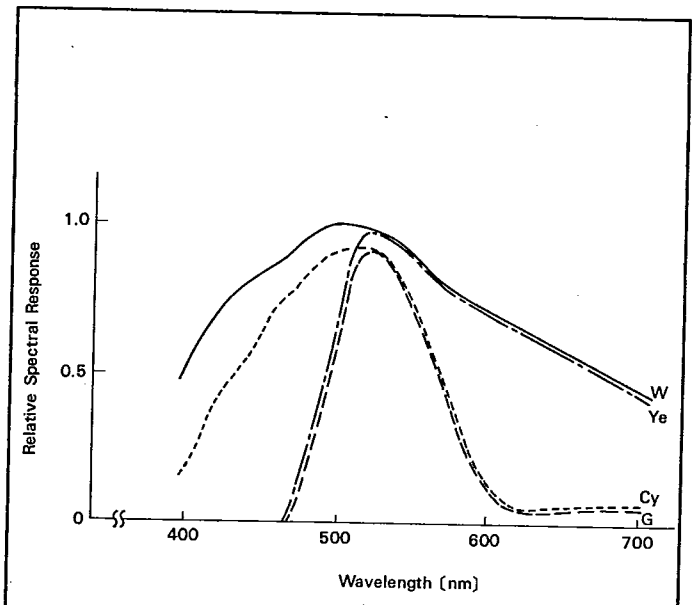
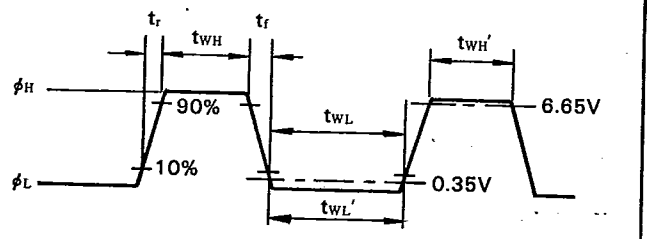
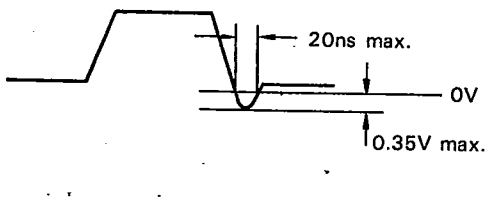


Fig. 6 Typical spectral response

■ Pulse Wave Form

Pin name	t_{WH}			t_{WH}'			t_{WL}			t_{WL}'			t_r			t_f			unit
	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
H_1	35	40	45	30	37		55	70		50	67		10	15	20	10	15	20	ns
H_2	35	40	45	30	37		55	70		50	67		10	15	20	10	15	20	ns
H_{IN}	65	100											10	15	20	10	15	20	ns
V_1	4.5	7.3											50 ns	0.2	0.5	50 ns	0.2	0.5	μs
V_2	54	56						7.7					50 ns	0.2	0.5	50 ns	0.2	0.5	μs
V_3	4.0	6.0											50 ns	0.2	0.5	50 ns	0.2	0.5	μs
V_{IN}	4.6	64											50 ns	0.1	0.5	50 ns	0.1	0.5	μs
FA	15.0	15.5												0.2 μs	0.5 μs		0.2 μs	0.5 μs	ms
FB	15.0	15.5												0.2 μs	0.5 μs		0.2 μs	0.5 μs	ms
WV	100	150	200											1	2		1	2	μs
WH	1	—	10																ms





Note: Pulse undershoot tolerance permissible range of Pin No. 20 (HIN).

■ Cautions in Handling

Protective register connect method

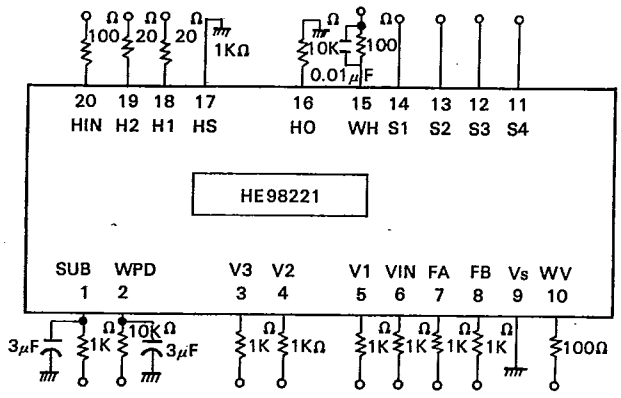


Fig 7. Protective register connect method

Cautions in Handling

(1) As imaging device HE98221 is MOS-LSI, take care of electrostatic breakdown. When handling, the body and instrument must be grounded. Moreover several hundred kiloohms registers should be added in series between the body and GND for safety, and to protect the device, add protective registers as stated above.

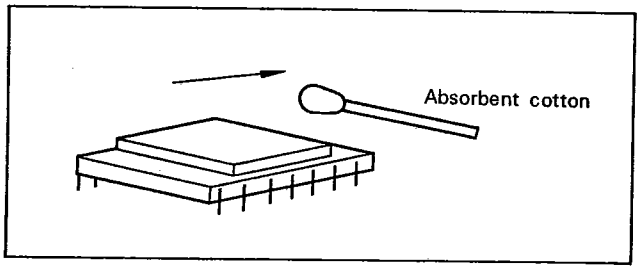
(2) V_{SUB} should be more than 6.5 volts when the voltage or the clockpulse is applied to the terminal. When turning off the power, turn off the voltage and the clockpulse under the condition that V_{SUB} is more than 6.5 volts.

(3) The above mentioned driving conditions assure the operation of the vertical and the horizontal shift registers, and obtaining the picture signals.

(4) Do not solder on the kovar metal at the back because color filter will be decomposed and the device will be damaged.

(5) Take care when handling the device because 7 volts (typical) is applied to the kovar metal at the back of the device under operating condition.

(6) When handling the device, do not touch the glass. In case you touch it and leave fingerprints on it, wipe it slowly and gently with absorbent cotton after moistening with your breath. (From left to right, about once a second)



(7) Take care not to drop the device because the glass cap is fragile.

(8) When storing and carrying the device, keep in its case. When instailing in the camera, do not expose the device to light except under operating conditions.

■ Dimensional Outline

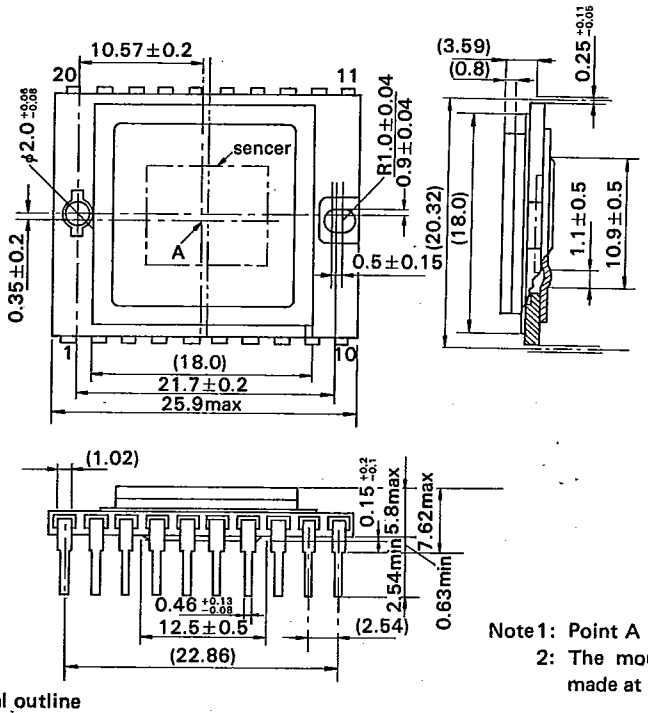


Fig. 8 Dimensional outline

Note 1: Point A is the center of the photodiode array.
2: The mounting standard of the package should be the holes made at both edges and the flat part of the mount back.