

# HEF4007UB

## Dual complementary pair and inverter

Rev. 4 — 31 August 2017

Product data sheet

## 1 General description

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## 2 Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

## 3 Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
HEF4007UBT		$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

## 4 Functional diagram

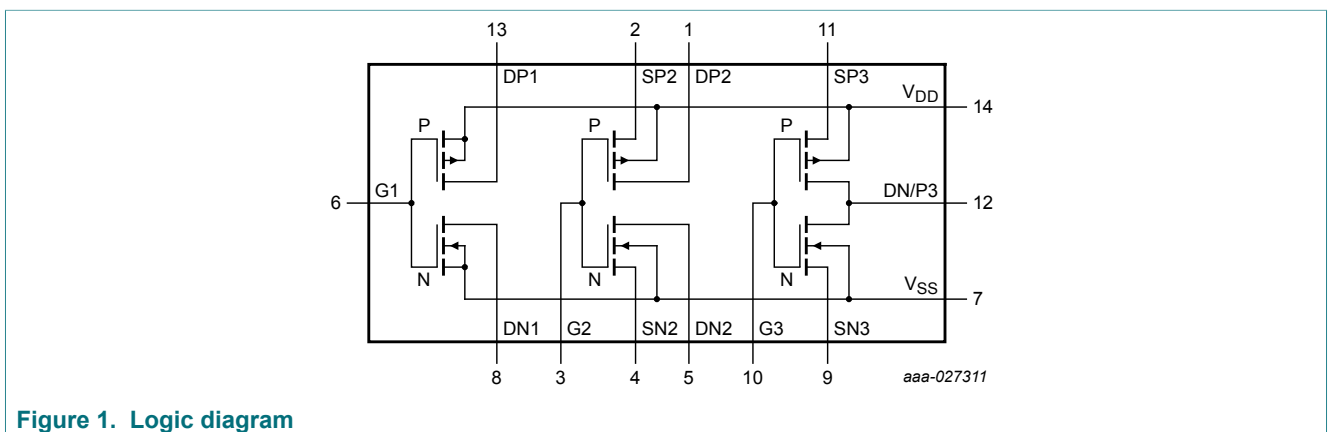
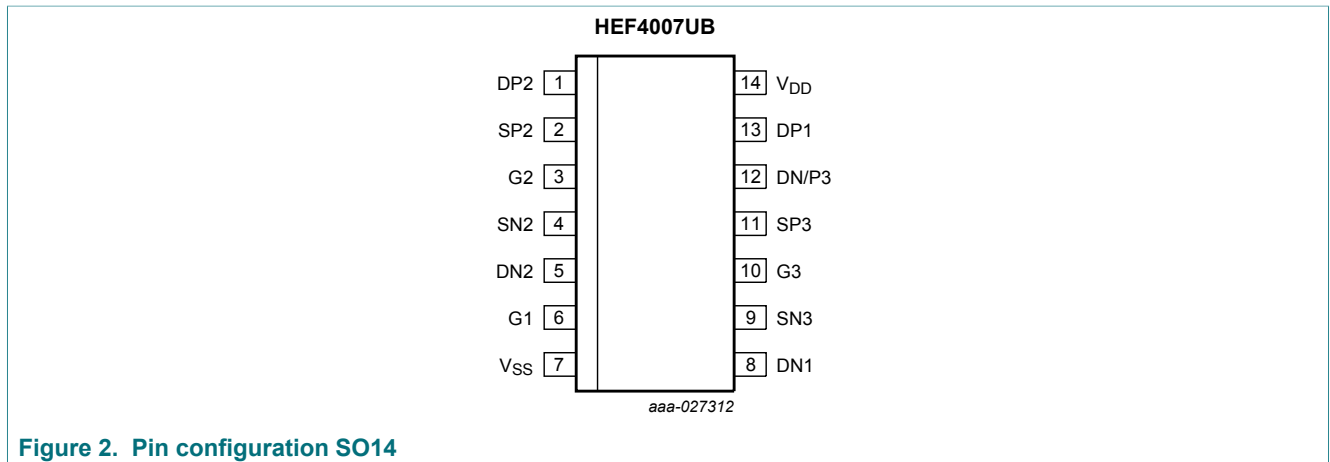


Figure 1. Logic diagram

## 5 Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
DP1, DP2	13, 1	drain connections from the 1st and 2nd p-channel transistors
SP2, SP3	2, 11	source connections to 2nd and 3rd p-channel transistors
G1, G2, G3	6, 3, 10	gate connections to n-channel and p-channel of the three transistor pairs
SN2, SN3	4, 9	source connections to the 2nd and 3rd n-channel transistors
DN1, DN2	8, 5	drain connection from the 1st and 2nd n-channel transistors
DN/P3	12	common connection to the 3rd p-channel and n-channel transistor drains
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

## 6 Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0\text{ V}$  (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current		-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current		-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C to } +85\text{ °C}$			
		SO14 [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO14 packages: above  $T_{amb} = 70\text{ °C}$ ,  $P_{tot}$  derates linearly with 8 mW/K.

## 7 Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 8 Static characteristics

**Table 5. Static characteristics**
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = +25\text{ }^{\circ}\text{C}$		$T_{amb} = +85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_O = 0.5\text{ V}$ or $4.5\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	5 V	4	-	4	-	4	-	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	10 V	8	-	8	-	8	-	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	15 V	12.5	-	12.5	-	12.5	-	V
$V_{IL}$	LOW-level input voltage	$V_O = 0.5\text{ V}$ or $4.5\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1	-	1	-	1	V
		$V_O = 1.0\text{ V}$ or $9.0\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	10 V	-	2	-	2	-	2	V
		$V_O = 1.5\text{ V}$ or $13.5\text{ V}$ ; $ I_O  < 1\text{ }\mu\text{A}$	15 V	-	2.5	-	2.5	-	2.5	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{SS}$ or $V_{DD}$ ; $ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{SS}$ or $V_{DD}$ ; $ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output (source) current	$V_O = 2.5\text{ V}$ ; $V_I = 0\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$ ; $V_I = 0\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$ ; $V_I = 0\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$ ; $V_I = 0\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output (sink) current	$V_O = 0.4\text{ V}$ ; $V_I = 5\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$ ; $V_I = 10\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$ ; $V_I = 15\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current	$V_I = 0\text{ V}$ to $15\text{ V}$	15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $V_I = V_{SS}$ or $V_{DD}$ ; $I_O = 0\text{ A}$	5 V	-	1.0	-	1.0	-	7.5	$\mu\text{A}$
			10 V	-	2.0	-	2.0	-	15.0	$\mu\text{A}$
			15 V	-	4.0	-	4.0	-	30.0	$\mu\text{A}$

## 9 Dynamic characteristics

**Table 6. Dynamic characteristics**

$T_{amb} = 25\text{ °C}$ ; for waveforms see [Figure 3](#); for test circuit see [Figure 4](#); unless otherwise specified.

Symbol	Parameter	Conditions	Extrapolation formula <sup>[1]</sup>	V <sub>DD</sub>	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	Gn to Dn or DP	$13 + 0.55 \times C_L$	5 V	-	40	80	ns
			$9 + 0.23 \times C_L$	10 V	-	20	40	ns
			$7 + 0.16 \times C_L$	15 V	-	15	30	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	Gn to Dn or DP	$13 + 0.55 \times C_L$	5 V	-	40	75	ns
			$9 + 0.23 \times C_L$	10 V	-	20	40	ns
			$7 + 0.16 \times C_L$	15 V	-	15	30	ns
t <sub>t</sub>	output transition time <sup>[2]</sup>		$10 + 1.0 \times C_L$	5 V	-	60	120	ns
			$9 + 0.42 \times C_L$	10 V	-	30	60	ns
			$6 + 0.28 \times C_L$	15 V	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula ( $C_L$  in pF).

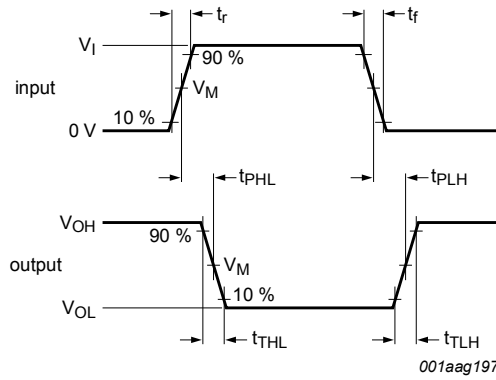
[2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

**Table 7. Dynamic power dissipation**

$V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	V <sub>DD</sub>	Typical formula	Where
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	$P_D = 20000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	
		15 V	$P_D = 50000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	

9.1 Waveforms and test circuit



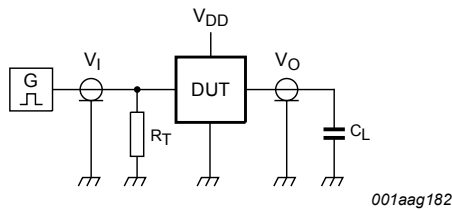
Measurement points are given in Table 8.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Figure 3. Propagation delay, output transition time

Table 8. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 9.

Definitions for test circuit:

$C_L$  = load capacitance including jig and probe capacitance.

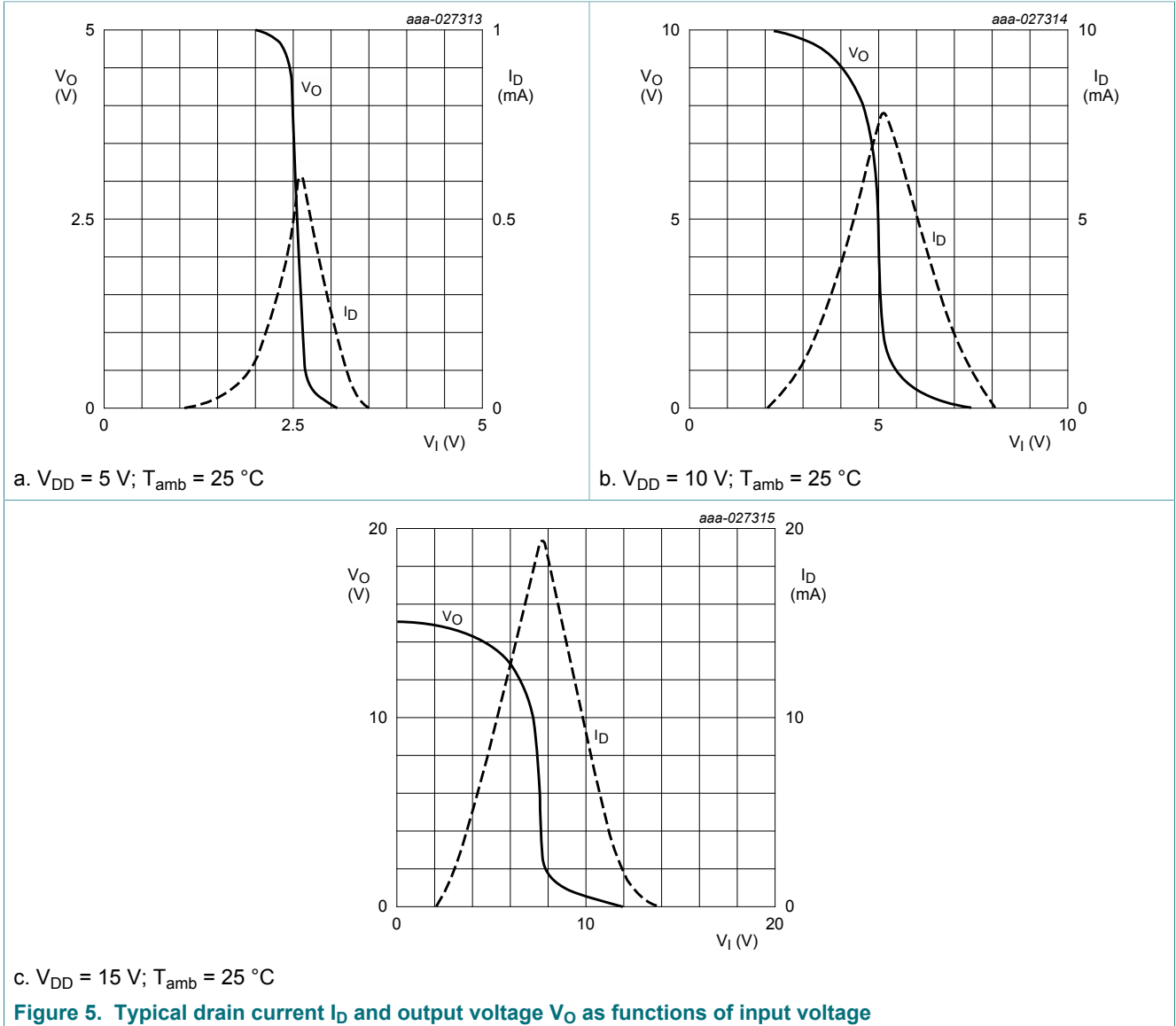
$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Figure 4. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns
		50 pF

9.2 Characteristics



## 10 Application information

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers

Note:

Rules for maintaining electrical isolation between transistors and monolithic substrate:

- The  $V_{DD}$  supply pin (Pin 14) must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.
- The  $V_{SS}$  ground pin (Pin 7) must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.

Figure 6 and Figure 7 show voltage gain and supply current. Figure 8 shows the test set-up and an example of an analog amplifier using one HEF4007UB.

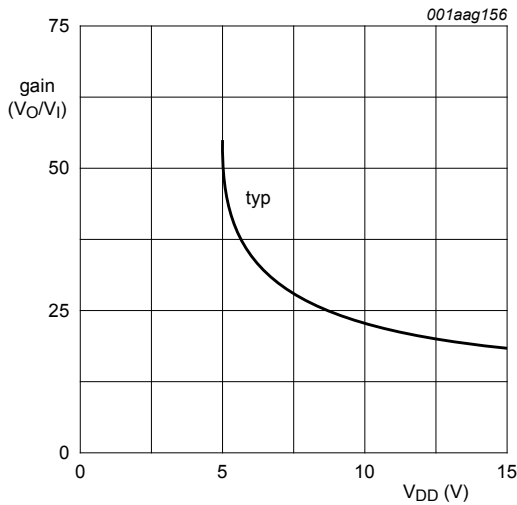


Figure 6. Typical voltage gain as a function of supply voltage

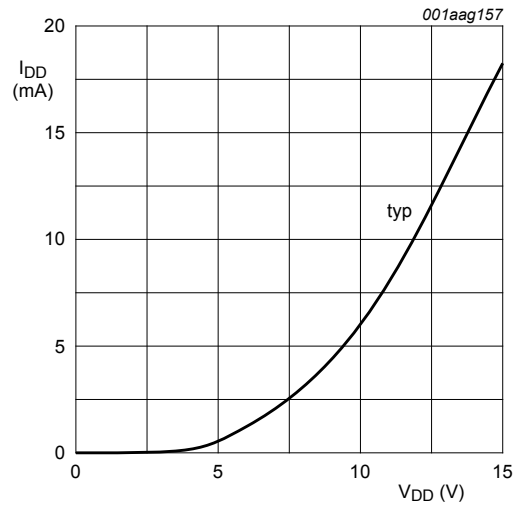


Figure 7. Typical supply current as a function of supply voltage

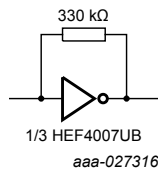


Figure 8. Test set-up



Figure 9 shows typical forward transconductance and Figure 10 shows the test set-up.

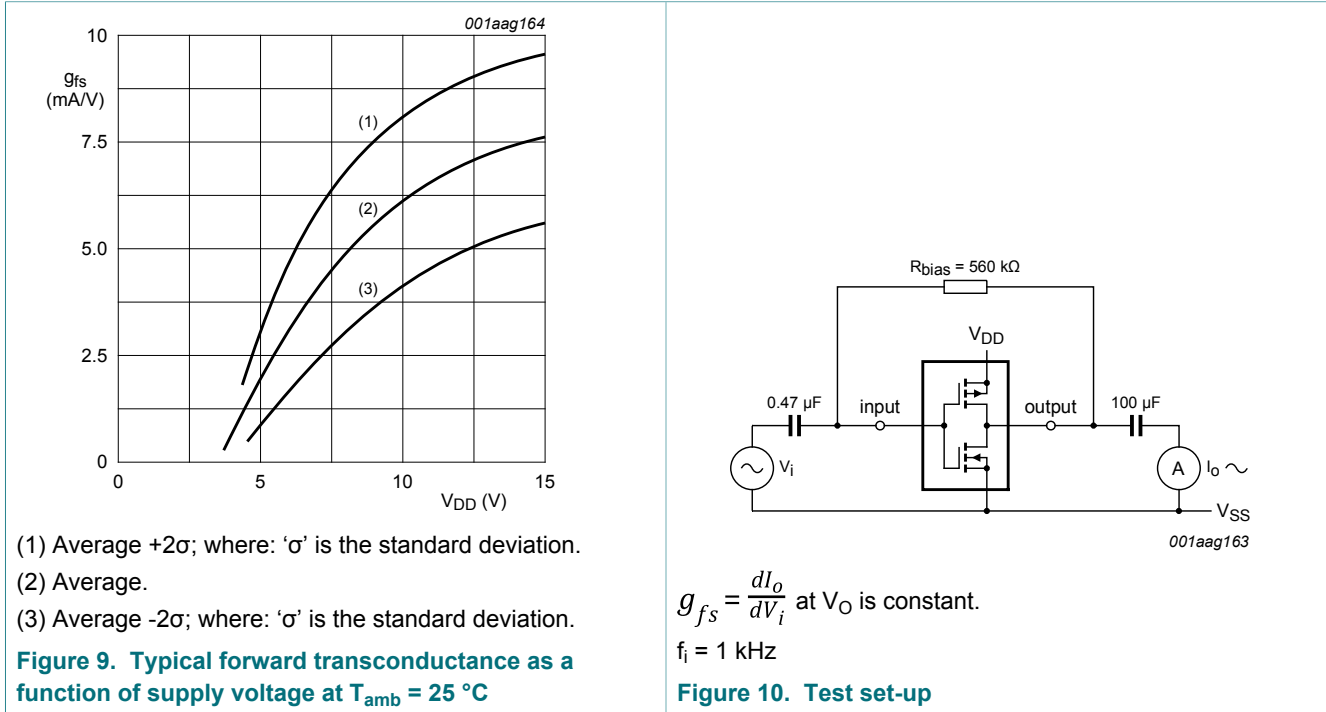
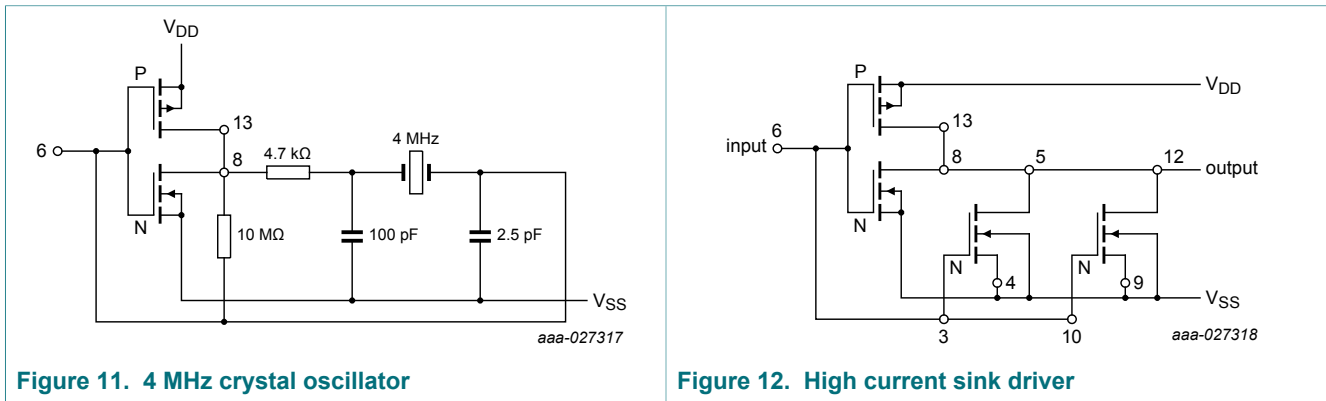


Figure 11, Figure 12, Figure 13 and Figure 14 show some applications in which the HEF4007UB is used.



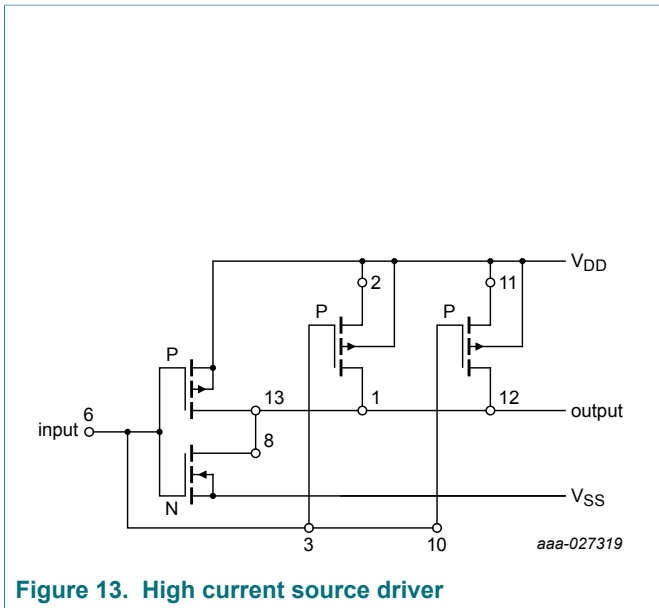


Figure 13. High current source driver

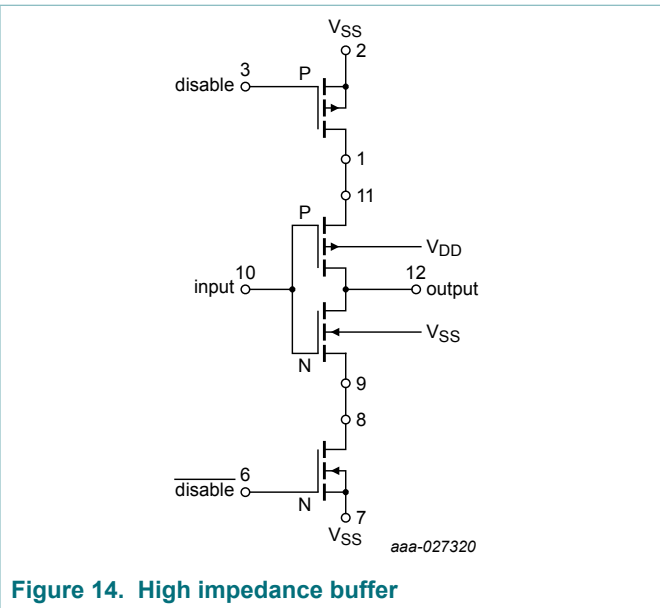


Figure 14. High impedance buffer

Table 10. Function table <sup>[1]</sup>

For Figure 14. High impedance buffer

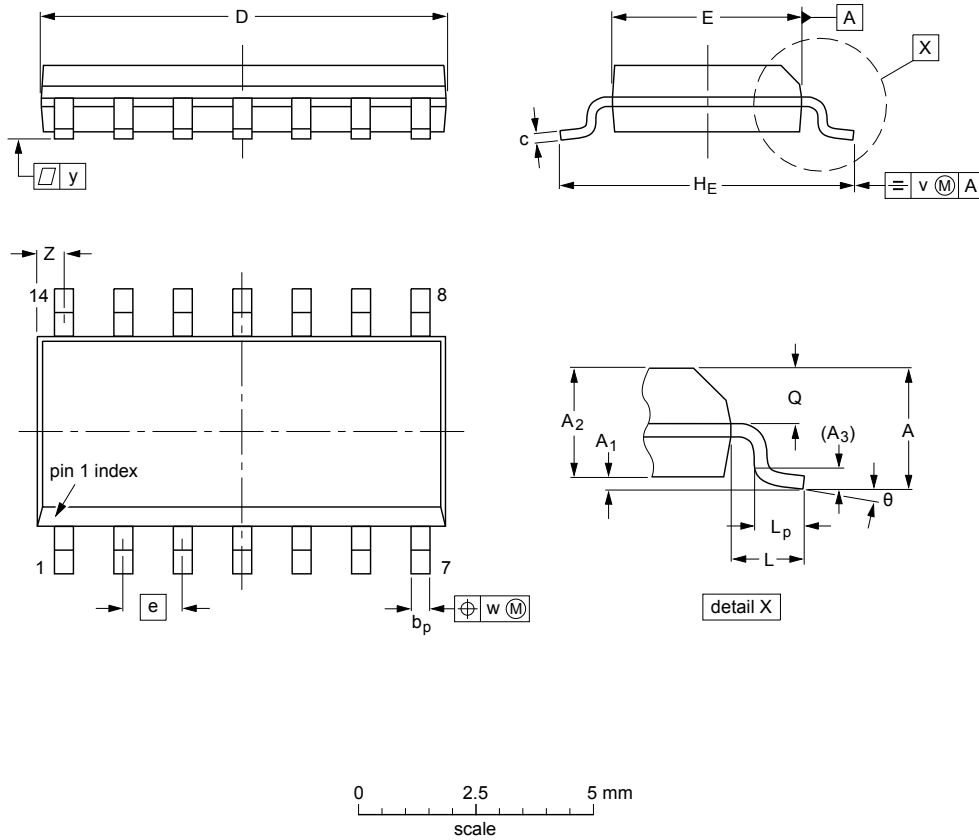
Input	Disable	Output
H	L	L
L	L	H
X	H	Z

[1] H = HIGH state (the more positive voltage);  
 L = LOW state (the less positive voltage);  
 X = state is immaterial  
 Z = HIGH-impedance OFF-state

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 15. Package outline SOT108-1 (SO14)

## 12 Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
MOS	Metal Oxide Semiconductor

## 13 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4007UB v.4	20170831	Product data sheet	-	HEF4007UB v.3
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number HEF4007UBP and HEF4007UBD removed.</li></ul>			
HEF4007UB v.3	19951201	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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