

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4014B

MSI

8-bit static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

8-bit static shift register

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DESCRIPTION

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (P_0 to P_7), a synchronous serial data input (D_S), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (O_5 to O_7).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop. When PE is HIGH, data is loaded into the register from P_0 to P_7 on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first position from D_S , and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times

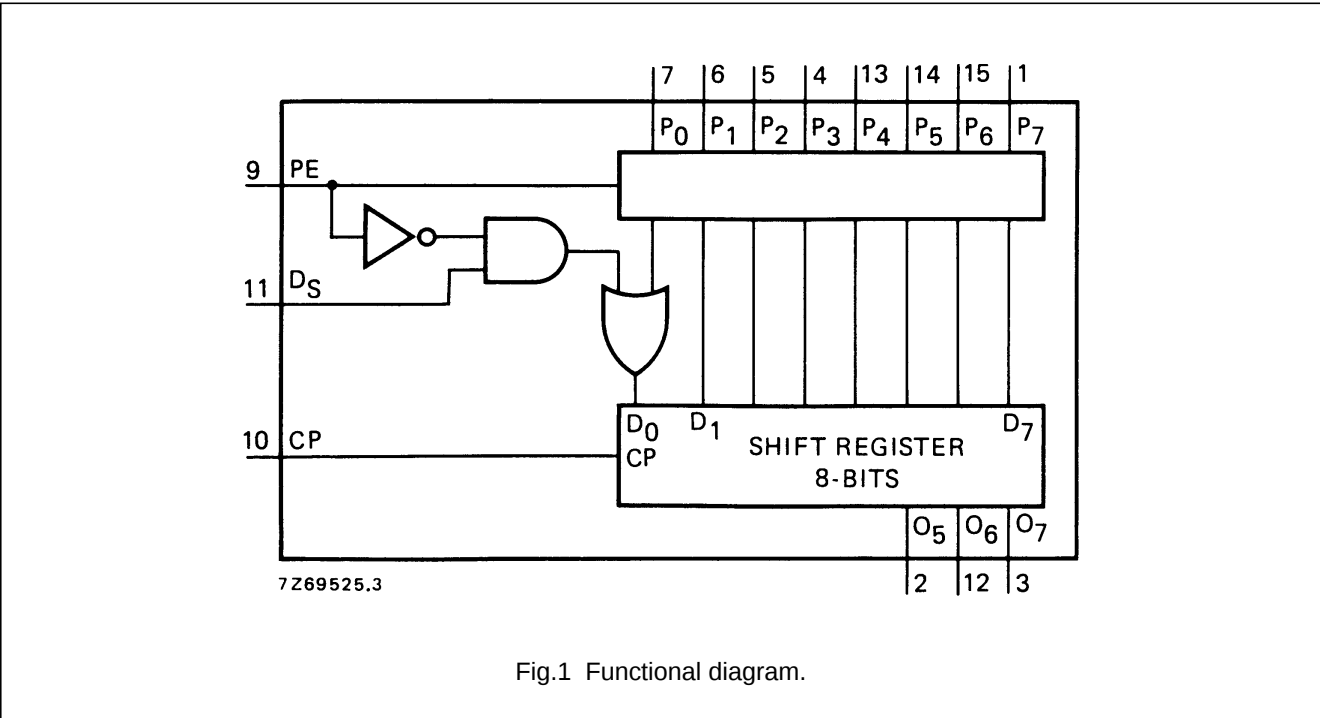


Fig.1 Functional diagram.

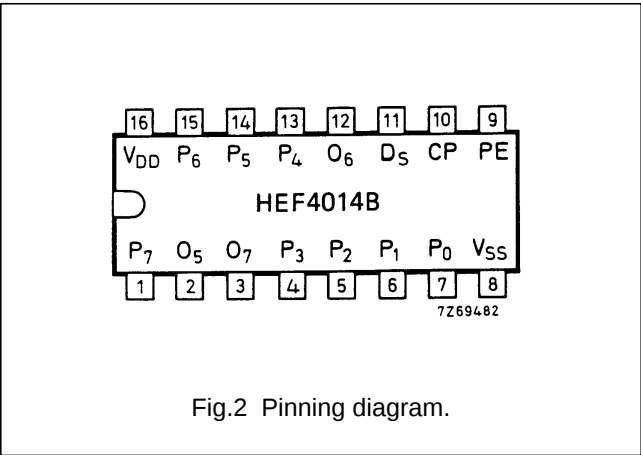


Fig.2 Pinning diagram.

- HEF4014BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4014BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4014BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI
See Family Specifications

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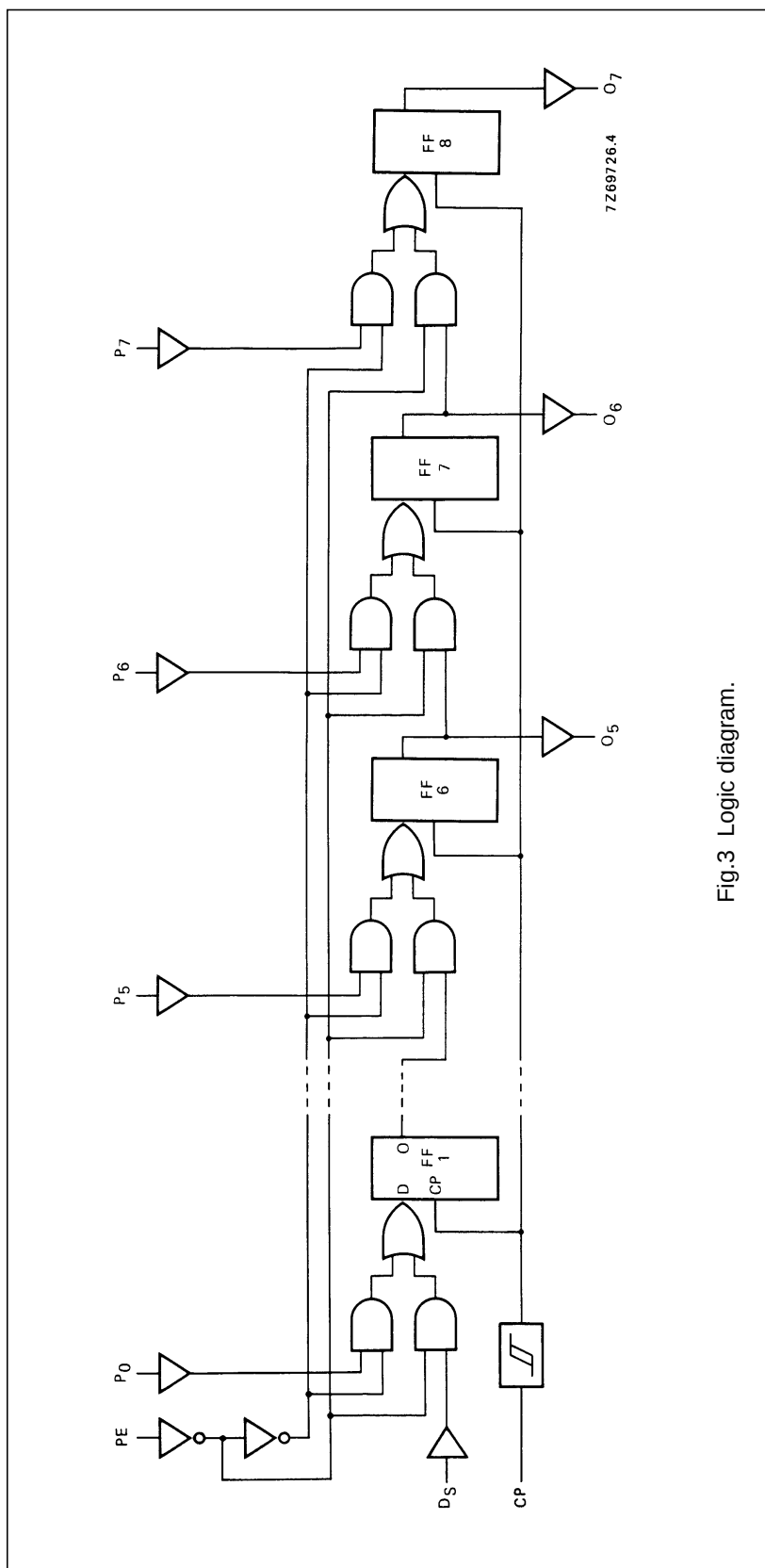


Fig.3 Logic diagram.

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PINNING

- PEparallel enable input
- P₀ to P₇parallel data inputs
- D_Sserial data input
- CPclock input (LOW to HIGH edge-triggered)
- O₅ to O₇buffered parallel outputs from the last three stages

FUNCTION TABLES

Serial operation

n	INPUTS			OUTPUTS		
	CP	D _S	PE	O ₅	O ₆	O ₇
1		D ₁	L	X	X	X
2		D ₂	L	X	X	X
3		D ₃	L	X	X	X
6		X	L	D ₁	X	X
7		X	L	D ₂	D ₁	X
8		X	L	D ₃	D ₂	D ₁
		X	X	no change		

Parallel operation

n	INPUTS			OUTPUTS		
	CP	D _S	PE	O ₅	O ₆	O ₇
1		X	H	P ₅	P ₆	P ₇
		X	X	no change		

Notes

1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
-  = positive-going transition
-  = negative-going transition
- D_n = either HIGH or LOW
- n = number of clock pulse transitions

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	900 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load cap. (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	4 300 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	12 000 f _i + ∑ (f _o C _L) × V _{DD} ²	

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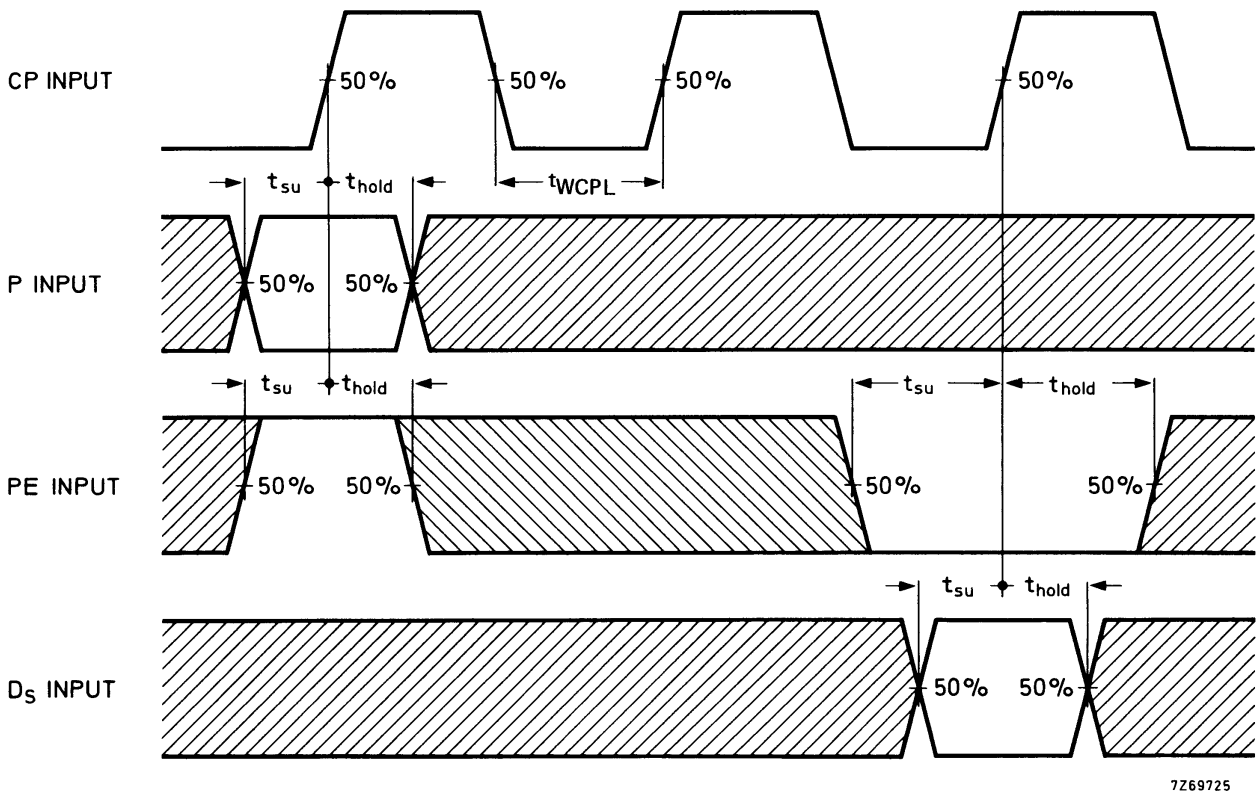
AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays C _P → O _n HIGH to LOW	5 10 15	t _{PHL}		130 55 40	260 110 80 ns	103 ns + (0,55 ns/pF) C _L 44 ns + (0,23 ns/pF) C _L 32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5 10 15	t _{PLH}		115 50 40	230 100 80 ns	88 ns + (0,55 ns/pF) C _L 39 ns + (0,23 ns/pF) C _L 32 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5 10 15	t _{THL}		60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C _L 9 ns + (0,42 ns/pF) C _L 6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5 10 15	t _{TLH}		60 30 20	120 60 40 ns	10 ns + (1,0 ns/pF) C _L 9 ns + (0,42 ns/pF) C _L 6 ns + (0,28 ns/pF) C _L
Set-up times PE → CP	5 10 15	t _{su}	40 25 15	10 5 0	ns ns ns	see also waveforms Fig.4
D _S → CP	5 10 15	t _{su}	35 25 25	− 5 −5 0	ns ns ns	
P _n → CP	5 10 15	t _{su}	35 25 25	−5 −5 0	ns ns ns	
Hold times PE → CP	5 10 15	t _{hold}	25 20 15	−5 0 0	ns ns ns	
D _S → CP	5 10 15	t _{hold}	30 20 15	15 10 7	ns ns ns	
P _n → CP	5 10 15	t _{hold}	30 20 15	15 10 7	ns ns ns	
Minimum clock pulse width; LOW	5 10 15	t _{WCPL}	70 30 24	35 15 12	ns ns ns	
Maximum clock pulse frequency	5 10 15	f _{max}	6 15 20	13 30 40	MHz MHz MHz	

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Fig.4 Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, D_S to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF4014B are:

- Parallel-to-serial converter
- Serial data queueing
- General purpose register