DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40163B
MSI
4-bit synchronous binary counter with synchronous reset

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

4-bit synchronous binary counter with synchronous reset

HEF40163B MSI

DESCRIPTION

The HEF40163B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_0 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

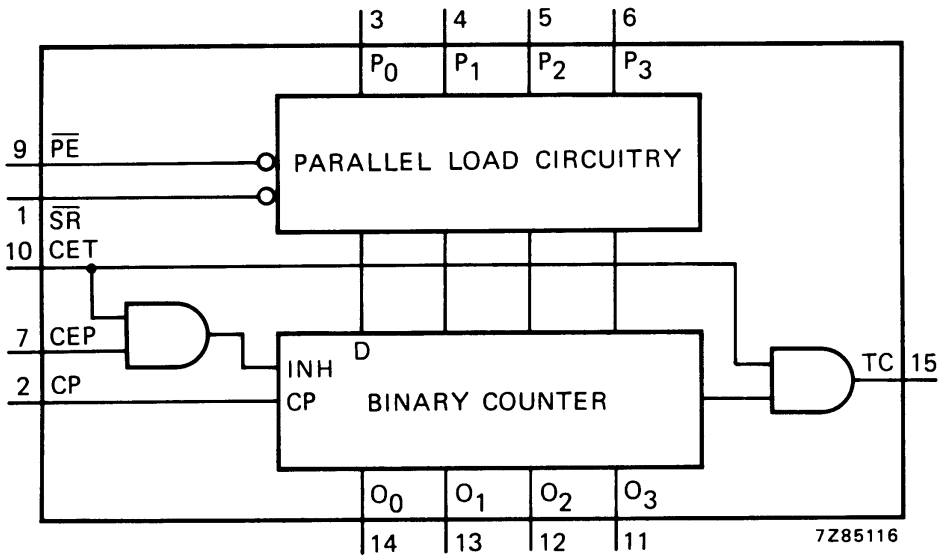


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

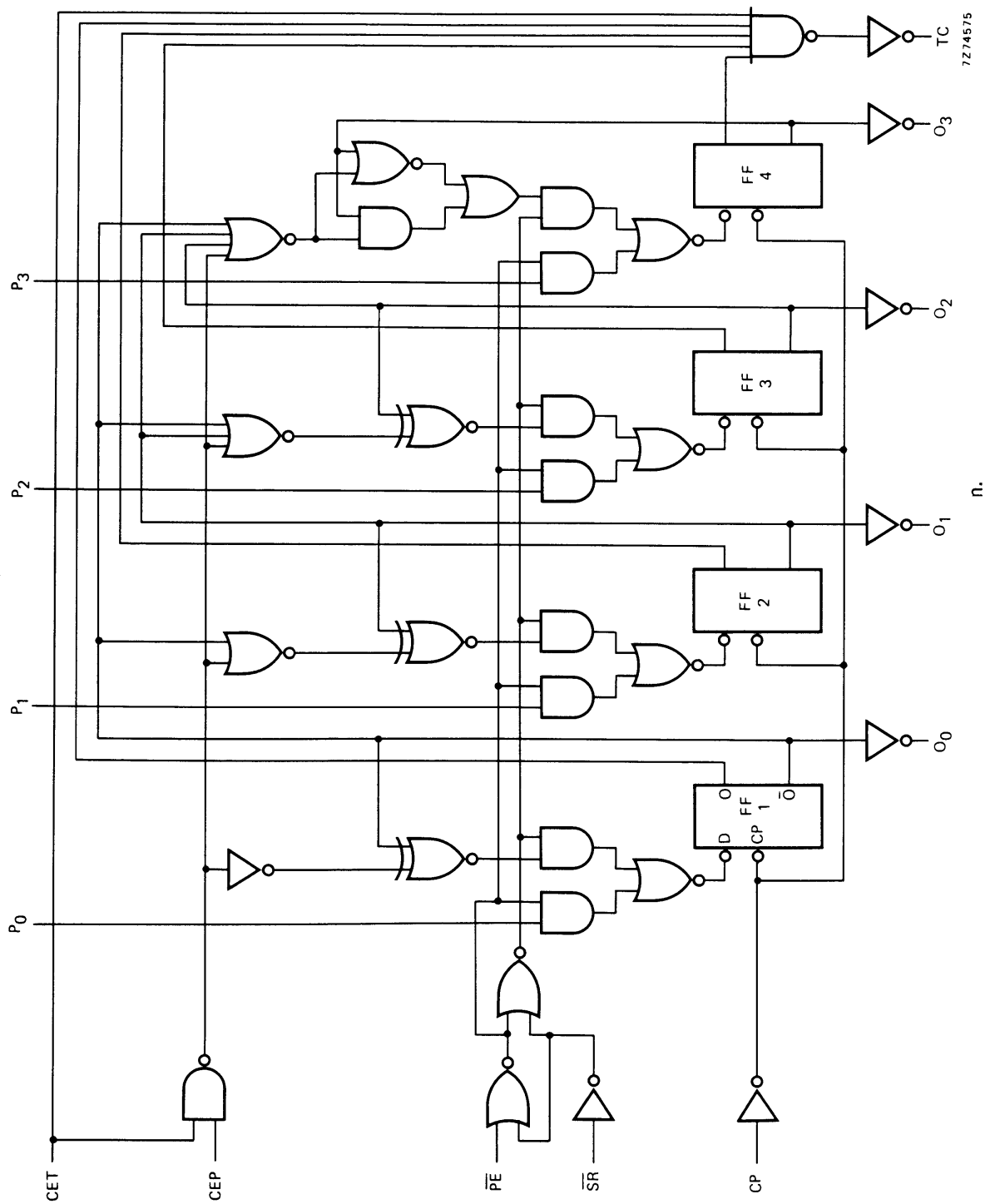


Fig.2 Logic diagram.

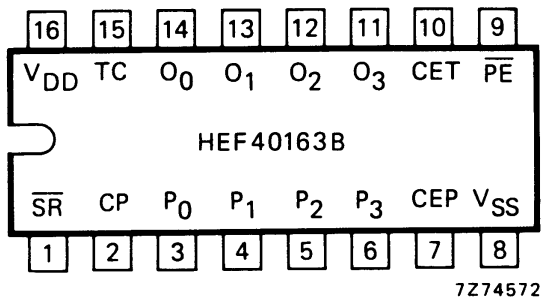


Fig.3 Pinning diagram.

PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{SR}$	synchronous reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

HEF40163BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40163BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40163BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. $TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$

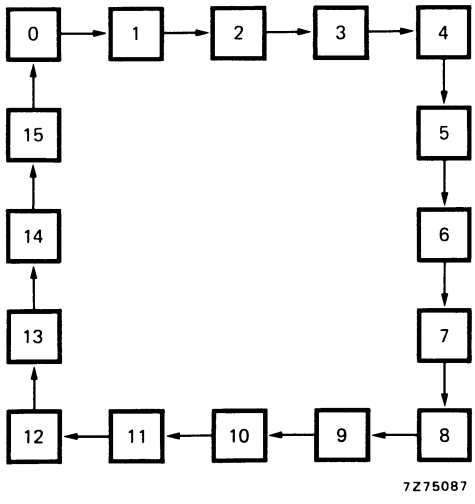


Fig.4 State diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 200 $f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5 600 $f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	16 000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	

AC CHARACTERISTICS

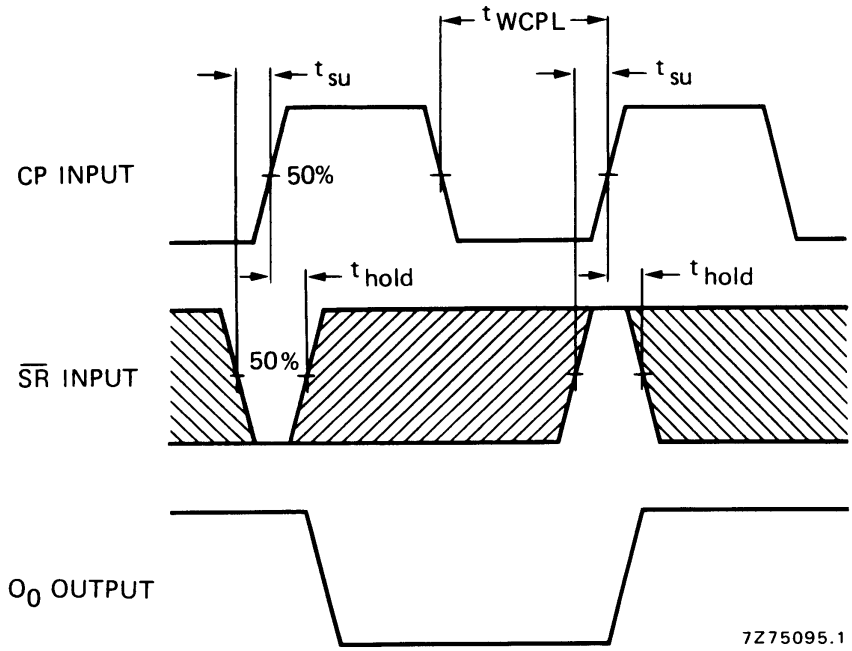
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTICS

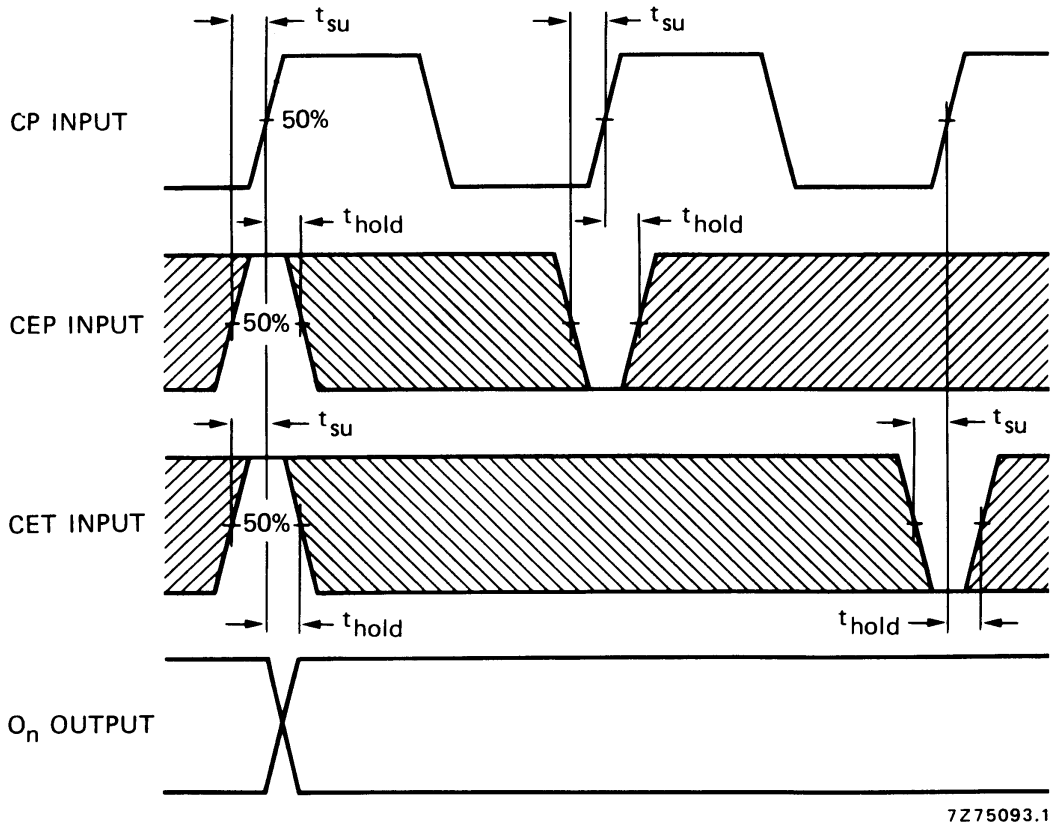
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20		ns	
	15		30	15		ns	
Set-up times $P_n \rightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \rightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET → CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
$\overline{SR} \rightarrow CP$	5	t_{su}	50	25		ns	
	10		20	10		ns	
	15		15	10		ns	
Hold times $P_n \rightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \rightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET → CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
$\overline{SR} \rightarrow CP$	5	t_{hold}	15	−10		ns	
	10		5	−5		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	



Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Fig.5 Waveforms showing set-up and hold times for $\overline{SR}$ input and minimum CP pulse width.



Condition:
$\overline{PE}$ = $\overline{SR}$ = HIGH.

Fig.6 Waveforms showing set-up times and hold times for CEP and CET inputs.

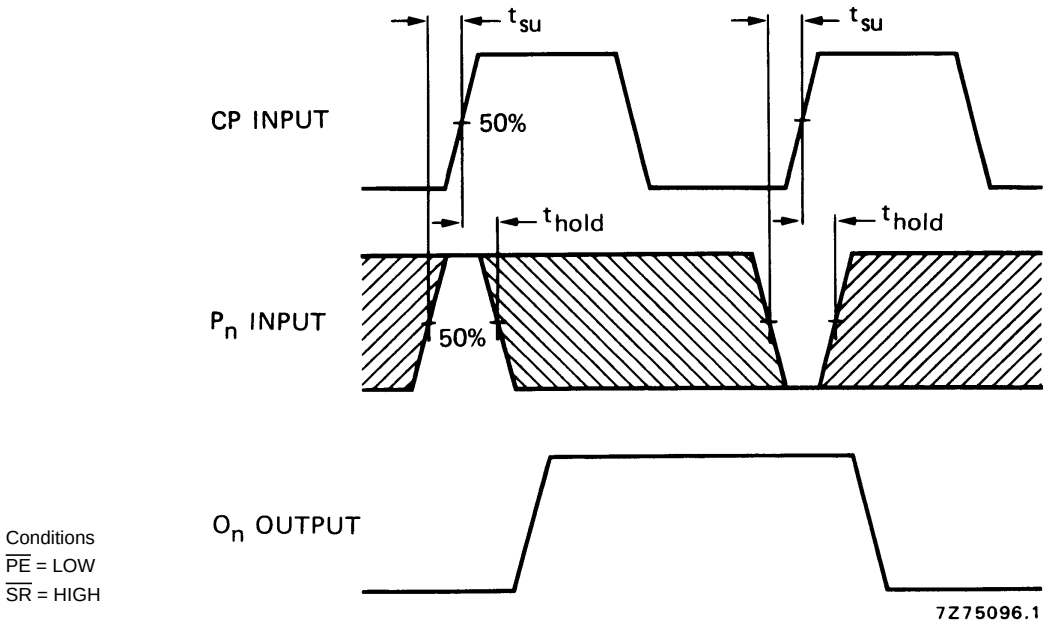


Fig.7 Waveforms showing set-up times and hold times for P_n inputs.

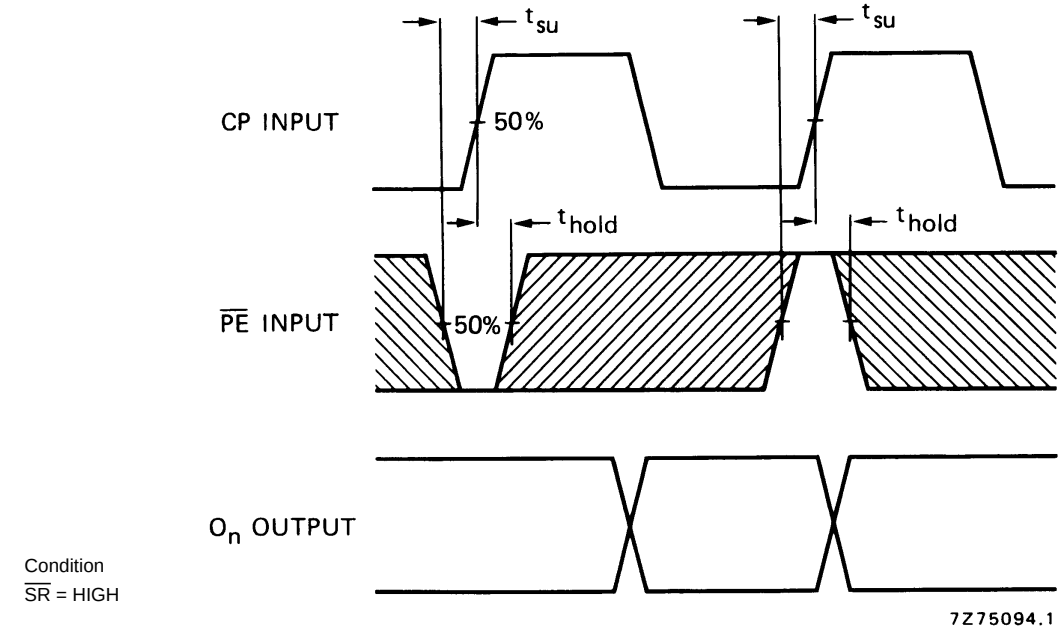


Fig.8 Waveforms showing set-up times and hold times for $\overline{PE}$ input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

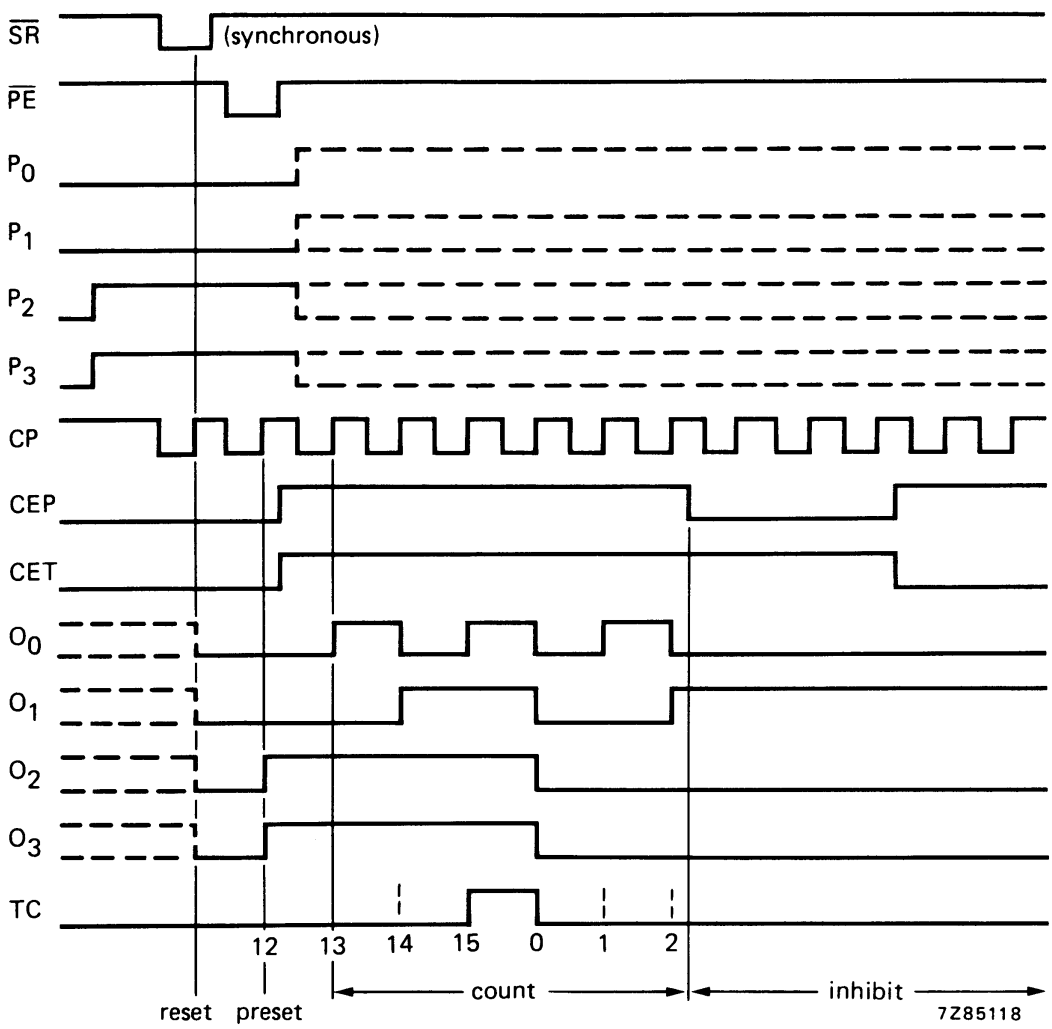
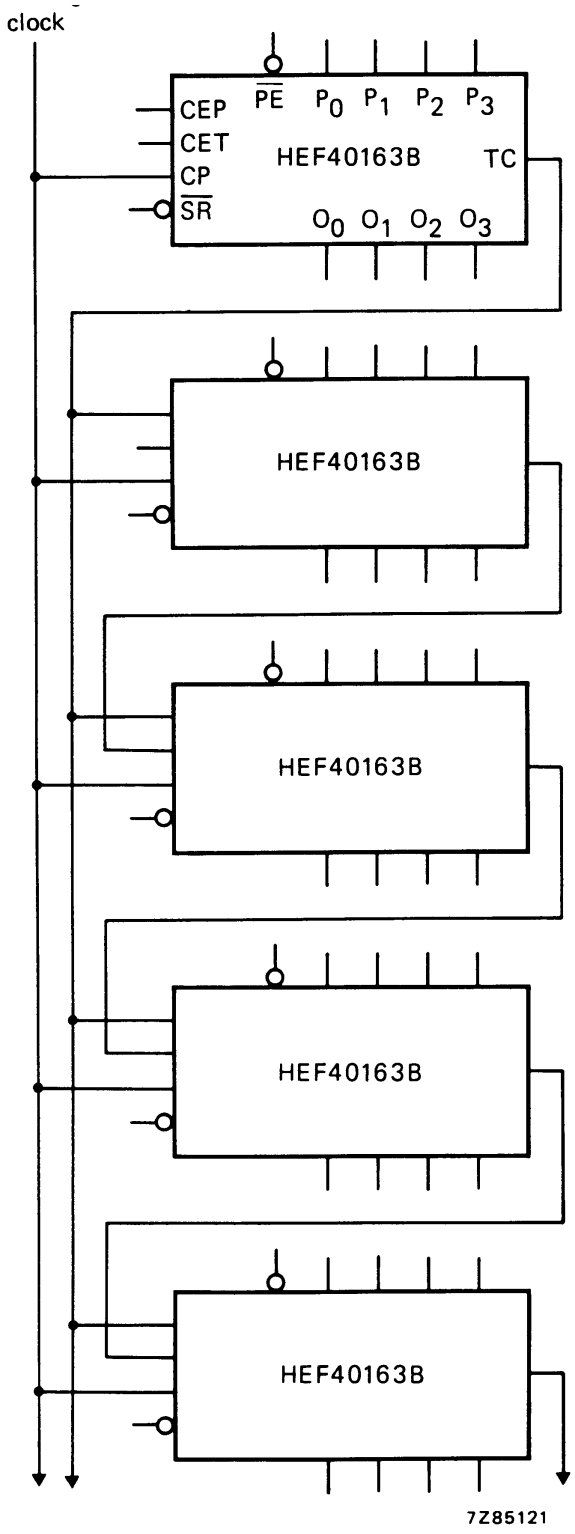


Fig.9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40163B is:

- Programmable binary counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig.10 Synchronous multi-stage counting scheme.