

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF40374B

### MSI

Octal D-type flip-flop with 3-state outputs

Product specification  
File under Integrated Circuits, IC04

January 1995

# Octal D-type flip-flop with 3-state outputs

## HEF40374B MSI

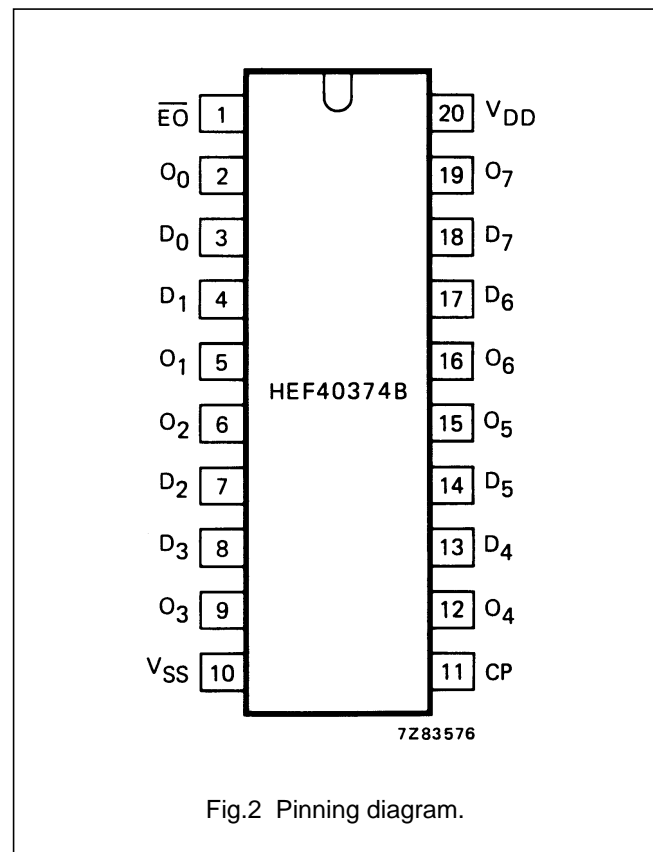
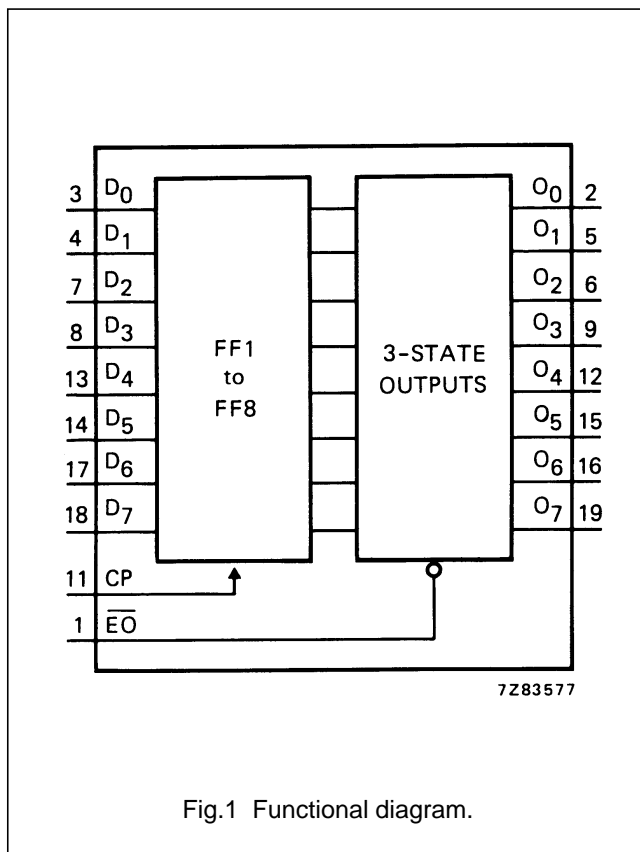
### DESCRIPTION

The HEF40374B is an octal D-type flip-flop with 3-state buffered outputs with a common clock input (CP). The device is used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus. Data on the D-inputs is transferred to storage during the LOW-to-HIGH transition of the clock (CP) input. The 3-state output buffers are controlled by an active LOW output enable input ( $\overline{EO}$ ). A HIGH on  $\overline{EO}$  forces the eight outputs to a high impedance OFF-state. When  $\overline{EO}$  is LOW, the data in the register appears at the outputs.

The output stages have high current output capability suitable for driving highly capacitive loads. The device features hysteresis on the CP input to improve noise rejection. Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40374B is pin and functionally compatible with the TTL '374' device.

Supply voltage range: 3 to 15 V.



- HEF40374BP(N): 20-lead DIL; plastic (SOT146-1)
- HEF40374BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
- HEF40374BT(D): 20-lead SO; plastic (SOT163-1)
- ( ): Package Designator North America

### PINNING

- D<sub>0</sub> to D<sub>7</sub> data inputs
- CP clock input
- $\overline{EO}$  output enable input (active LOW)
- O<sub>0</sub> to O<sub>7</sub> 3-state buffered outputs

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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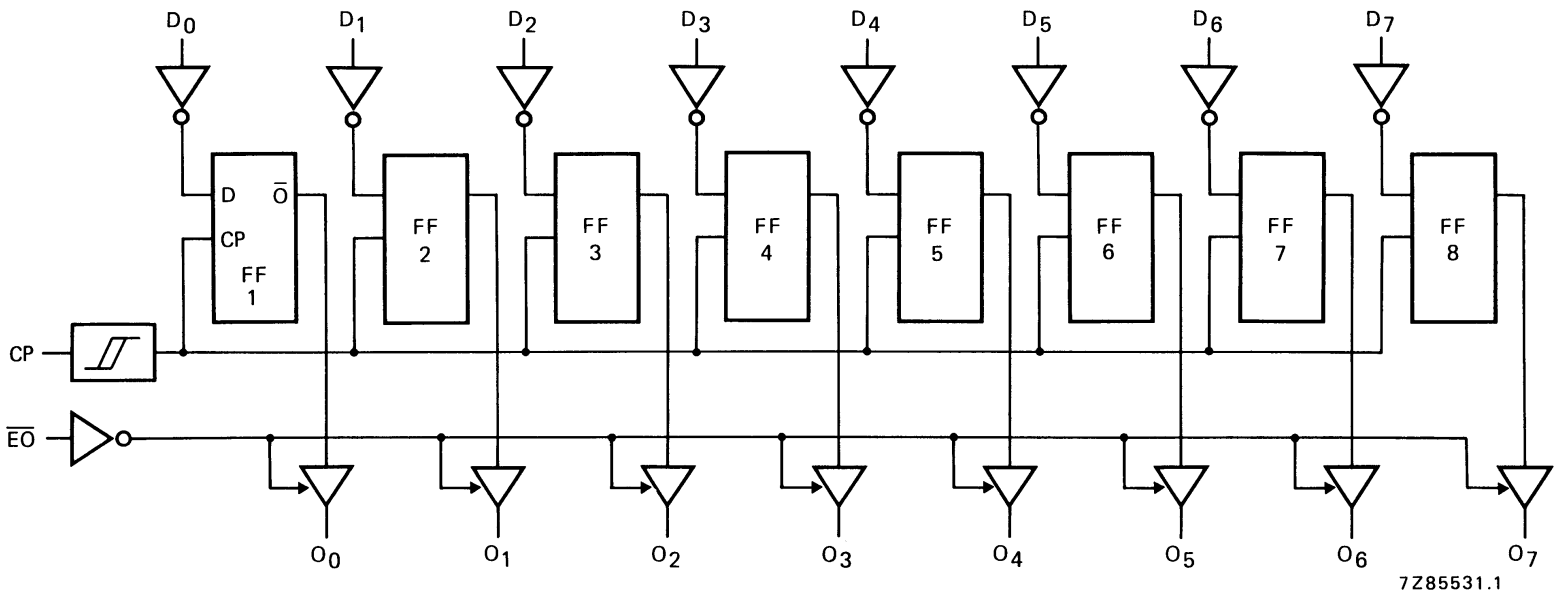






Fig.3 Logic diagram.


## Octal D-type flip-flop with 3-state outputs

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## FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS O <sub>0</sub> TO O <sub>7</sub>
	$\overline{EO}$	CP	D <sub>n</sub>		
load & read register	L		l	L	L
	L		h	H	H
load register & disable outputs	H		l	L	Z
	H		h	H	Z

## Notes

- H = HIGH state (the more positive voltage)  
 h = HIGH state (one set-up time prior to the LOW-to-HIGH clock transition)  
 L = LOW state (the less positive voltage)  
 l = LOW state (one set-up time prior to the LOW-to-HIGH clock transition)  
 Z = high impedance OFF-state  
 = LOW-to-HIGH clock transition

# Octal D-type flip-flop with 3-state outputs

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## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C. source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

## DC CHARACTERISTICS

$V_{SS} = 0 V$

	$V_{DD}$ V	$V_{OH}$ V	$V_{OL}$ V	SYMBOL	$T_{amb} (°C)$					
					-40		+25		+85	
					MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
Output current HIGH	5	4,6		$-I_{OH}$	0,75	0,6	1,2	0,45	mA	
	10	9,5			1,85	1,5	3,0	1,1	mA	
	15	13,5			14,5	15	50	15,5	mA	
Output current HIGH	5	3,6		$-I_{OH}$	9,3	10	24	10,7	mA	
	10	8,4			14,4	15	46	15,0	mA	
	15	13,2			19,5	20	62	19,8	mA	
Output current LOW	5		0,4	$I_{OL}$	2,9	2,3	5,4	1,75	mA	
	10		0,5		9,5	7,6	17	5,50	mA	
	15		1,5		30,0	25	45	19,0	mA	
Hysteresis voltage at clock input (CP)	5			$V_H$			220		mV	
	10						250		mV	
	15						320		mV	

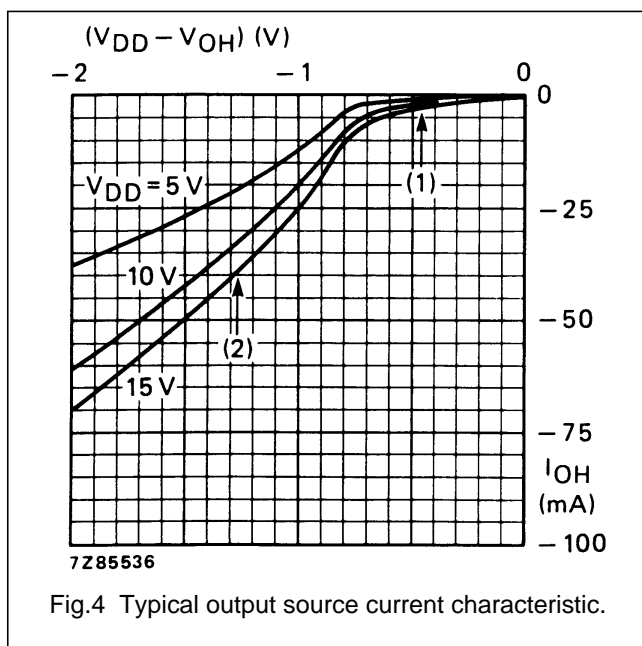
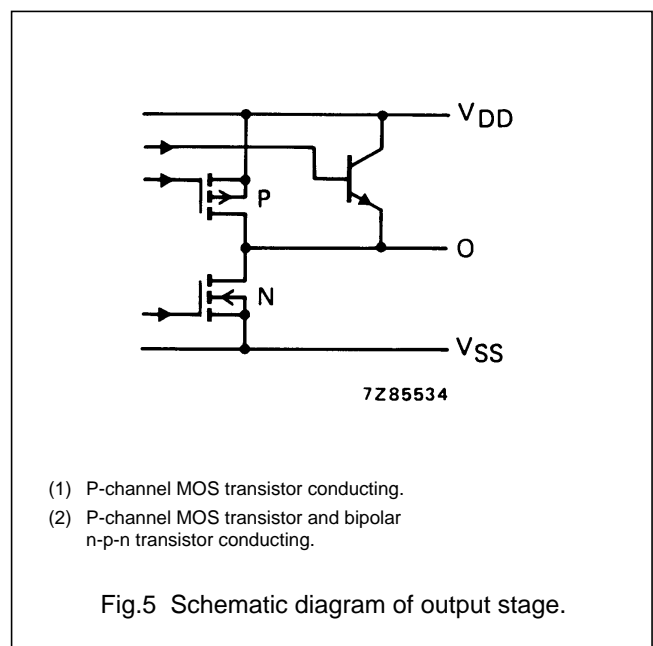


Fig.4 Typical output source current characteristic.



- (1) P-channel MOS transistor conducting.
- (2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Fig.5 Schematic diagram of output stage.

## Octal D-type flip-flop with 3-state outputs

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	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays CP $\rightarrow$ $O_n$ HIGH to LOW	5	$t_{PHL}$		125	250	ns	113 ns + (0,24 ns/pF) $C_L$ 54 ns + (0,01 ns/pF) $C_L$ 36 ns + (0,07 ns/pF) $C_L$	
	10			55	110	ns		
	15			40	80	ns		
	CP $\rightarrow$ $O_n$ LOW to HIGH	5	$t_{PLH}$		125	250	ns	122 ns + (0,06 ns/pF) $C_L$ 53 ns + (0,03 ns/pF) $C_L$ 39 ns + (0,02 ns/pF) $C_L$
		10			55	110	ns	
		15			40	80	ns	
Output transition times HIGH to LOW	5	$t_{THL}$		40	80	ns	see Fig.6	
	10			20	40	ns		
	15			15	30	ns		
	LOW to HIGH	5	$t_{TLH}$		30	60		ns
		10			20	40		ns
		15			15	30		ns
3-state propagation delays Output disable times $\overline{EO} \rightarrow O_n$ HIGH	5	$t_{PHZ}$		60	120	ns		
	10			30	60	ns		
	15			24	48	ns		
	LOW	5	$t_{PLZ}$		70	140		ns
		10			35	70		ns
		15			30	60		ns
Output enable times $\overline{EO} \rightarrow O_n$ HIGH	5	$t_{PZH}$		65	130	ns		
	10			30	60	ns		
	15			24	48	ns		
	LOW	5	$t_{PZL}$		85	170		ns
		10			35	70		ns
		15			25	50		ns
Set-up time $D_n \rightarrow CP$	5	$t_{su}$	20	0		ns		
	10		20	2		ns		
	15		20	5		ns		
Hold time $D_n \rightarrow CP$	5	$t_{hold}$	20	10		ns		
	10		15	2		ns		
	15		10	0		ns		

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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; LOW	5	t <sub>WCPL</sub>	50	25	ns	
	10		25	12	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f <sub>max</sub>	25	5	MHz	
	10		6	12	MHz	
	15		8	17	MHz	

AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; input transition times ≤ 20 ns

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	3 775 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
	10	15 700 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	
	15	40 575 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	

