HEF4049B

Hex inverting buffers

Rev. 11 — 23 June 2016

Product data sheet

1. General description

The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in Table 3.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Accepts input voltages in excess of the supply voltage
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- LOCMOS (Local Oxidation CMOS) to DTL/TTL converter
- HIGH sink current for driving two TTL loads
- HIGH-to-LOW level logic conversion

4. Ordering information

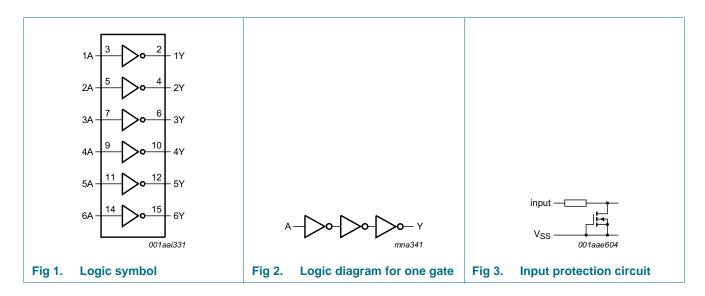
Table 1. Ordering information

All types operate from -40 °C to +85 °C.

Type number	Package							
	Name	Description	Version					
HEF4049BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1					

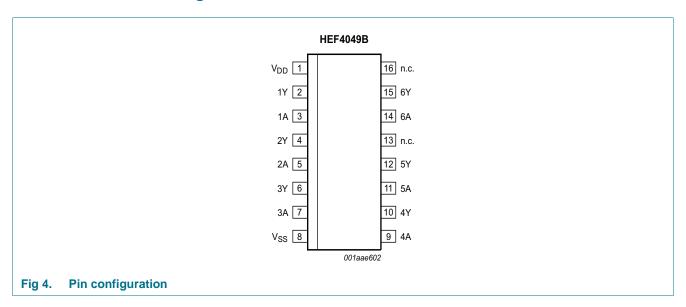


5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DD}	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output
1A to 6A	3, 5, 7, 9, 11, 14	input
V _{SS}	8	ground supply voltage
n.c.	13, 16	not connected

7. Functional description

Table 3. Guaranteed fan-out

Driven element	Guaranteed fan-out
Standard TTL	2
74 LS	9
74 L	16

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V		-10	-	mA
VI	input voltage			-0.5	+18	V
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$		-	±10	mA
I _{I/O}	input/output current			-	±10	mA
I _{DD}	supply current			-	50	mA
T _{stg}	storage temperature			-65	+150	°C
T _{amb}	ambient temperature			-40	+85	°C
P _{tot}	total power dissipation	T _{amb} –40 °C to +85 °C				
		SO16 package	[1]	-	500	mW
Р	power dissipation	per output		-	100	mW

^[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	15	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$; $V_I = V_{SS} \ or \ V_{DD} \ unless \ otherwise \ specified.$

Symbol	Parameter	Conditions V _{DD}	V_{DD}	T _{amb} =	T _{amb} = -40 °C T _{amb} =		= 25 °C T _{amb}		85 °C	Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V

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 Table 6.
 Static characteristics ...continued

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	-40 °C	T _{amb} =	25 °C	T _{amb} =	85 °C	Unit
				Min	Min Max	Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	$ I_{O} < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	$V_0 = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mΑ
		$V_0 = 4.6 \text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mΑ
		$V_0 = 9.5 \ V$	10 V	-	-1.3	-	-1.1	-	-0.9	mΑ
		$V_0 = 13.5 \text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mΑ
I _{OL}	LOW-level output current	$V_0 = 0.4 \ V$	4.75 V	3.5	-	2.9	-	2.3	-	mΑ
		$V_0 = 0.5 \ V$	10 V	12.0	-	10.0	-	8.0	-	mΑ
		$V_0 = 1.5 \text{ V}$	15 V	24.0	-	20.0	-	16.0	-	mΑ
l _l	input leakage current	V _{DD} = 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	μΑ
I _{DD}	supply current	I _O = 0 A	5 V	-	4.0	-	4.0	-	30	μΑ
			10 V	-	8.0	-	8.0	-	60	μΑ
			15 V	-	16.0	-	16.0	-	120	μΑ
Cı	input capacitance			-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

 $V_{SS} = 0$ V; $C_L = 50$ pF; $t_r = t_f \le 20$ ns; $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	nA to nY;	5 V [1]	26 ns + (0.18 ns/pF)C _L	-	35	70	ns
	propagation delay	see Figure 5	10 V	11 ns + (0.08 ns/pF)C _L	-	15	30	ns
			15 V	9 ns + (0.05 ns/pF)C _L	-	12	25	ns
t _{PLH}	LOW to HIGH	nA to nY;	5 V [1]	23 ns + (0.55 ns/pF)C _L	-	50	100	ns
	propagation delay	see Figure 5	10 V	14 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C _L	-	20	40	ns
t _{THL}	HIGH to LOW output	see Figure 5	5 V [1]	3 ns + (0.35 ns/pF)C _L	-	20	40	ns
	transition time		10 V	3 ns + (0.14 ns/pF)C _L	-	10	20	ns
			15 V	2 ns + (0.09 ns/pF)C _L	-	7	14	ns
t _{TLH}	LOW to HIGH output	see Figure 5	5 V [1]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

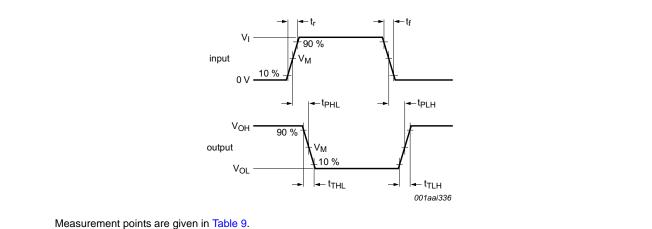
^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_{D}

 P_D can be calculated from the formulas shown. $V_{SS} = 0 \ V$; $t_r = t_f \le 20 \ ns$; $T_{amb} = 25 \ ^{\circ}C$.

Symbol	Parameter	V_{DD}	Typical formula for P _D (μW)	where:
P_D	dynamic power	5 V	$P_D = 2500 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz;
	dissipation	10 V	$P_D = 11000 \times f_i + \Sigma (f_0 \times C_L) \times V_{DD}^2$	fo = output frequency in MHz;
		15 V	$P_{D} = 35000 \times f_{i} + \Sigma (f_{o} \times C_{L}) \times V_{DD}^{2}$	C _L = output load capacitance in pF;
				V _{DD} = supply voltage in V;
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

12. Waveforms

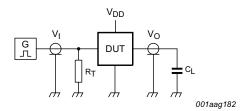


 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Input (nA) to output (nY) propagation delays and transition times Fig 5.

Table 9. **Measurement points**

Input		Output				
V _M	VI	V _M	V _X	V _Y		
0.5V _{DD}	0 V to V _{DD}	0.5V _{DD}	0.1V _{DD}	0.9V _{DD}		



Test data is given in Table 10.

Definitions for test circuit:

 C_L = Load capacitance including jig and probe capacitance.

 R_{T} = Termination resistance should be equal to output impedance Z_{0} of the pulse generator.

Fig 6. Test circuit for measuring switching times

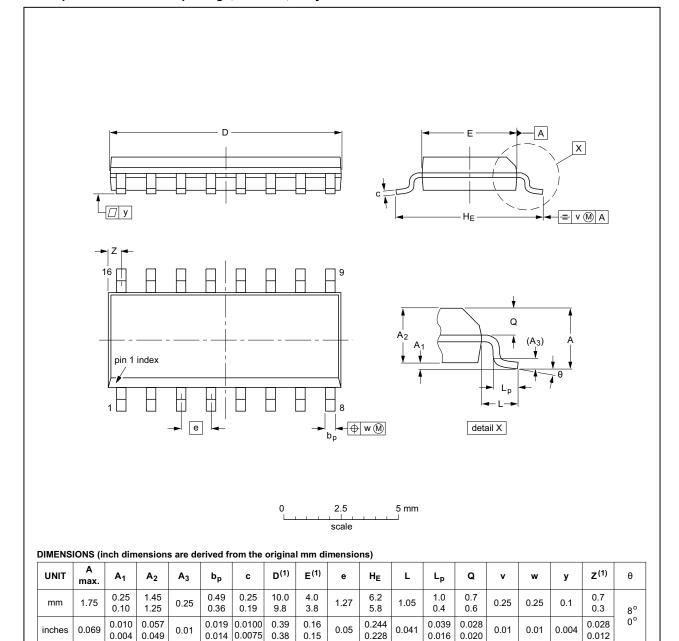
Table 10. Test data

Supply voltage	Supply voltage Input I					
V_{DD}	VI	V _M	t _r , t _f	C _L		
5 V to 15 V	V_{DD}	0.5V _I	≤ 20 ns	50 pF		

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	JEITA PROJECTION		ISSUE DATE
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 7. Package outline SOT109-1 (SO16)

HEF4049B

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DTL	Diode Transistor Logic
DUT	Device Under Test
LOCMOS	Local Oxidation CMOS
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4049B v.11	20160623	Product data sheet	-	HEF4049B v.10
Modifications:	Table 4: condition for input clamping current changed (typo corrected).			
	• Table 5: max	imum value for input voltage ch	nanged (typo correct	ed).
HEF4049B v.10	20160324	Product data sheet	-	HEF4049B v.9
Modifications:	Type number	HEF4049BP (SOT38-4) remo	ved.	
HEF4049B v.9	20111118	Product data sheet	-	HEF4049B v.8
Modifications:	Table 6: I _{OH} minimum values changed to maximum			
	• <u>Table 11</u> : Add	ded DUT		
HEF4049B v.8	20091202	Product data sheet	-	HEF4049B v.7
HEF4049B v.7	20090721	Product data sheet	-	HEF4049B v.6
HEF4049B v.6	20090325	Product data sheet	-	HEF4049B v.5
HEF4049B v.5	20081111	Product data sheet	-	HEF4049B v.4
HEF4049B v.4	20080704	Product data sheet	-	HEF4049B_CNV v.3
HEF4049B_CNV v.3	19950101	Product specification	-	HEF4049B_CNV v.2
HEF4049B_CNV v.2	19950101	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

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