

HEF4053B

Triple single-pole double-throw analog switch

Rev. 12 — 25 March 2016

Product data sheet

1. General description

The HEF4053B is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (S_n), two independent inputs/outputs (nY_0 and nY_1) and a common input/output (nZ). All three switches share an enable input (\bar{E}). A HIGH on \bar{E} causes all switches into the high-impedance OFF-state, independent of S_n .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_n and \bar{E}). The V_{DD} to V_{SS} range is 3 V to 15 V. The analog inputs/outputs (nY_0 , nY_1 and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| HEF4053BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| HEF4053BTT | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

5. Functional diagram

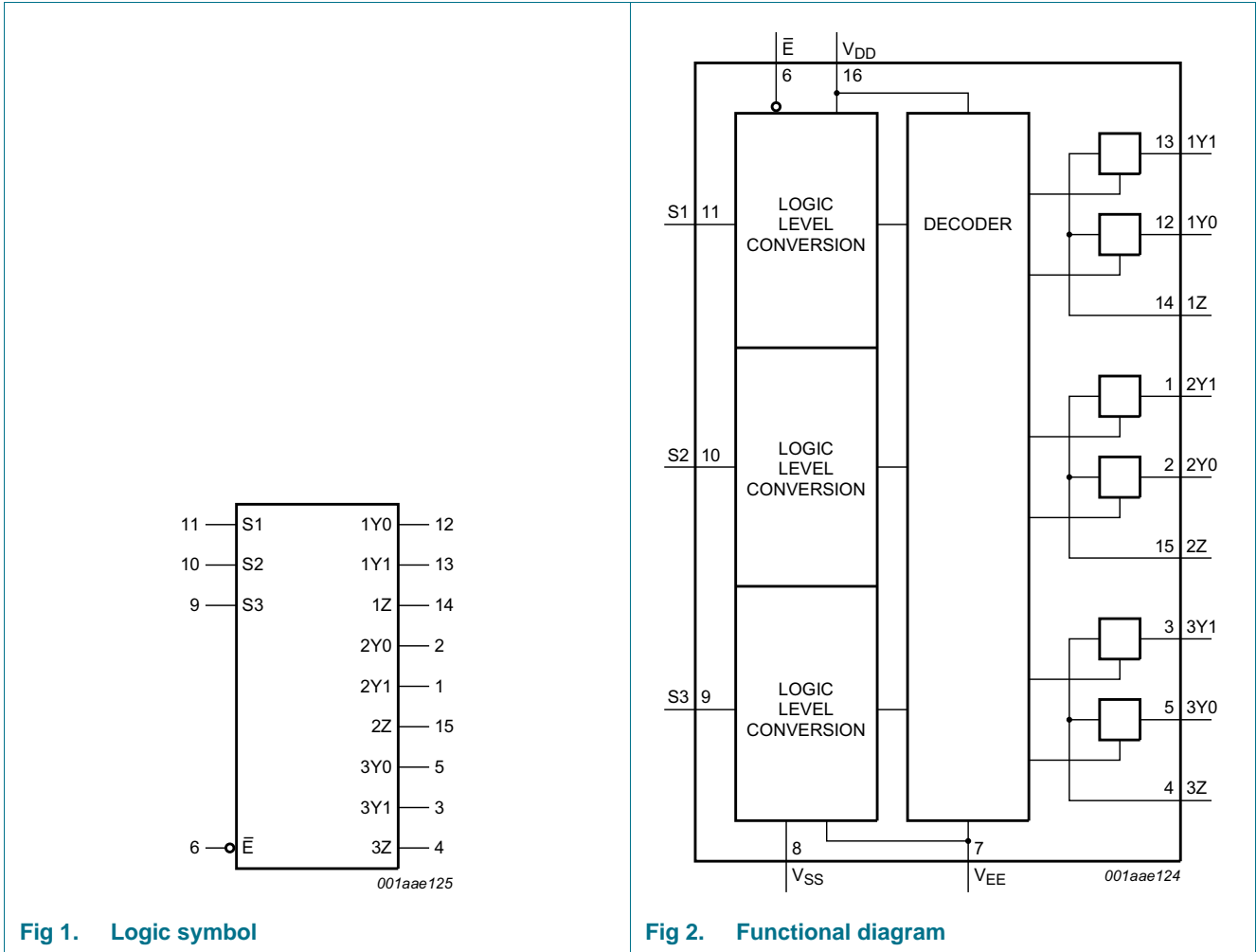


Fig 1. Logic symbol

Fig 2. Functional diagram

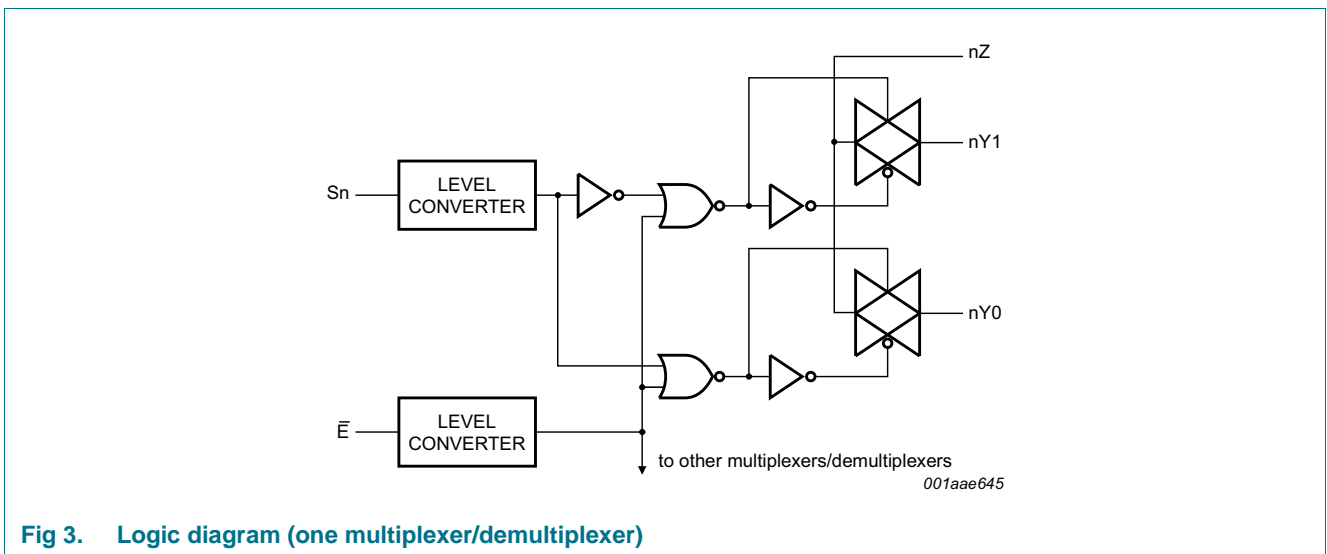


Fig 3. Logic diagram (one multiplexer/demultiplexer)

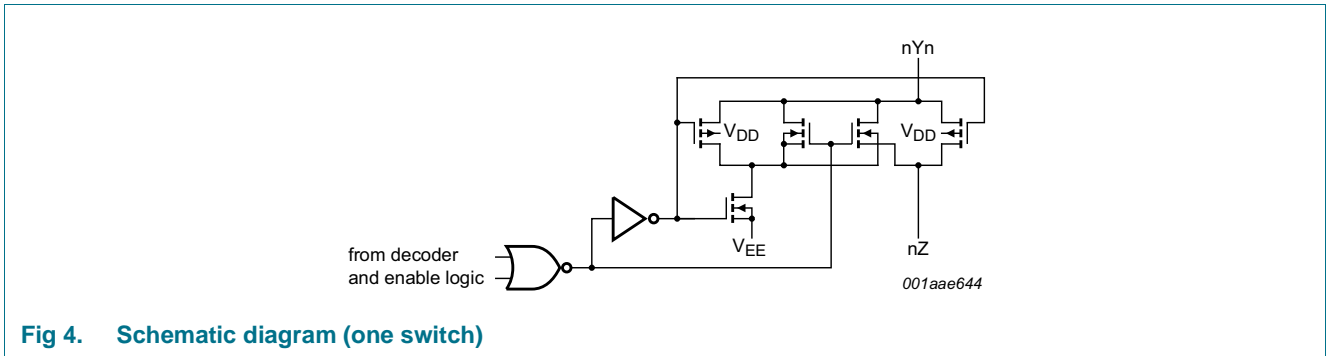


Fig 4. Schematic diagram (one switch)

6. Pinning information

6.1 Pinning

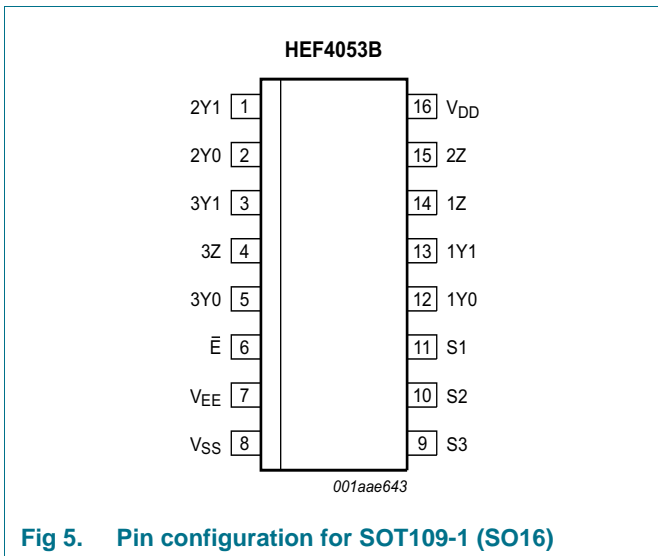


Fig 5. Pin configuration for SOT109-1 (SO16)

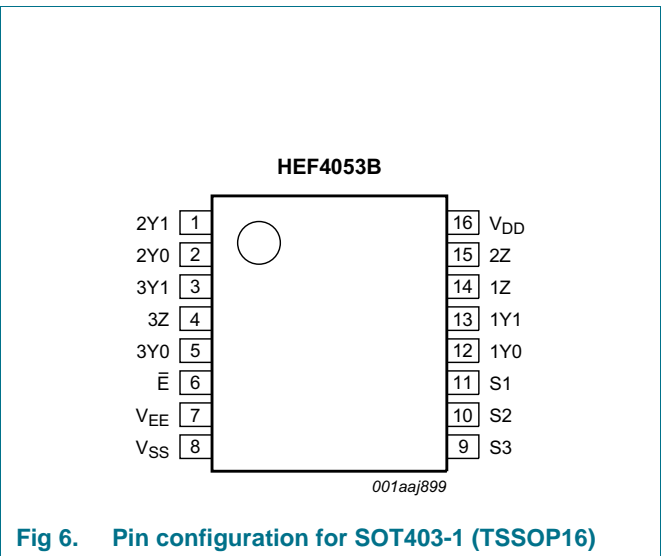


Fig 6. Pin configuration for SOT403-1 (TSSOP16)

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---------------|-----------|-----------------------------|
| \bar{E} | 6 | enable input (active LOW) |
| V_{EE} | 7 | supply voltage |
| V_{SS} | 8 | ground supply voltage |
| S1, S2, S3 | 11, 10, 9 | select input |
| 1Y0, 2Y0, 3Y0 | 12, 2, 5 | independent input or output |
| 1Y1, 2Y1, 3Y1 | 13, 1, 3 | independent input or output |
| 1Z, 2Z, 3Z | 14, 15, 4 | independent output or input |
| V_{DD} | 16 | supply voltage |

7. Functional description

Table 3. Function table [1]

| Inputs | | Channel on |
|-----------|----|--------------|
| \bar{E} | Sn | |
| L | L | nY0 to nZ |
| L | H | nY1 to nZ |
| H | X | switches OFF |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|------|----------------|------|
| V_{DD} | supply voltage | | -0.5 | +18 | V |
| V_{EE} | supply voltage | referenced to V_{DD} [1] | -18 | +0.5 | V |
| I_{IK} | input clamping current | pins Sn and \bar{E} ; $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | - | ± 10 | mA |
| V_I | input voltage | | -0.5 | $V_{DD} + 0.5$ | V |
| $I_{I/O}$ | input/output current | | - | ± 10 | mA |
| I_{DD} | supply current | | - | 50 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | | | |
| | | SO16 package [2] | - | 500 | mW |
| | | TSSOP16 package [2] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, and in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE} .

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------------------------|-----|-----|----------|-----------------|
| V_{DD} | supply voltage | see Figure 7 | 3 | - | 15 | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5$ V | - | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10$ V | - | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15$ V | - | - | 0.08 | $\mu\text{s/V}$ |

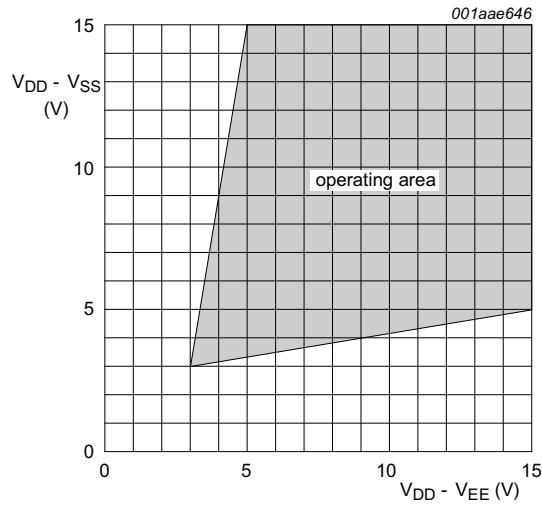


Fig 7. Operating area as a function of the supply voltages

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = V_{EE} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ }^{\circ}\text{C}$ | | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | | $T_{amb} = 85\text{ }^{\circ}\text{C}$ | | $T_{amb} = 125\text{ }^{\circ}\text{C}$ | | Unit |
|--------------|---------------------------|--|----------|---|-----------|--|-----------|--|-----------|---|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| I_I | input leakage current | | 15 V | - | ± 0.1 | - | ± 0.1 | - | ± 1.0 | - | ± 1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | Z port; all channels OFF; see Figure 8 | 15 V | - | - | - | 1000 | - | - | - | - | nA |
| | | Y port; per channel; see Figure 9 | 15 V | - | - | - | 200 | - | - | - | - | nA |
| I_{DD} | supply current | $I_O = 0\text{ A}$ | 5 V | - | 5 | - | 5 | - | 150 | - | 150 | μA |
| | | | 10 V | - | 10 | - | 10 | - | 300 | - | 300 | μA |
| | | | 15 V | - | 20 | - | 20 | - | 600 | - | 600 | μA |
| C_I | input capacitance | S_n, \bar{E} inputs | - | - | - | - | 7.5 | - | - | - | - | pF |

10.1 Test circuits

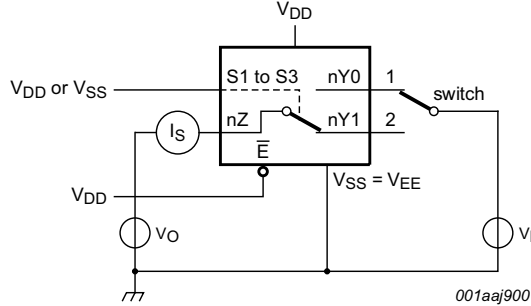


Fig 8. Test circuit for measuring OFF-state leakage current Z port

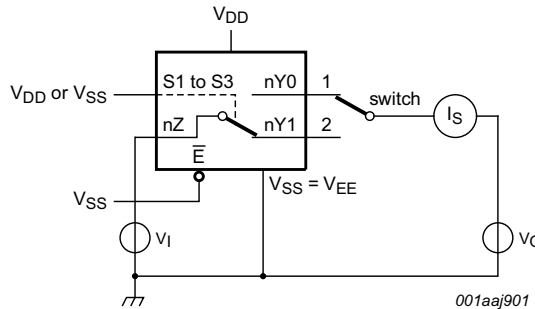


Fig 9. Test circuit for measuring OFF-state leakage current nYn port

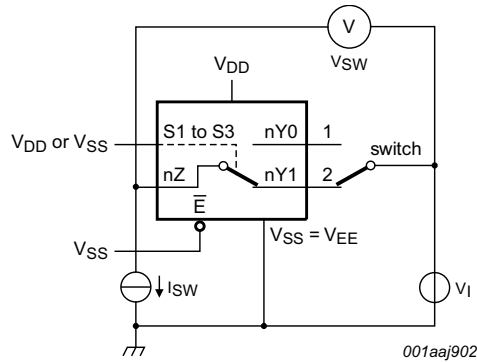
10.2 ON resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $I_{SW} = 200\text{ }\mu\text{A}$; $V_{SS} = V_{EE} = 0\text{ V}$.

| Symbol | Parameter | Conditions | $V_{DD} - V_{EE}$ | Typ | Max | Unit |
|-----------------|---|--|-------------------|-----|------|----------|
| $R_{ON(peak)}$ | ON resistance (peak) | $V_I = 0\text{ V to }V_{DD} - V_{EE}$; see Figure 10 and Figure 11 | 5 V | 350 | 2500 | Ω |
| | | | 10 V | 80 | 245 | Ω |
| | | | 15 V | 60 | 175 | Ω |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_I = 0\text{ V}$; see Figure 10 and Figure 11 | 5 V | 115 | 340 | Ω |
| | | | 10 V | 50 | 160 | Ω |
| | | | 15 V | 40 | 115 | Ω |
| | | $V_I = V_{DD} - V_{EE}$; see Figure 10 and Figure 11 | 5 V | 120 | 365 | Ω |
| | | | 10 V | 65 | 200 | Ω |
| | | | 15 V | 50 | 155 | Ω |
| ΔR_{ON} | ON resistance mismatch between channels | $V_I = 0\text{ V to }V_{DD} - V_{EE}$; see Figure 10 | 5 V | 25 | - | Ω |
| | | | 10 V | 10 | - | Ω |
| | | | 15 V | 5 | - | Ω |

10.2.1 ON resistance waveform and test circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Fig 10. Test circuit for measuring R_{ON}

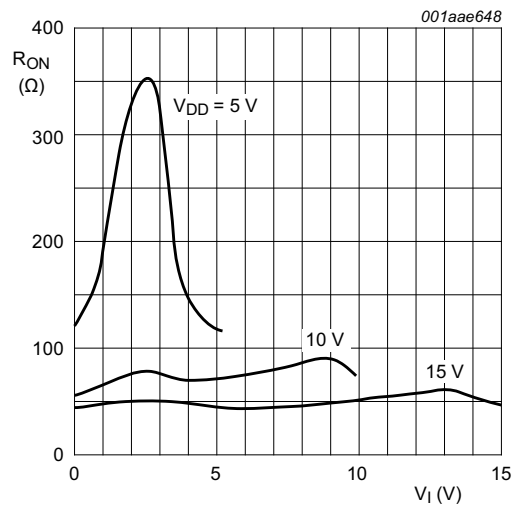


Fig 11. Typical R_{ON} as a function of input voltage

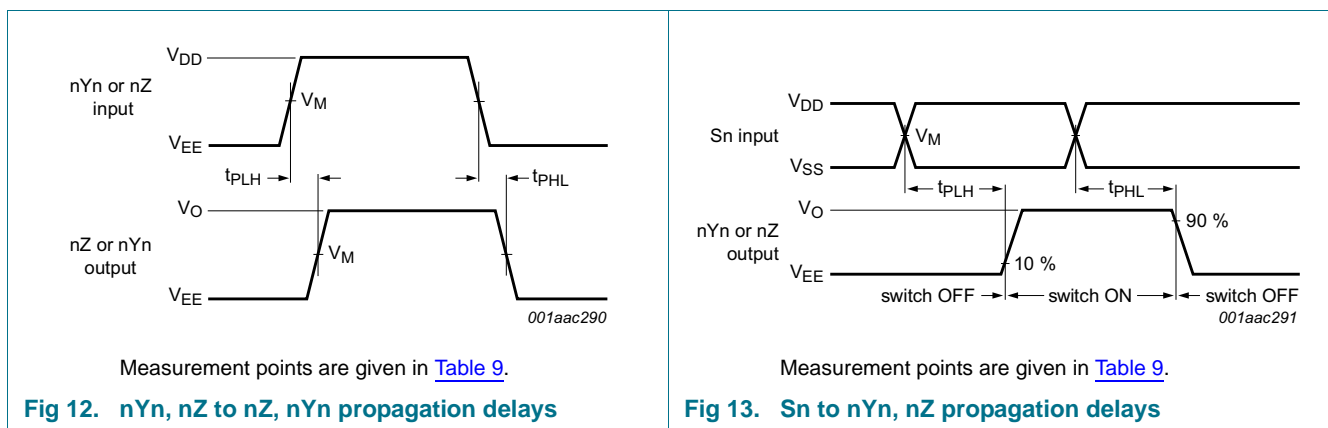
11. Dynamic characteristics

Table 8. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = V_{EE} = 0\text{ V}$; for test circuit see [Figure 15](#).

| Symbol | Parameter | Conditions | V_{DD} | Typ | Max | Unit |
|-----------|-------------------------------------|---|----------|-----|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | nYn, nZ to nZ, nYn; see Figure 12 | 5 V | 10 | 20 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 13 | 5 V | 200 | 400 | ns |
| | | | 10 V | 85 | 170 | ns |
| | | | 15 V | 65 | 130 | ns |
| t_{PLH} | LOW to HIGH propagation delay | nYn, nZ to nZ, nYn; see Figure 12 | 5 V | 15 | 30 | ns |
| | | | 10 V | 5 | 10 | ns |
| | | | 15 V | 5 | 10 | ns |
| | | Sn to nYn, nZ; see Figure 13 | 5 V | 275 | 555 | ns |
| | | | 10 V | 100 | 200 | ns |
| | | | 15 V | 65 | 130 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | \bar{E} to nYn, nZ; see Figure 14 | 5 V | 200 | 400 | ns |
| | | | 10 V | 115 | 230 | ns |
| | | | 15 V | 110 | 220 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | \bar{E} to nYn, nZ; see Figure 14 | 5 V | 260 | 525 | ns |
| | | | 10 V | 95 | 190 | ns |
| | | | 15 V | 65 | 130 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | \bar{E} to nYn, nZ; see Figure 14 | 5 V | 200 | 400 | ns |
| | | | 10 V | 120 | 245 | ns |
| | | | 15 V | 110 | 215 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | \bar{E} to nYn, nZ; see Figure 14 | 5 V | 280 | 565 | ns |
| | | | 10 V | 105 | 205 | ns |
| | | | 15 V | 70 | 140 | ns |

11.1 Waveforms and test circuit



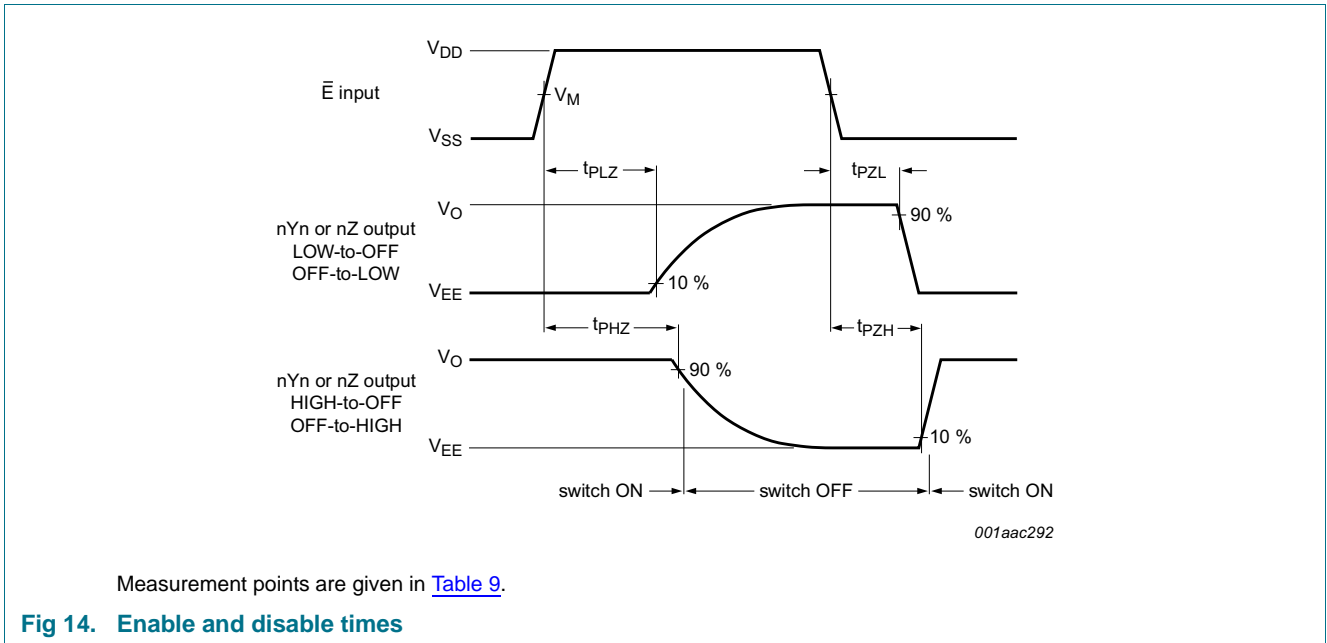
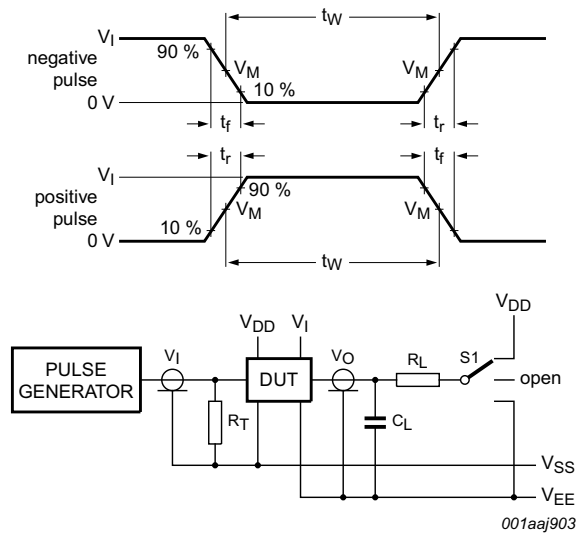


Table 9. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{DD} | V_M | V_M |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |



Test data is given in [Table 10](#).

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 15. Test circuit for measuring switching times

Table 10. Test data

| Input | | | | Load | | S1 position | | | | |
|----------------------|----------------------|--------------|-------------|-------|---------------|----------------------|-----------|--------------------|--------------------|----------|
| nYn, nZ | Sn and \bar{E} | t_r, t_f | V_M | C_L | R_L | t_{PHL} [1] | t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} | other |
| V_{DD} or V_{EE} | V_{DD} or V_{SS} | ≤ 20 ns | $0.5V_{DD}$ | 50 pF | 10 k Ω | V_{DD} or V_{EE} | V_{EE} | V_{EE} | V_{DD} | V_{EE} |

[1] For nYn to nZ or nZ to nYn propagation delays use V_{EE} . For Sn to nYn or nZ propagation delays use V_{DD} .

11.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

$V_{SS} = V_{EE} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | V_{DD} | Typ | Max | Unit | |
|----------------|---------------------------|---|----------|-----|------|------|-----|
| THD | total harmonic distortion | see Figure 16; $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1\text{ kHz}$ | 5 V | [1] | 0.25 | - | % |
| | | | 10 V | [1] | 0.04 | - | % |
| | | | 15 V | [1] | 0.04 | - | % |
| $f_{(-3dB)}$ | -3 dB frequency response | see Figure 17; $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_I = 0.5V_{DD}$ (p-p) | 5 V | [1] | 13 | - | MHz |
| | | | 10 V | [1] | 40 | - | MHz |
| | | | 15 V | [1] | 70 | - | MHz |
| α_{iso} | isolation (OFF-state) | see Figure 18; $f_i = 1\text{ MHz}$; $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_I = 0.5V_{DD}$ (p-p) | 10 V | [1] | -50 | - | dB |
| V_{ct} | crosstalk voltage | digital inputs to switch; see Figure 19; $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; E or $S_n = V_{DD}$ (square-wave) | 10 V | | 50 | - | mV |
| Xtalk | crosstalk | between switches; see Figure 20; $f_i = 1\text{ MHz}$; $R_L = 1\text{ k}\Omega$; $V_I = 0.5V_{DD}$ (p-p) | 10 V | [1] | -50 | - | dB |

[1] f_i is biased at $0.5 V_{DD}$; $V_I = 0.5V_{DD}$ (p-p).

Table 12. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown; $V_{EE} = V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | V_{DD} | Typical formula for P_D (μW) | where: |
|--------|---------------------------|----------|---|--|
| P_D | dynamic power dissipation | 5 V | $P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs. |
| | | 10 V | $P_D = 11500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 29000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

11.2.1 Test circuits

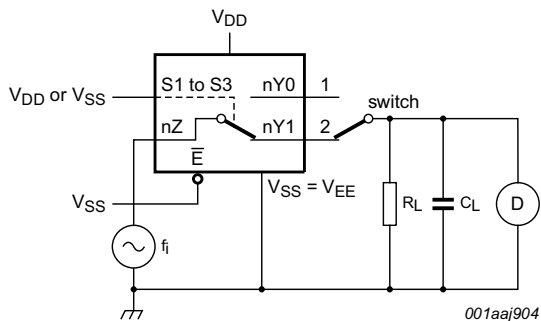


Fig 16. Test circuit for measuring total harmonic distortion

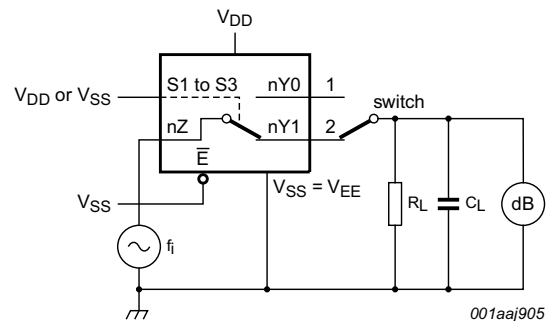


Fig 17. Test circuit for measuring frequency response

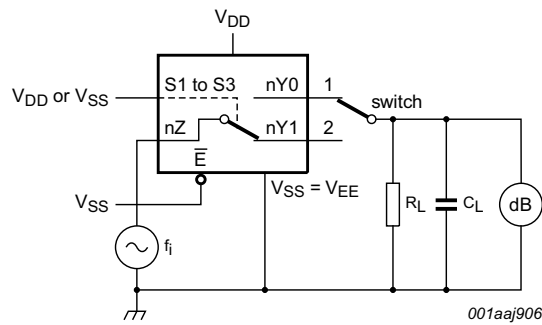
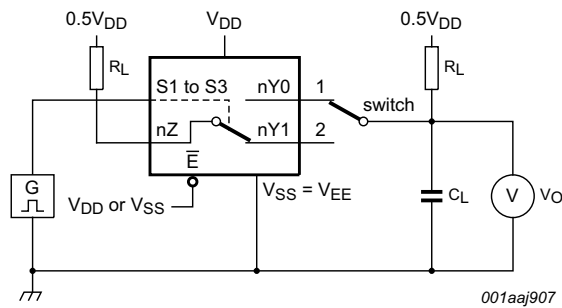
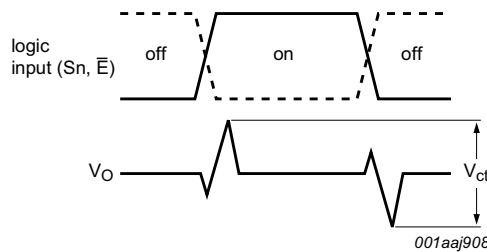


Fig 18. Test circuit for measuring isolation (OFF-state)

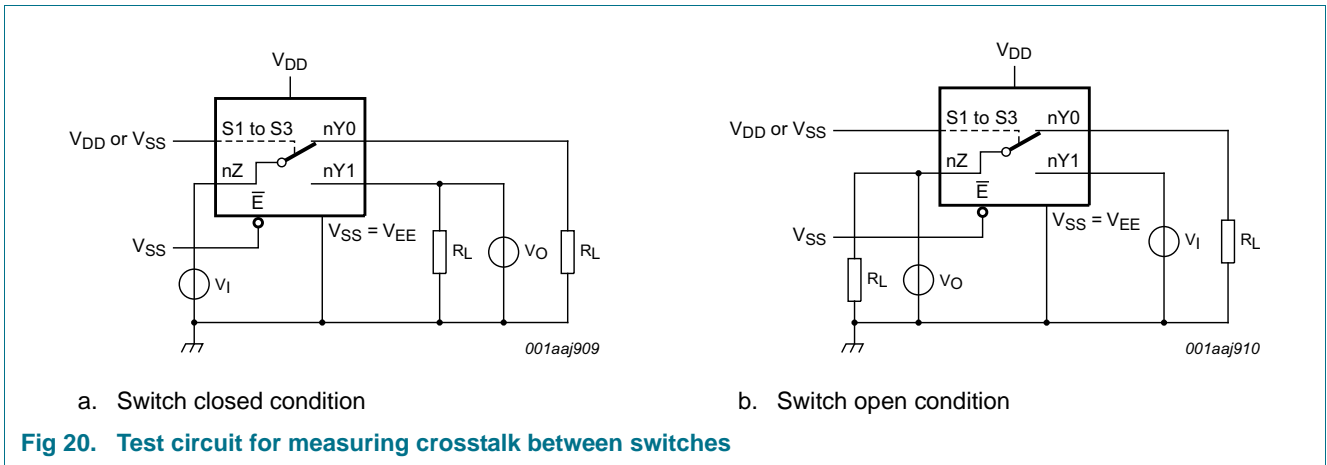


a. Test circuit



b. Input and output pulse definitions

Fig 19. Test circuit for measuring crosstalk voltage between digital inputs and switch



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

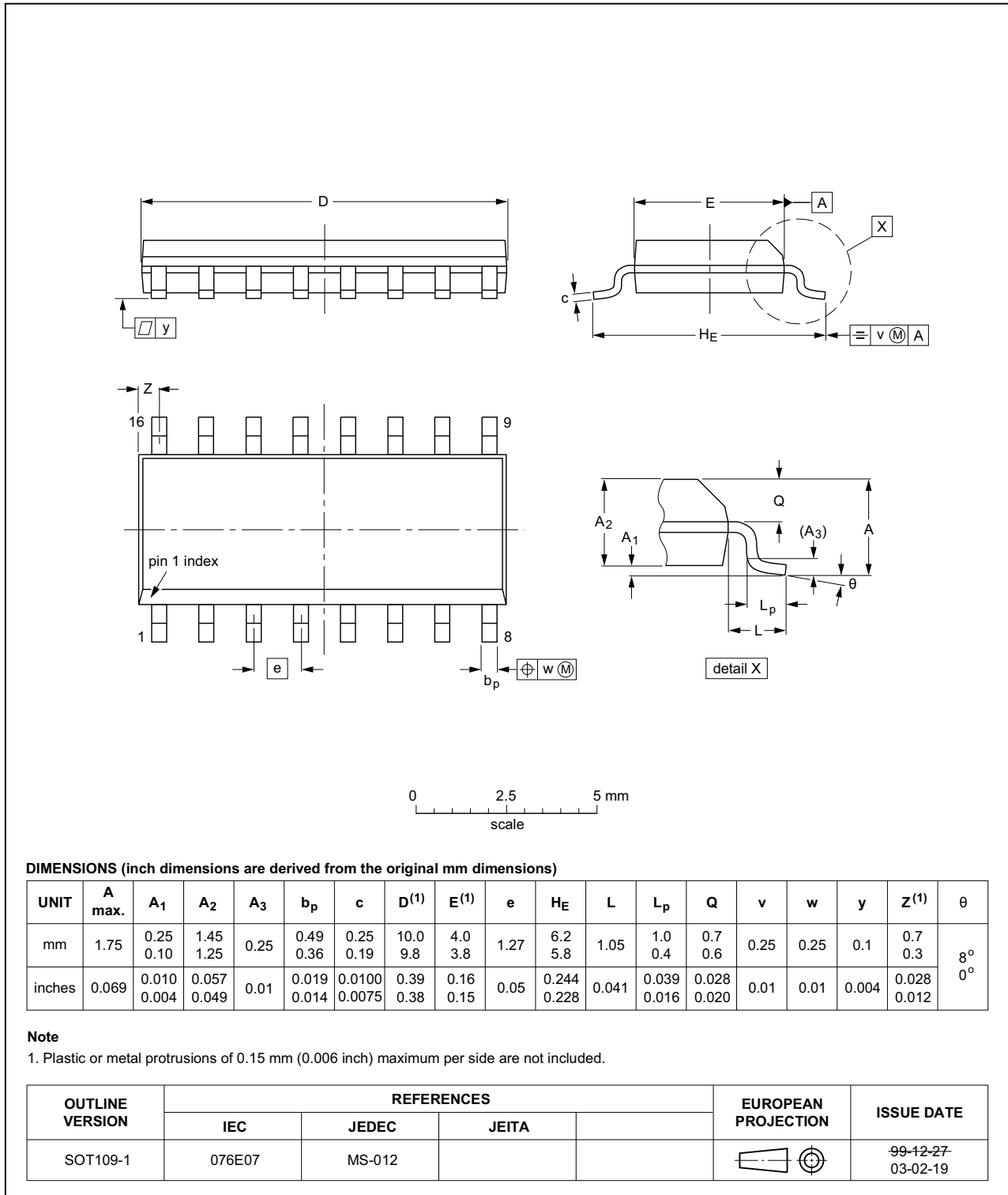


Fig 21. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

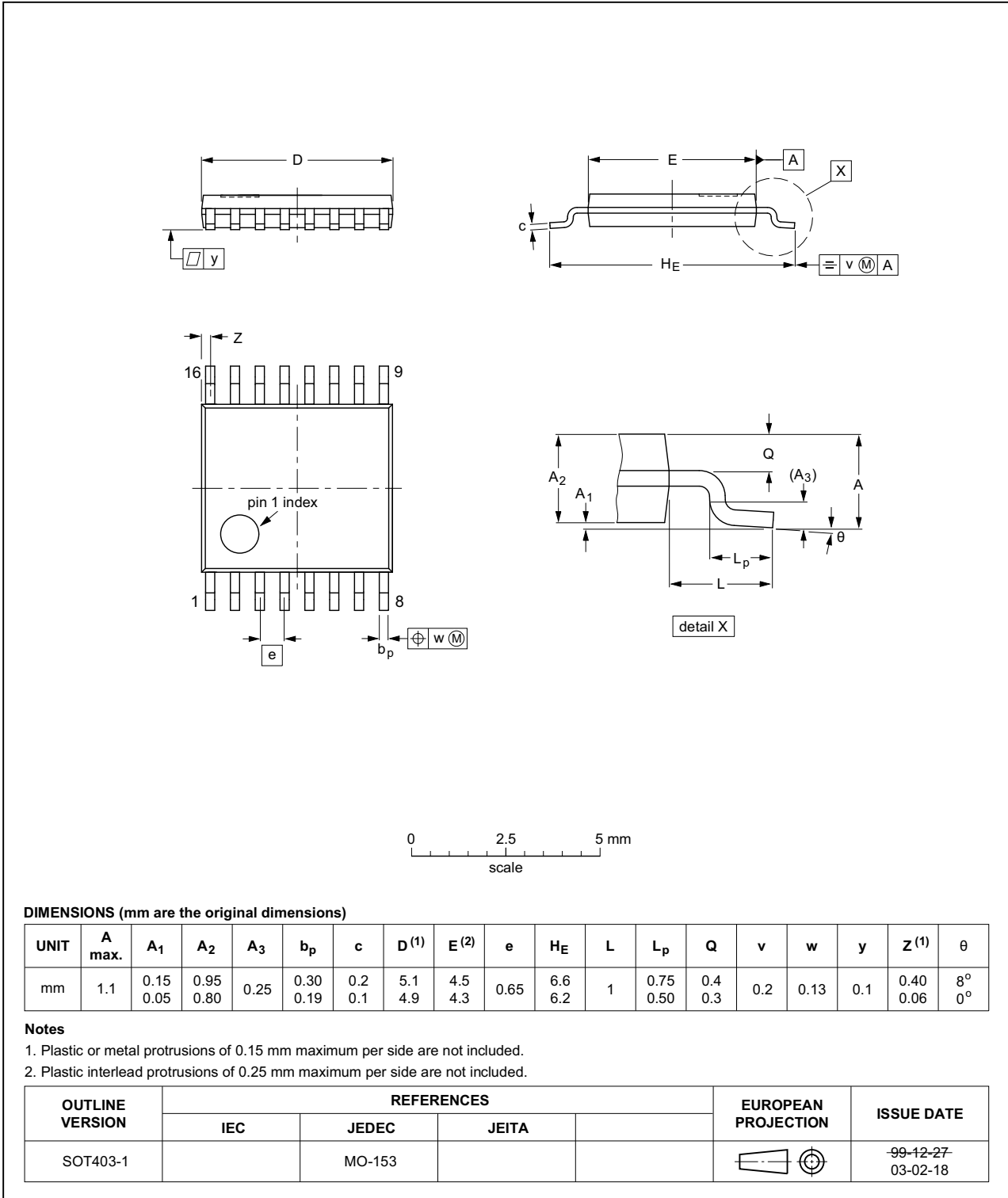


Fig 22. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 13. Abbreviations

| Acronym | Description |
|---------|-------------------|
| DUT | Device Under Test |

14. Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|-----------------------|---------------|------------------|
| HEF4053B v.12 | 20160325 | Product data sheet | - | HEF4053B v.11 |
| Modifications: | <ul style="list-style-type: none"> Type number HEF4053BP (SOT38-4) removed. | | | |
| HEF4053B v.11 | 20140911 | Product data sheet | - | HEF4053B v.10 |
| Modifications: | <ul style="list-style-type: none"> Figure 19: Test circuit modified | | | |
| HEF4053B v.10 | 20111117 | Product data sheet | - | HEF4053B v.9 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. Changes in “General description”, “Features and benefits” and “Applications”. | | | |
| HEF4053B v.9 | 20100325 | Product data sheet | - | HEF4053B v.8 |
| HEF4053B v.8 | 20100224 | Product data sheet | - | HEF4053B v.7 |
| HEF4053B v.7 | 20091127 | Product data sheet | - | HEF4053B v.6 |
| HEF4053B v.6 | 20090924 | Product data sheet | - | HEF4053B v.5 |
| HEF4053B v.5 | 20090825 | Product data sheet | - | HEF4053B v.4 |
| HEF4053B v.4 | 20090713 | Product data sheet | - | HEF4053B_CNV v.3 |
| HEF4053B_CNV v.3 | 19950101 | Product specification | - | HEF4053B_CNV v.2 |
| HEF4053B_CNV v.2 | 19950101 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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