

HEF4069UB

Hex unbuffered inverter

Rev. 11 — 5 September 2024

Product data sheet

1. General description

The HEF4069UB is a hex unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Oscillator

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4069UBT	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4069UBTT	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

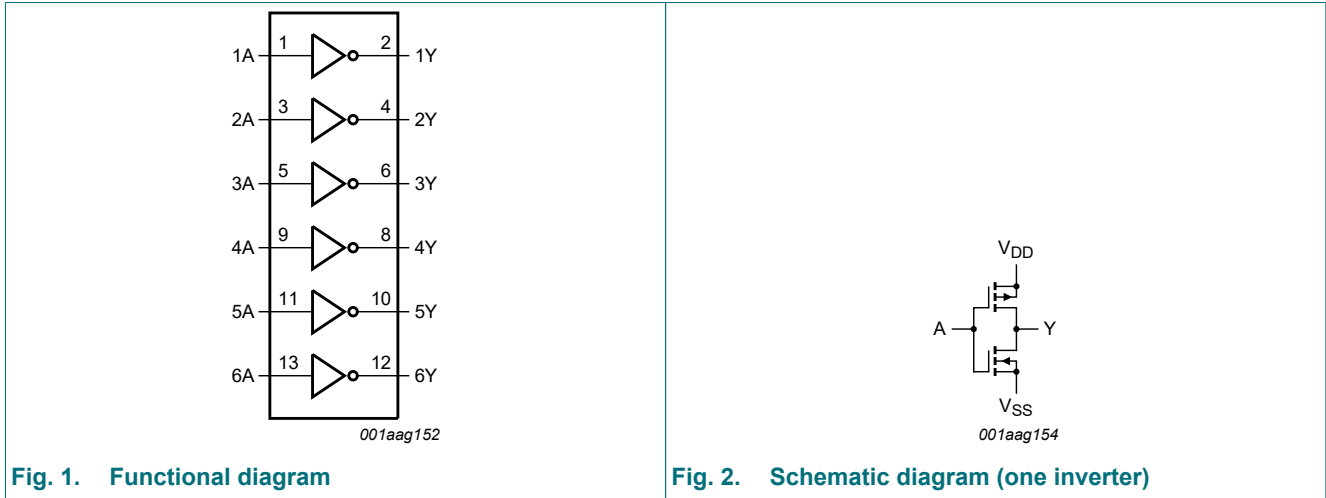


Fig. 1. Functional diagram

Fig. 2. Schematic diagram (one inverter)

6. Pinning information

6.1. Pinning

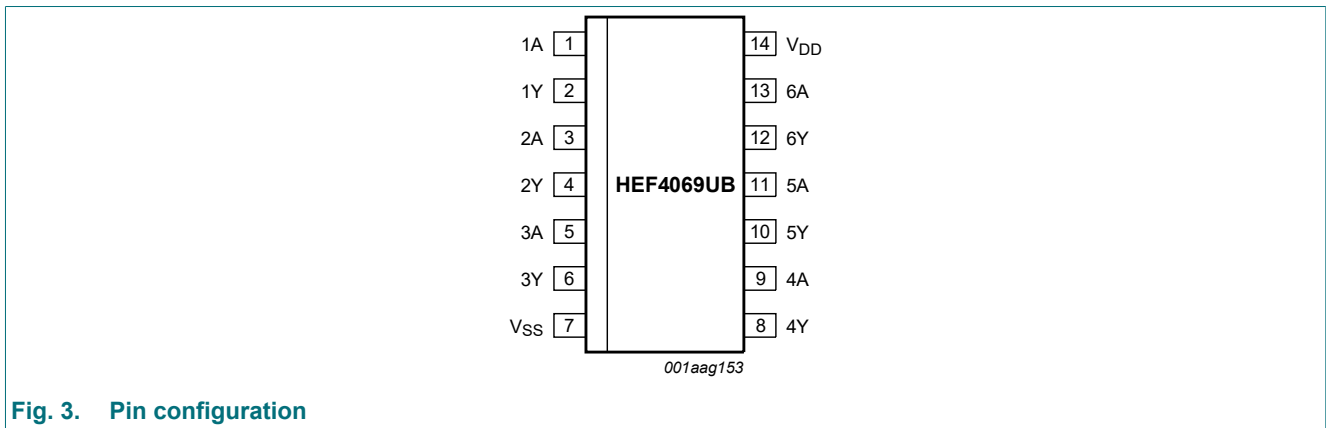


Fig. 3. Pin configuration

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C

9. Static characteristics

Table 5. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4	-	4	-	4	-	4	-	V
			10 V	8	-	8	-	8	-	8	-	V
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1	-	1	-	1	-	1	V
			10 V	-	2	-	2	-	2	-	2	V
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		T _{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I _{DD}	supply current	all valid input combinations; I _O = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	µA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	µA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	µA
C _I	input capacitance	digital inputs		-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 25 °C; for waveforms see Fig. 4; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nA to nY	5 V	18 ns + (0.55 ns/pF)C _L	-	45	90	ns
			10 V	9 ns + (0.23 ns/pF)C _L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	25	ns
t _{PLH}	LOW to HIGH propagation delay	nA to nY	5 V	13 ns + (0.55 ns/pF)C _L	-	40	80	ns
			10 V	9 ns + (0.23 ns/pF)C _L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	30	ns
t _{THL}	HIGH to LOW output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time	output nY	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

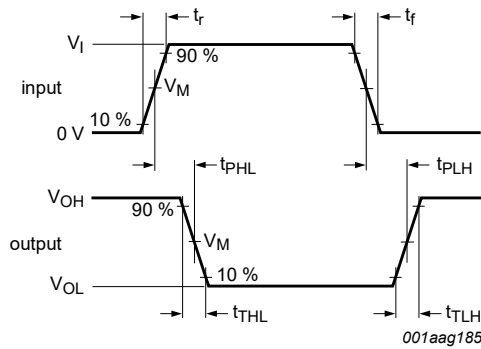
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 7. Dynamic power dissipation

V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula	Where
P _D	dynamic power dissipation	5 V	P _D = 600 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	f _i = input frequency in MHz; f _o = output frequency in MHz; C _L = output load capacitance in pF; Σ(f _o × C _L) = sum of the outputs; V _{DD} = supply voltage in V.
		10 V	P _D = 4000 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	
		15 V	P _D = 22000 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	

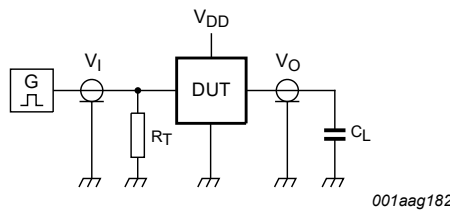
10.1. Waveforms and test circuit



Measurement points: $V_M = 0.5V_{DD}$.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Propagation delay and transition times



For test data refer to [Table 8](#).

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

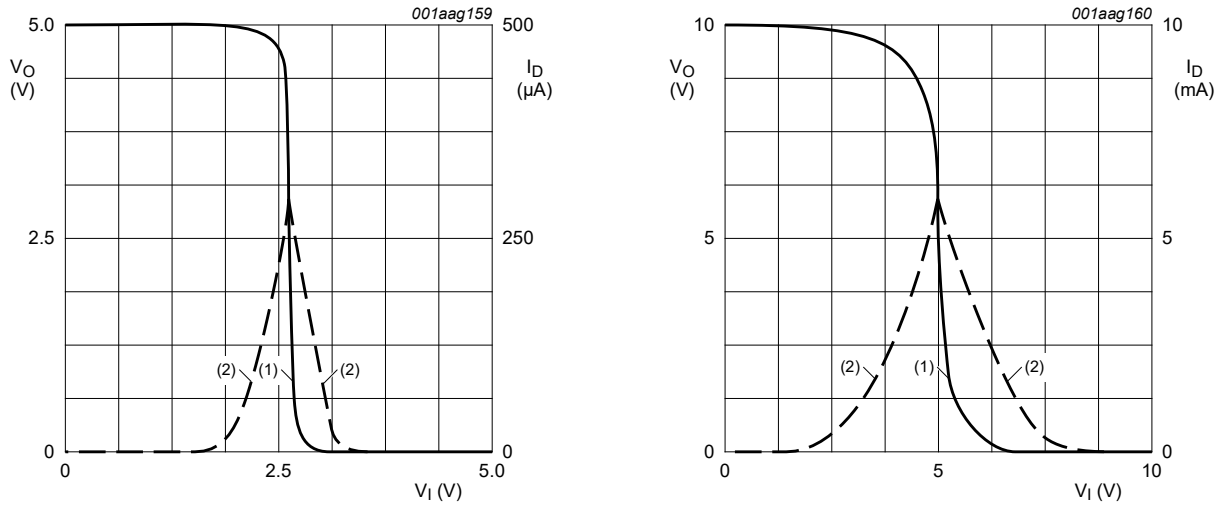
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 8. Test data

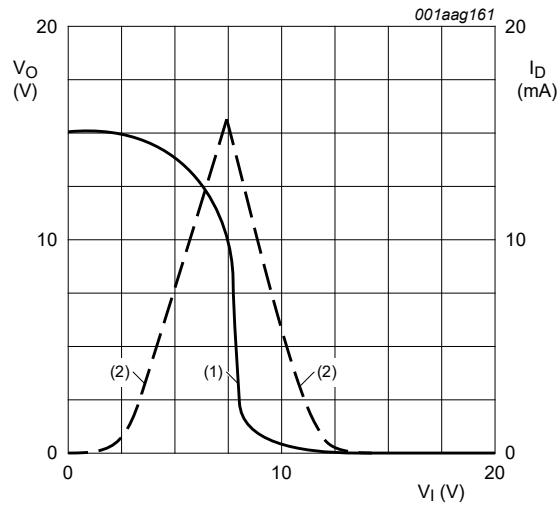
Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns

10.2. Transfer characteristics



a. $V_{DD} = 5\text{ V}$; $I_O = 0\text{ A}$

b. $V_{DD} = 10\text{ V}$; $I_O = 0\text{ A}$



c. $V_{DD} = 15\text{ V}$; $I_O = 0\text{ A}$

(1) V_O = output voltage.
 (2) I_D = drain current.

Fig. 6. Typical transfer characteristics

11. Application information

Some examples of applications for HEF4069UB.

[Fig. 7](#) shows an astable relaxation oscillator using two HEF4069UB inverters and two BAW62 diodes. The oscillation frequency is mainly determined by $R1 \times C1$, provided $R1 \ll R2$ and $R2 \times C2 \ll R1 \times C1$.

The function of $R2$ is to minimize the influence of the forward voltage across the protection diodes on the frequency; $C2$ is a stray (parasitic) capacitance.

The period T_p is given by $T_p = T_1 + T_2$,

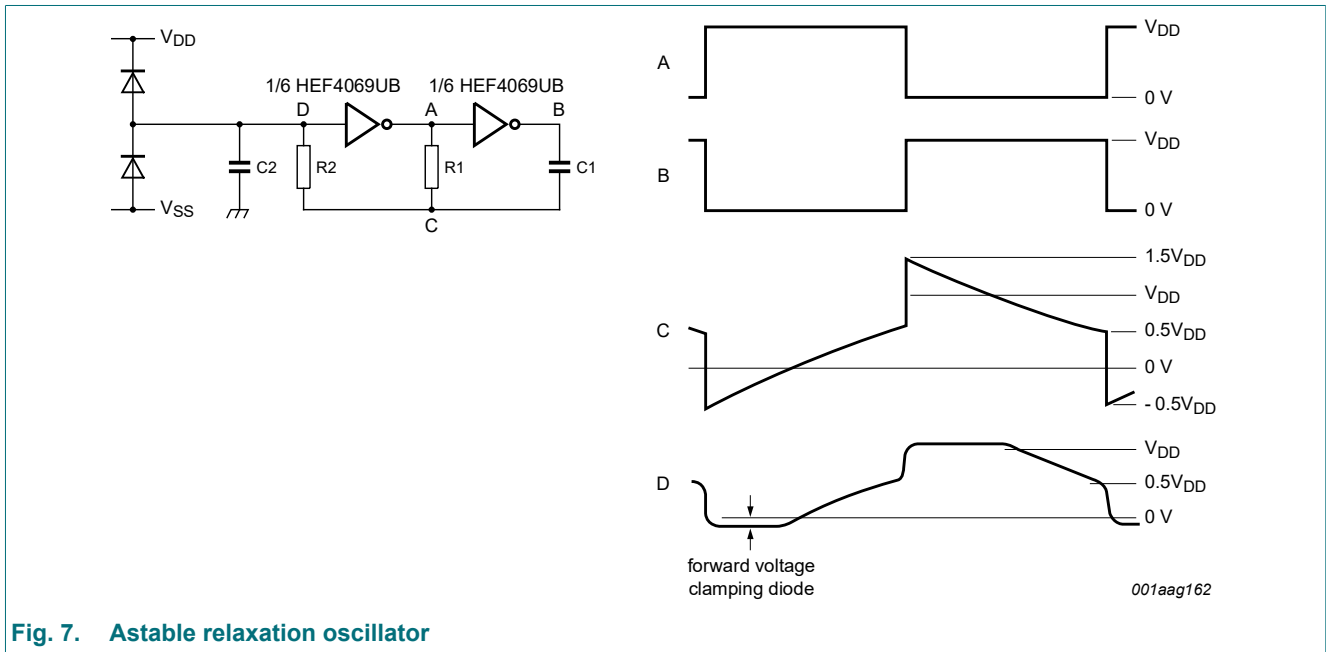
where:

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}}$$

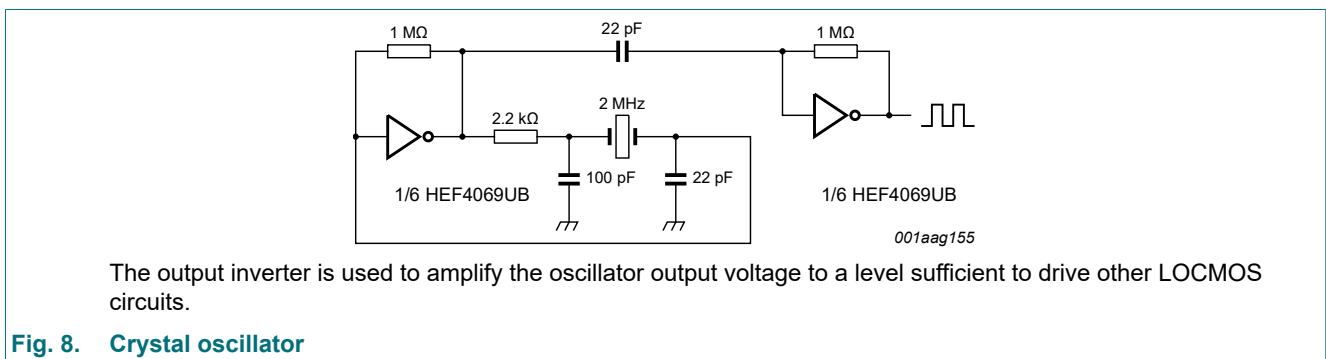
$$T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

V_{ST} = the signal threshold level of the inverter.

The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .



[Fig. 8](#) shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.



The output inverter is used to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig. 9 and Fig. 10 show voltage gain and supply current. Fig. 11 shows the test set-up and an example of an analog amplifier using one HEF4069UB.

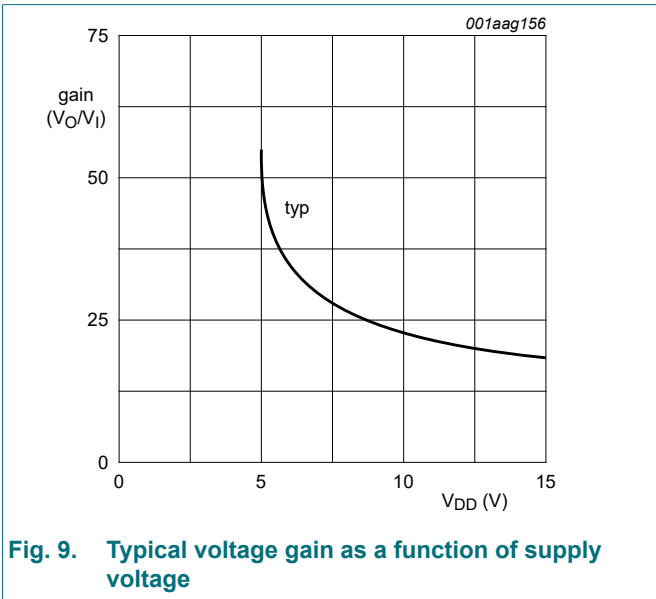


Fig. 9. Typical voltage gain as a function of supply voltage

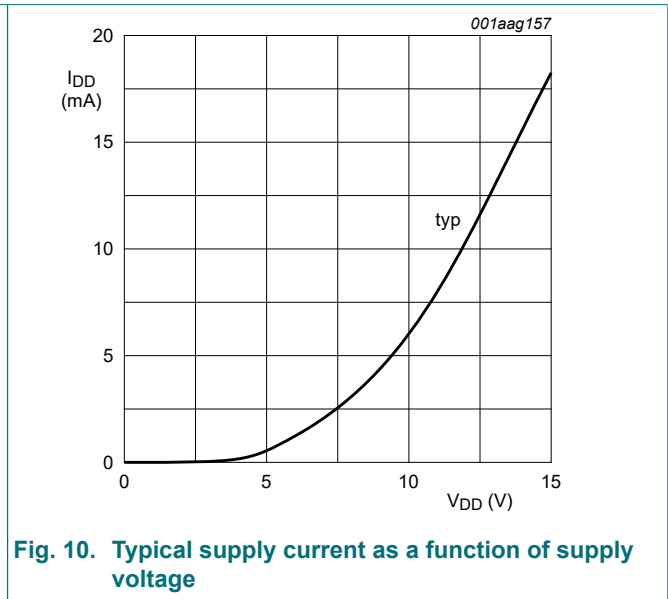


Fig. 10. Typical supply current as a function of supply voltage

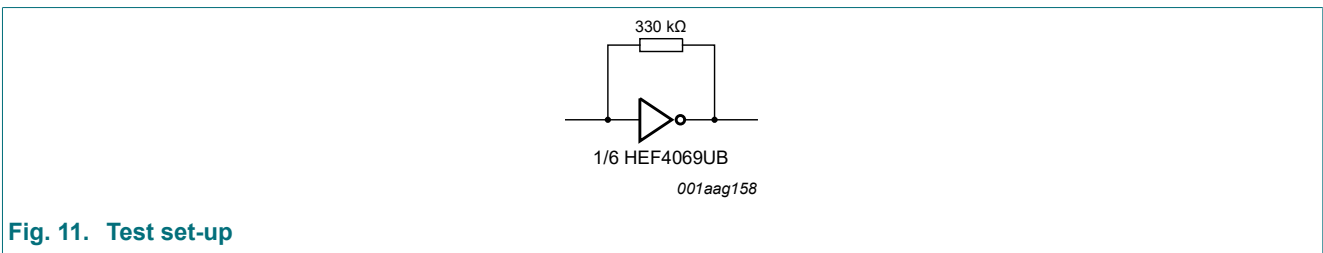


Fig. 11. Test set-up

Fig. 12 shows typical forward transconductance. Fig. 13 shows the test set-up.

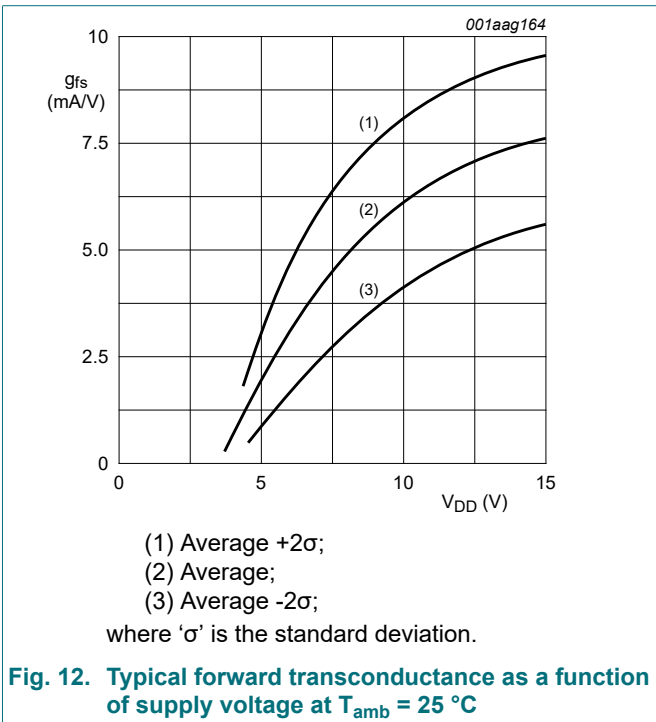


Fig. 12. Typical forward transconductance as a function of supply voltage at $T_{amb} = 25\text{ °C}$

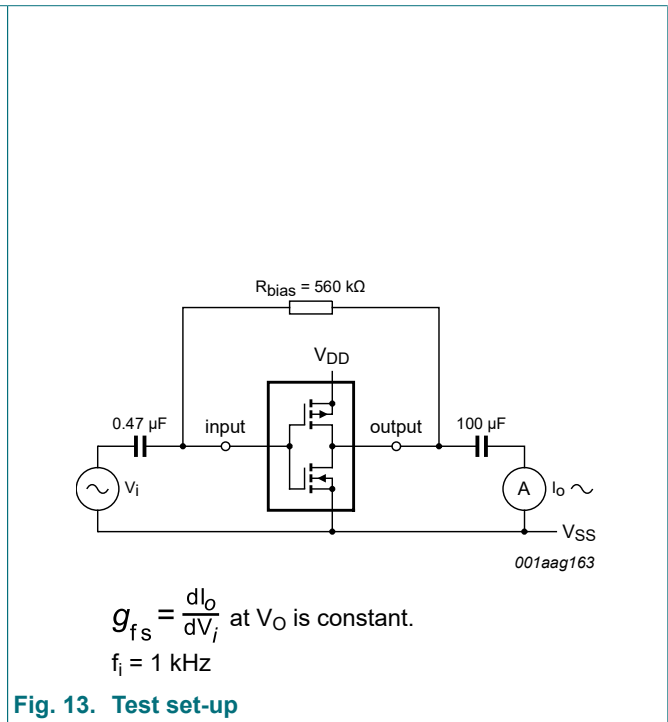


Fig. 13. Test set-up

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

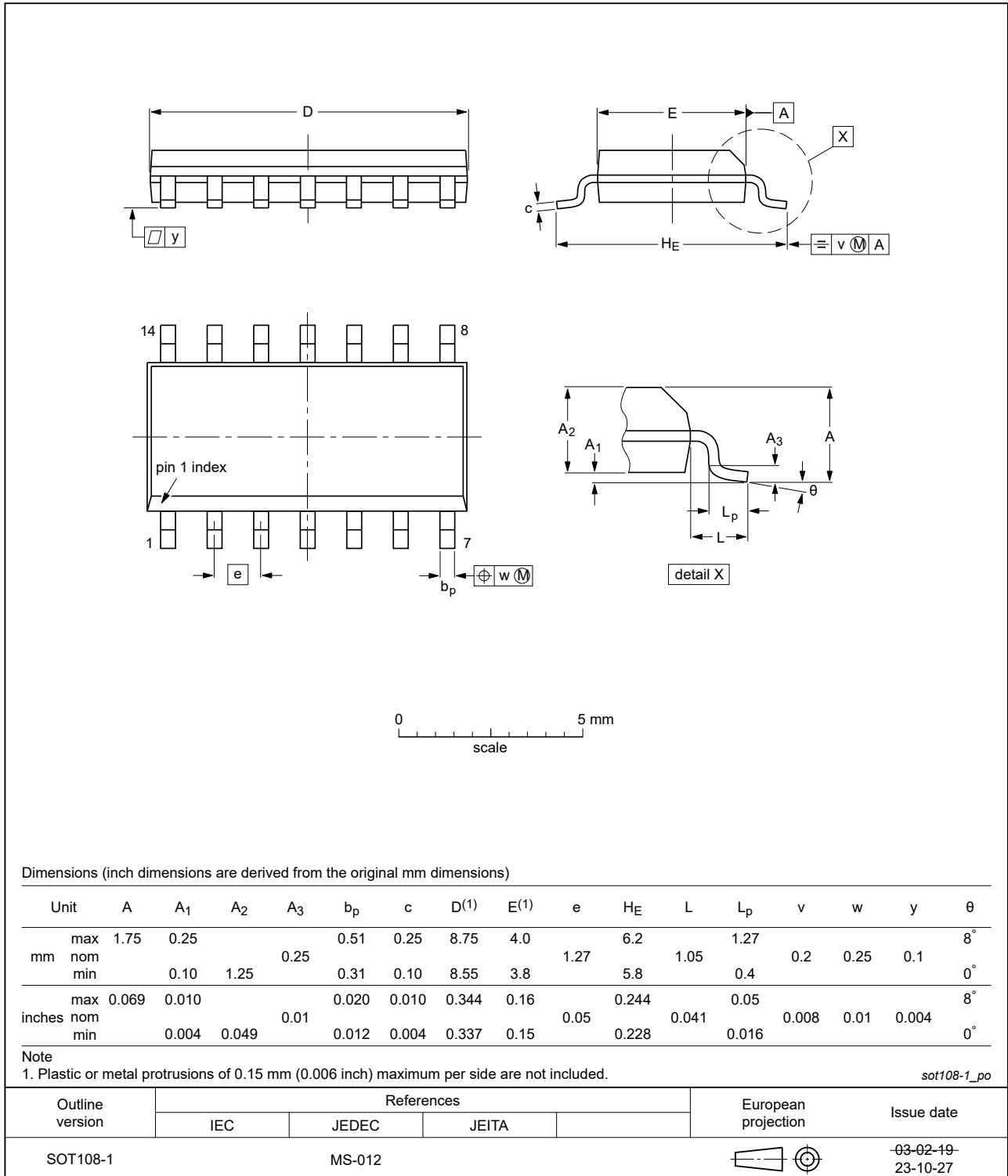


Fig. 14. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

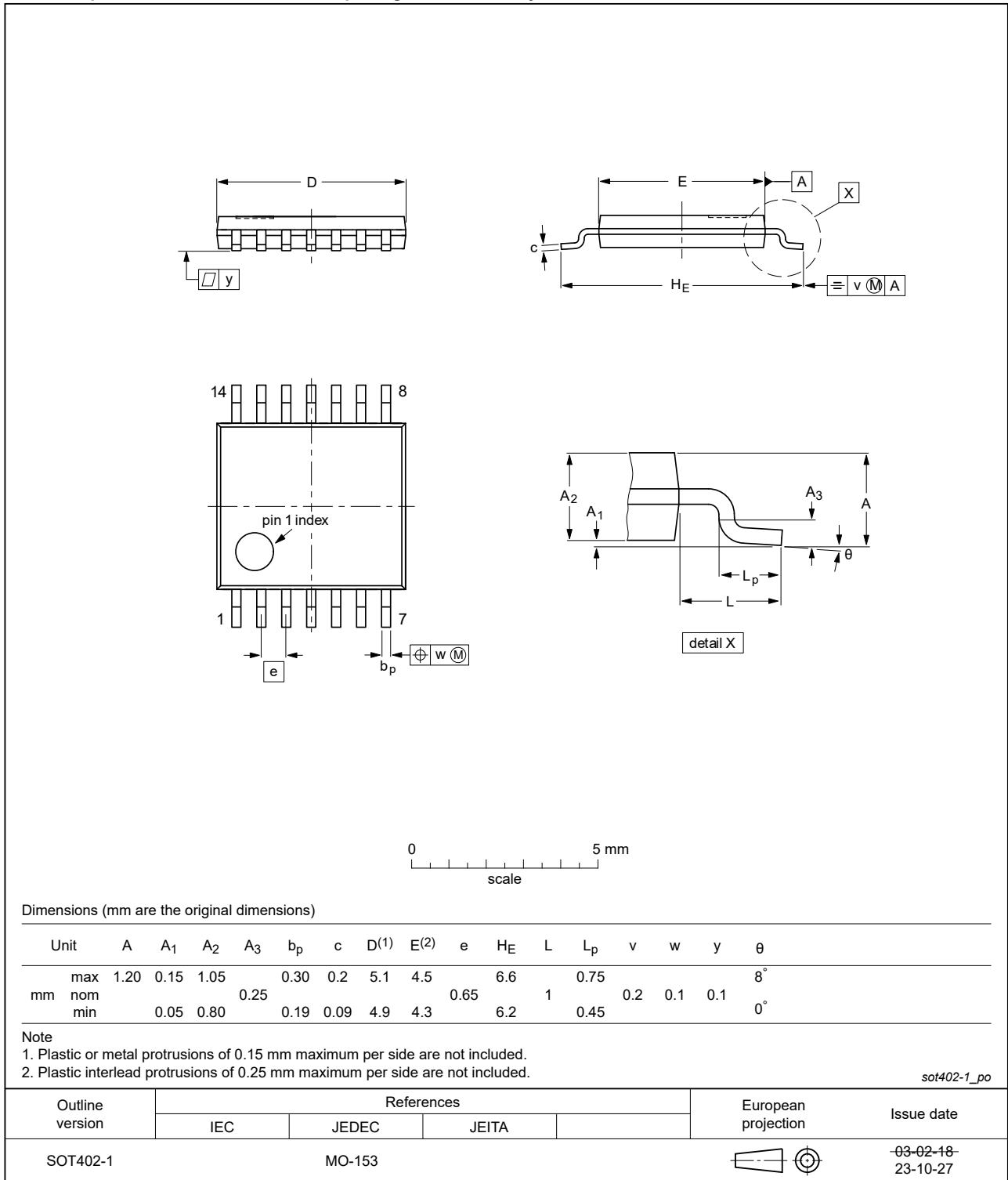


Fig. 15. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LOC MOS	Local Oxidation Complementary Metal-Oxide Semiconductor

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4069UB v.11	20240905	Product data sheet	-	HEF4069UB v10
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 14, Fig. 15: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 			
HEF4069UB v.10	20220210	Product data sheet	-	HEF4069UB v.9
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 3: Derating values for P_{tot} total power dissipation updated. 			
HEF4069UB v.9	20151216	Product data sheet	-	HEF4069UB v.8
Modifications:	<ul style="list-style-type: none"> • Type number HEF4069UBP (SOT27-1) removed. 			
HEF4069UB v.8	20111116	Product data sheet	-	HEF4069UB v.7
Modifications:	<ul style="list-style-type: none"> • Legal pages updated. • Changes in "General description", "Features and benefits" and "Applications". 			
HEF4069UB v.7	20110511	Product data sheet	-	HEF4069UB v.6
HEF4069UB v.6	20091208	Product data sheet	-	HEF4069UB v.5
HEF4069UB v.5	20090723	Product data sheet	-	HEF4069UB v.4
HEF4069UB v.4	20080704	Product data sheet	-	HEF4069UB_CNV v.3
HEF4069UB_CNV v.3	19950101	Product specification	-	HEF4069UB_CNV v.2
HEF4069UB_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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