

HEF4555B

1-of-4 decoder/demultiplexer

Rev. 5 — 18 November 2011

Product data sheet

1. General description

The HEF4555B contains two 1-of-4 decoders/demultiplexers. Each has two address inputs (nA0 and nA1, an active LOW enable input (n \bar{E}) and four mutually exclusive outputs which are active HIGH (nY0 to nY3). When used as a decoder, n \bar{E} when HIGH, forces nY0 to nY3 LOW. When used as a demultiplexer, the appropriate output is selected by the information on nA0 and nA1 with n \bar{E} as data input. All unselected outputs are LOW.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Code conversion
- Address decoding
- Demultiplexing: when using the enable input as data input

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF4555BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4555BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



5. Functional diagram

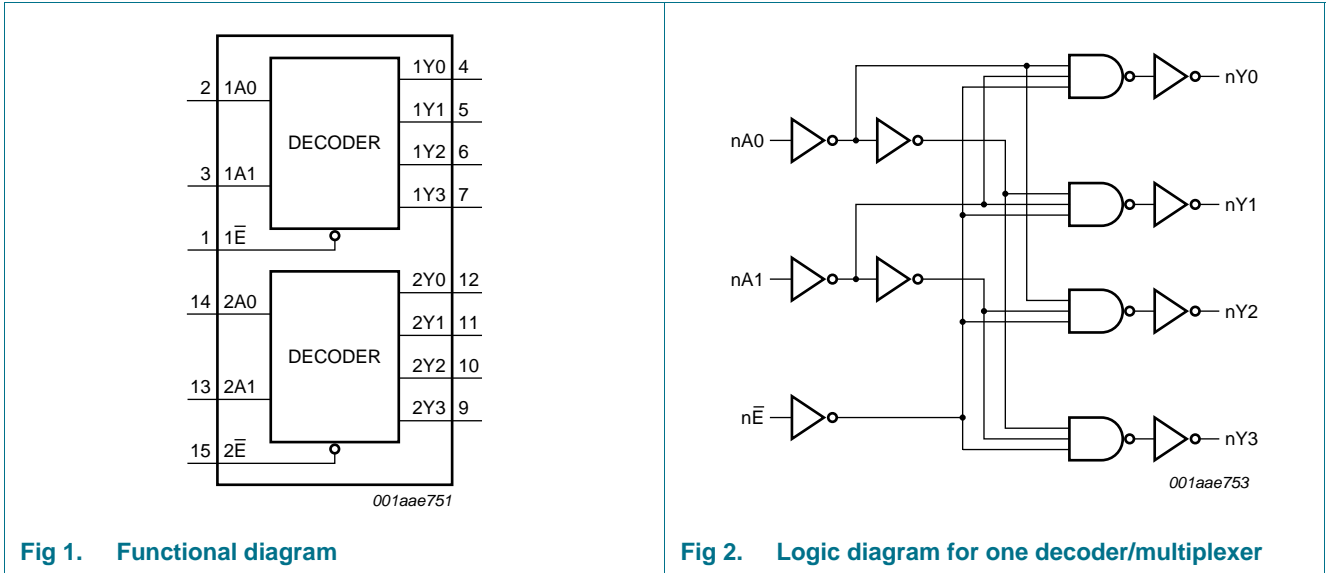


Fig 1. Functional diagram

Fig 2. Logic diagram for one decoder/multiplexer

6. Pinning information

6.1 Pinning

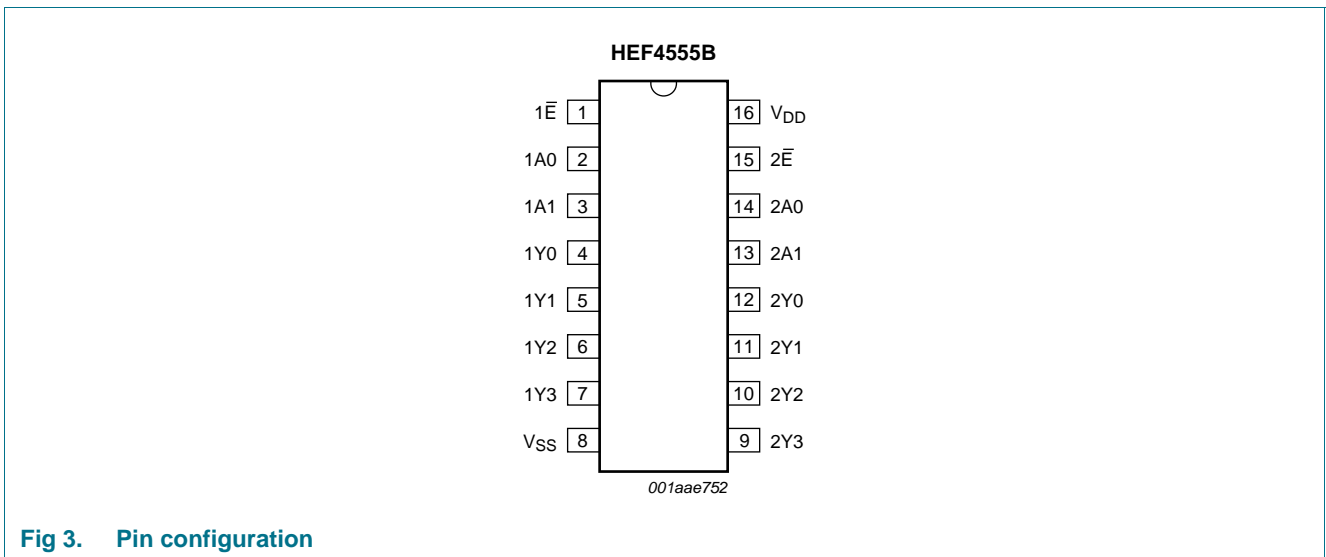


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 2A0, 2A1	2, 3, 14, 13	address input
$1\bar{E}$, $2\bar{E}$	1, 15	enable input (active LOW)
1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3	4, 5, 6, 7, 12, 11, 10, 9	output (active HIGH)
V_{DD}	16	supply voltage
V_{SS}	8	ground (GND)

7. Functional description

Table 3. Function selection^[1]

Inputs			Outputs			
$n\bar{E}$	nA0	nA1	nY0	nY1	nY2	nY3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	DIP16 package	^[1] -	750	mW
		SO16 package	^[2] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit			
				Min	Max	Min	Max	Min	Max				
V_{IH}	HIGH-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V			
			10 V	7.0	-	7.0	-	7.0	-	V			
			15 V	11.0	-	11.0	-	11.0	-	V			
V_{IL}	LOW-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V			
			10 V	-	3.0	-	3.0	-	3.0	V			
			15 V	-	4.0	-	4.0	-	4.0	V			
V_{OH}	HIGH-level output voltage	$ I_O < 1\ \mu\text{A}$; $V_I = V_{SS}$ or V_{DD}	5 V	4.95	-	4.95	-	4.95	-	V			
			10 V	9.95	-	9.95	-	9.95	-	V			
			15 V	14.95	-	14.95	-	14.95	-	V			
V_{OL}	LOW-level output voltage	$ I_O < 1\ \mu\text{A}$; $V_I = V_{SS}$ or V_{DD}	5 V	-	0.05	-	0.05	-	0.05	V			
			10 V	-	0.05	-	0.05	-	0.05	V			
			15 V	-	0.05	-	0.05	-	0.05	V			
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA			
			5 V	-	-0.52	-	-0.44	-	-0.36	mA			
			10 V	-	-1.3	-	-1.1	-	-0.9	mA			
			15 V	-	-3.6	-	-3.0	-	-2.4	mA			
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA			
			10 V	1.3	-	1.1	-	0.9	-	mA			
			15 V	3.6	-	3.0	-	2.4	-	mA			
I_I	input leakage current	$V_{DD} = 15\text{ V}$	15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA			
			I_{DD}	supply current	$I_O = 0\text{ A}$; $V_I = V_{SS}$ or V_{DD}	5 V	-	20	-	20	-	150	μA
						10 V	-	40	-	40	-	300	μA
C_I	input capacitance		15 V	-	80	-	80	-	600	μA			
			-	-	-	-	7.5	-	-	pF			

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nAn → nYn; see Figure 4	5 V	[1] $88\text{ ns} + (0.55\text{ ns/pF})C_L$	-	115	230	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	65	ns
		n \bar{E} → nYn	5 V	$98\text{ ns} + (0.55\text{ ns/pF})C_L$	-	125	250	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	95	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	65	ns
t_{PLH}	LOW to HIGH propagation delay	nAn → nYn	5 V	[1] $113\text{ ns} + (0.55\text{ ns/pF})C_L$	-	140	280	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	105	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	75	ns
		n \bar{E} → nYn	5 V	$123\text{ ns} + (0.55\text{ ns/pF})C_L$	-	150	295	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	75	ns
t_t	transition time	on nYn	5 V	[1][2] $10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

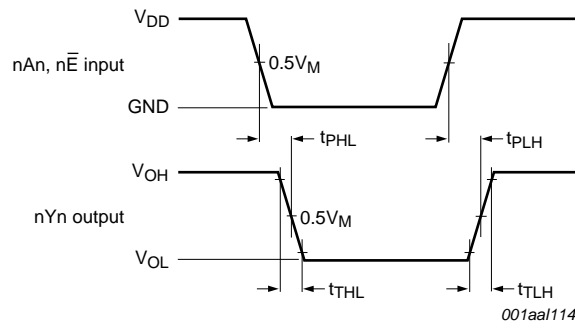
[2] Transition time t_t is the same as the HIGH to LOW and LOW to HIGH transition times t_{THL} and t_{TLH} .

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 18800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 45700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

12. Waveforms



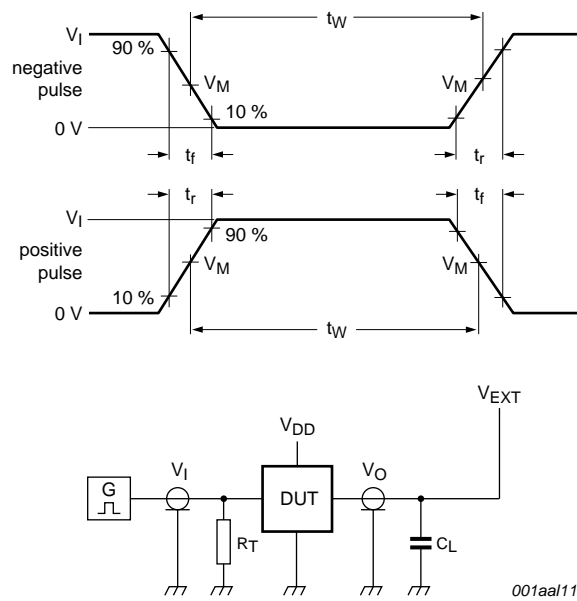
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Inputs nA_n and $n\bar{E}$ to output nY_n propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

Device Under Test (DUT);

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig 5. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input		Load	V_{EXT}	
	V_I	$t_r = t_f$	C_L	t_{PLH}, t_{PHL}	t_{THL}, t_{TLH}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	open	V_{DD}

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

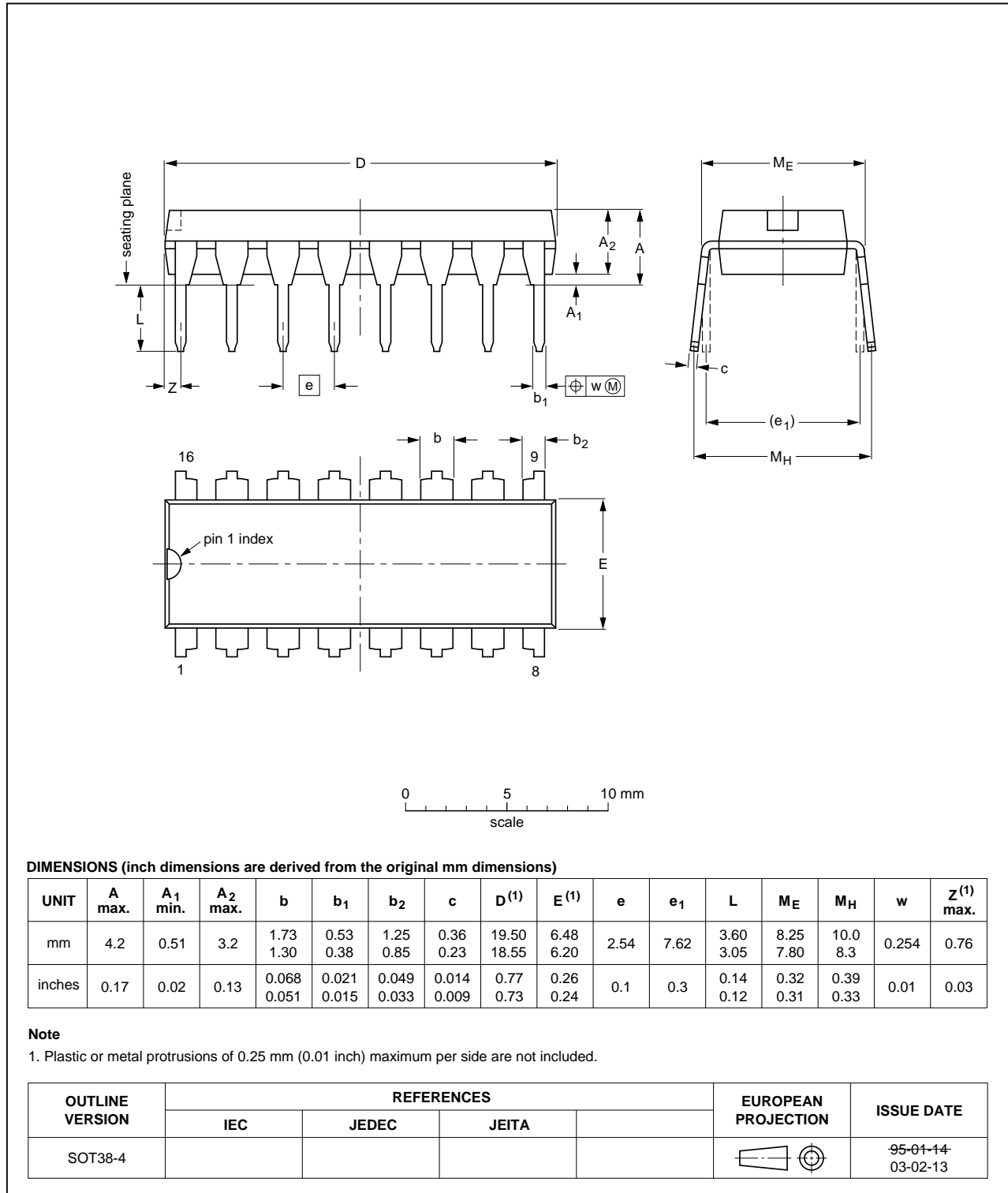


Fig 6. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

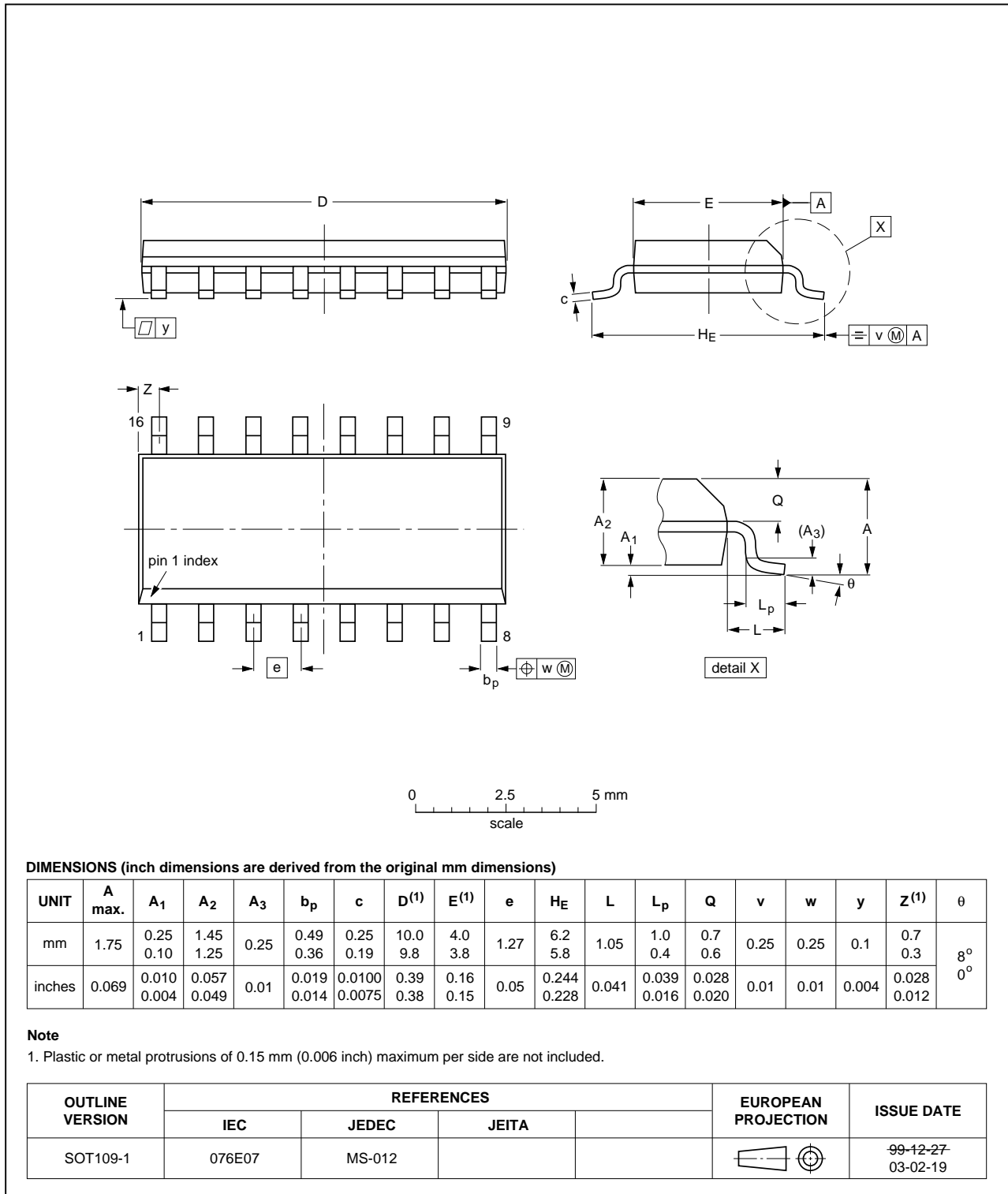


Fig 7. Package outline SOT109-1 (SO16)

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4555B v.5	20111118	Product data sheet	-	HEF4555B v.4
Modifications:	• Table 6 : I _{OH} minimum values changed to maximum			
HEF4555B v.4	20100106	Product data sheet	-	HEF4555B_CNV v.3
HEF4555B_CNV v.3	19950101	Product specification	-	HEF4555B_CNV v.2
HEF4555B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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