

HFBR-1116TZ Transmitter

HFBR-2116TZ Receiver

Fiber Optic Transmitter and Receiver Data Links for 155 MBd



Data Sheet

Description

The HFBR-1116TZ/-2116TZ series of data links are high-performance, cost-efficient, transmitter and receiver modules for serial optical data communication applications specified at 155 Mbps for ATM UNI applications.

These modules are designed for 50 or 62.5 μm core multimode optical fiber and operate at a nominal wavelength of 1300 nm. They incorporate our high-performance, reliable, long-wavelength, optical devices and proven circuit technology to give long life and consistent performance.

Transmitter

The transmitter utilizes a 1300 nm surface-emitting InGaAsP LED, packaged in an optical subassembly. The LED is DC-coupled to a custom IC which converts differential-input, PECL logic signals, ECL-referenced (shifted) to a +5 V power supply, into an analog LED drive current.

Receiver

The receiver utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. The PIN-preamplifier combination is AC-coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. Both the Data and Signal Detect Outputs are differential. Also, both Data and Signal Detect Outputs are PECL compatible, ECL-referenced (shifted) to a +5 V power supply.

Package

The overall package concept for the Data Links consists of the following basic elements: two optical subassemblies, two electrical subassemblies, and the outer housings as illustrated in Figure 1.

Features

- Full compliance with the optical performance requirements of the ATM Forum UNI SONET OC-3 multimode physical layer specification
- Other versions available for:
 - FDDI
 - Fibre Channel
- Compact 16-pin DIP package with plastic ST* connector
- Wave solder and aqueous wash process compatible package
- Manufactured in an ISO 9001 certified facility

Applications

- ATM switches, hubs, and network interface cards
- Multimode fiber ATM wiring closet-to-desktop links
- Point-to-point data communications
- Replaces DLT/R1040-ST1 model transmitters and receivers

* ST is a registered trademark of AT&T Lightguide Cable Connectors.

The package outline drawing and pinout are shown in Figures 2 and 3. The details of this package outline and pinout are compatible with other data-link modules from other vendors.

The optical subassemblies consist of a transmitter subassembly in which the LED resides and a receiver subassembly housing the PIN-preamplifier combination.

The electrical subassemblies consist of a multi-layer printed circuit board on which the IC chips and various surface-mounted, passive circuit elements are attached.

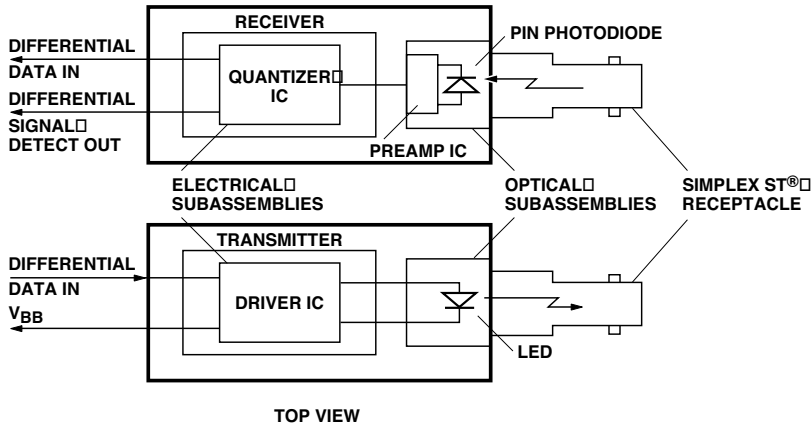
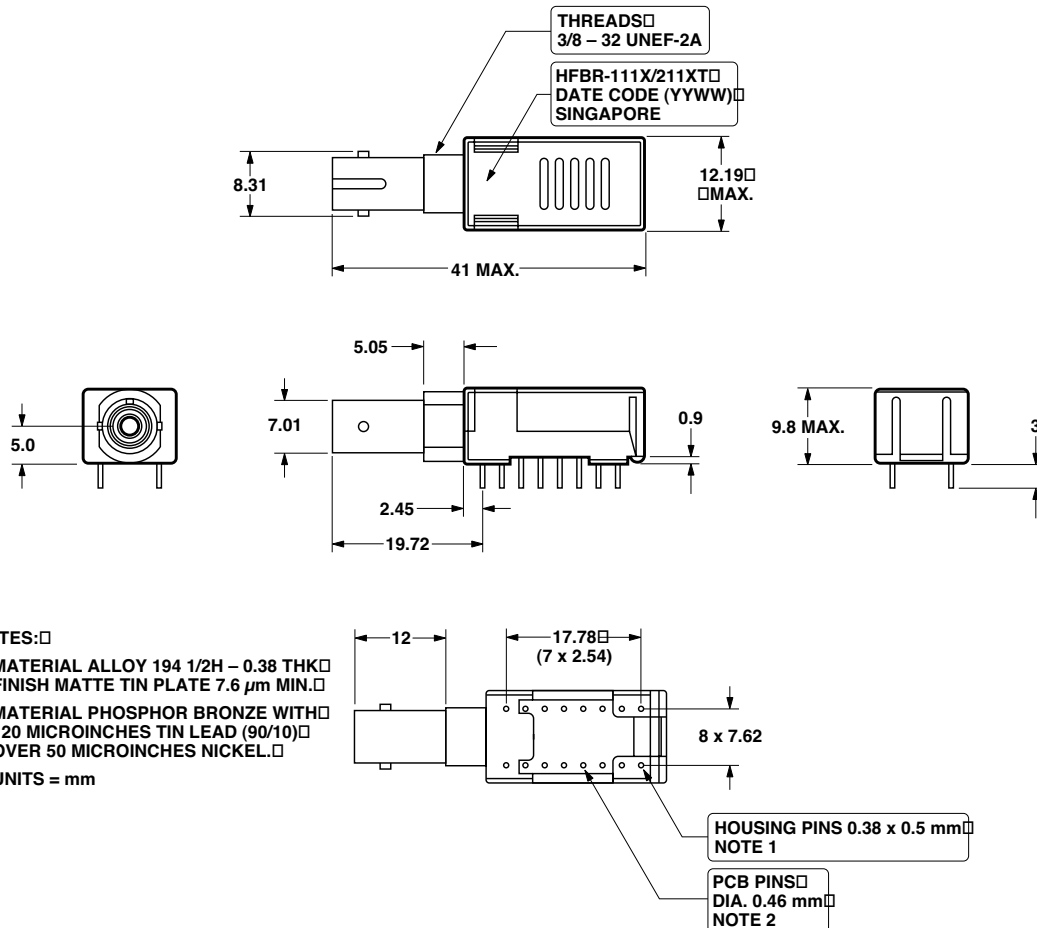


Figure 1. Transmitter and receiver block diagram.



NOTES:

1. MATERIAL ALLOY 194 1/2H - 0.38 THK
FINISH MATTE TIN PLATE 7.6 μm MIN.
2. MATERIAL PHOSPHOR BRONZE WITH
120 MICRINCHES TIN LEAD (90/10)
OVER 50 MICRINCHES NICKEL.
3. UNITS = mm

Figure 2. Package outline drawing.

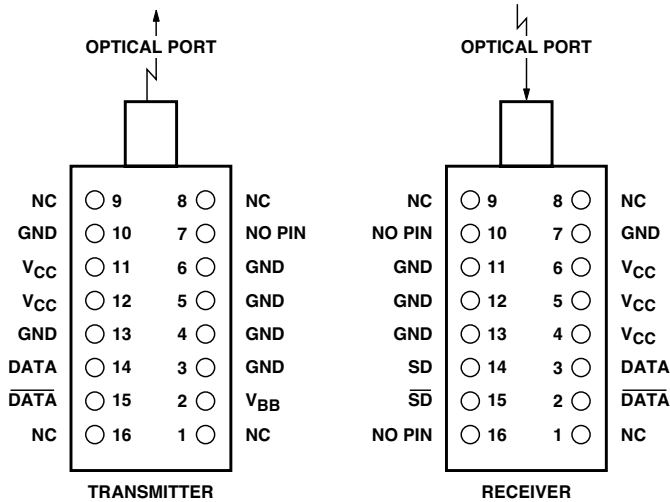


Figure 3. Pinout drawing.

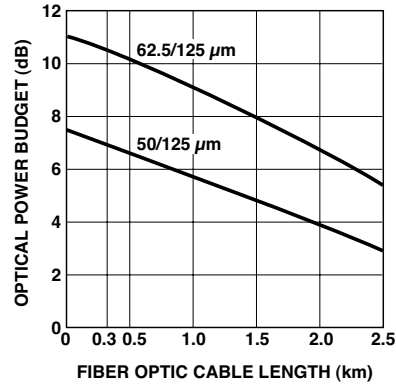


Figure 4. Optical power budget at BOL vs. fiber optic cable length.

Each transmitter and receiver package includes an internal shield for the electrical subassembly to ensure low EMI emissions and high immunity to external EMI fields.

The outer housing, including the ST* port, is molded of filled, nonconductive plastic to provide mechanical strength and electrical isolation. For other port styles, please contact your Avago Technologies Sales Representative.

Each data-link module is attached to a printed circuit board via the 16-pin DIP interface. Pins 8 and 9 provide mechanical strength for these plastic-port devices and will provide port-ground for forthcoming metal-port modules.

Application Information

The Applications Engineering group of the Fiber Optics Product Division is available to assist you with the technical understanding and design tradeoffs associated with these transmitter and receiver modules. You can contact them through your Avago Technologies sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transmitter and Receiver Optical Power Budget versus Link Length

The Optical Power Budget (OPB) is the available optical power for a fiber-optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transmitter and receiver specified in this data sheet at the Beginning of Life (BOL). This curve represents the attenuation and chromatic plus modal dispersion losses associated with 62.5/125 μm and 50/125 μm fiber cables only. The area under the curve represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs; however, Avago 1300 nm LEDs will experience less than 1 dB of aging over normal commercial equipment mission-life periods. Contact your Avago Technologies sales representative for additional details.

Figure 4 was generated with an Avago fiber-optic link model containing the current industry conventions for fiber cable specifications and the draft ANSI T1E1.2. These parameters are reflected in the guaranteed performance of the transmitter and receiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI T1E1.2 committee, to establish the optical performance requirements for various fiberoptic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

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Transmitter and Receiver Signaling Rate Range and BER Performance

For purposes of definition, the symbol rate (Baud), also called signaling rate, is the reciprocal of the symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in 115 Mbps SONET OC-3 applications, the performance of Avago Technologies' 1300 nm data link modules, HFBR-1116TZ/-2116TZ, is guaranteed to the full conditions listed in the individual product specification tables.

The data link modules may be used for other applications at signaling rates different than the 155 Mbps with some variation in the link optical power budget. Figure 5 gives an indication of the typical performance of these 1300 nm products at different rates.

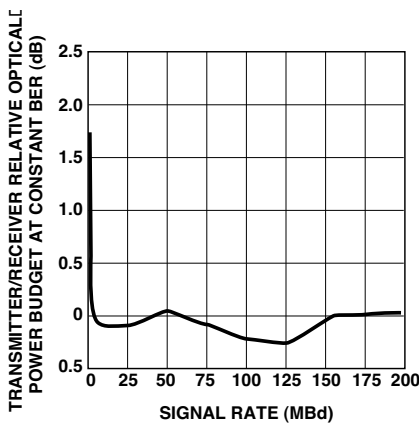
These data link modules can also be used for applications which require different bit-error-ratio (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receiver input optical power level.

Data Link Jitter Performance

The Avago 1300 nm data link modules are designed to operate per the system jitter allocations stated in Table B1 of Annex B of the ANSI T1E1.2 Revision 3 standard.

The 1300 nm transmitter will tolerate the worst-case input electrical jitter allowed in Annex B without violating the worst-case output jitter requirements.

The 1300 nm receiver will tolerate the worst-case input optical jitter allowed in Annex B without violating the worst-case output electrical jitter allowed.



- CONDITIONS: □
1. PRBS 2⁷-1 □
 2. DATA SAMPLED AT CENTER OF DATA SYMBOL □
 3. BER = 10⁻⁶ □
 4. T_A = 25° C □
 5. V_{CC} = 5 Vdc □
 6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 5. Transmitter/Receiver relative optical power budget at constant BER vs. signaling rate.

The jitter specifications stated in the following transmitter and receiver specification table are derived from the values in Table B1 of Annex B. They represent the worst-case jitter contribution that the transmitter and receiver are allowed to make to the overall system jitter without violating the Annex B allocation example. In practice, the typical jitter contribution of the Avago Technologies' data link modules is well below the maximum amounts.

Recommended Handling Precautions

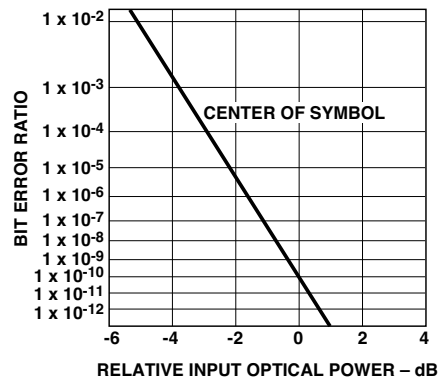
It is advised that normal static precautions be taken in the handling and assembly of these data link modules to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-1116TZ/-2116TZ series meets MIL-STD-883C Method 3015.4 Class 2.

Care should be taken to avoid shorting the receiver Data or Signal Detect Outputs directly to ground without proper current-limiting impedance.

Solder and Wash Process Compatibility

The transmitter and receiver are delivered with protective process caps covering the individual ST* ports. These process caps protect the optical subassemblies during wave solder and aqueous wash processing and act as dust covers during shipping.

These data link modules are compatible with either industry standard wave- or hand-solder processes.



- CONDITIONS: □
1. 155 MBd □
 2. PRBS 2⁷-1 □
 3. T_A = 25° C □
 4. V_{CC} = 5 Vdc □
 5. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

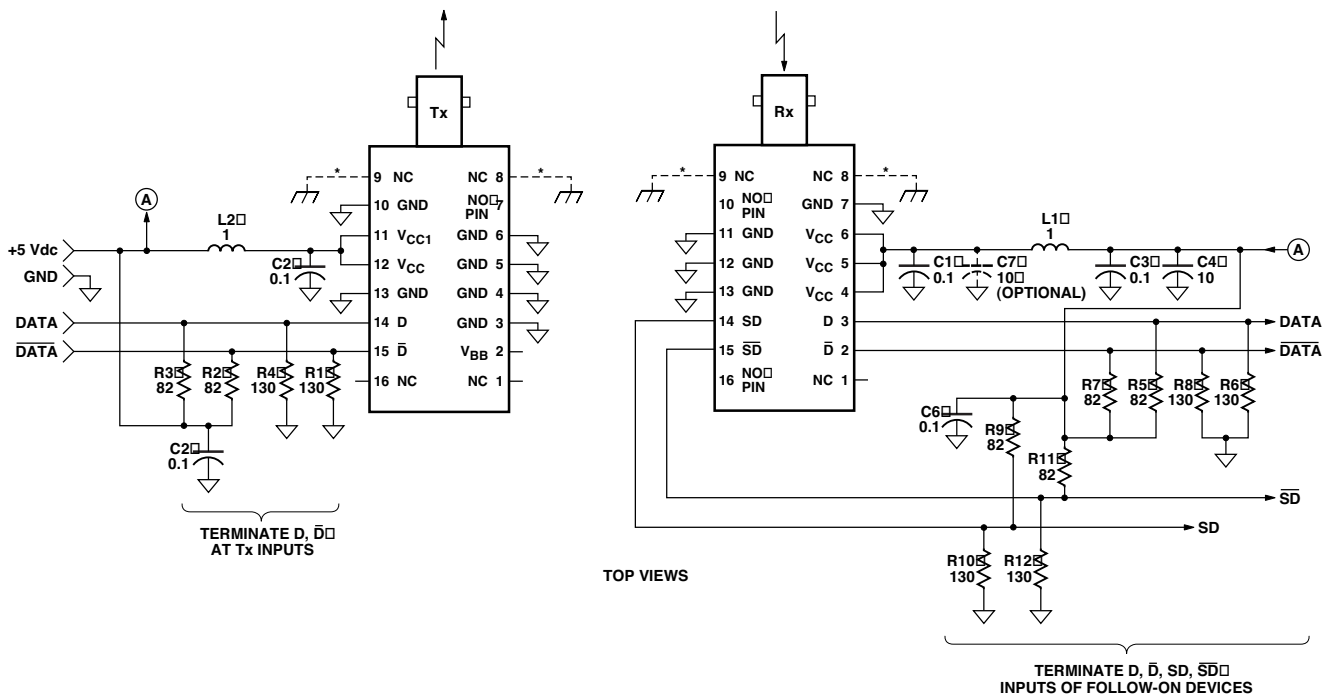
Figure 6. Bit error ratio vs. relative receiver input optical power.

Shipping Container

The data link modules are packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout – Interface Circuit and Layout Guidelines

It is important to take care in the layout of your circuit board to achieve optimum performance from these data link modules. Figure 7 provides a good example of a power supply filter circuit that works well with these parts. Also, suggested signal terminations for the Data, Data-bar, Signal Detect and Signal Detect-bar lines are shown. Use of a multilayer, ground-plane printed circuit board will provide good high-frequency circuit performance with a low inductance ground return path. See additional recommendations noted in the interface schematic shown in Figure 7.



Notes:

1. Resistance is in ohms. Capacitance is in microfarads. Inductance is in microhenries.
2. Terminate transmitter input data and data-bar at the transmitter input pins. Terminate the receiver output data, data-bar, and signal detect-bar at the follow-on device input pins. For lower power dissipation in the signal detect termination circuitry with small compromise to the signal quality, each signal detect output can be loaded with 510 ohms to ground instead of the two resistor, split-load pecl termination shown in this schematic.
3. Make differential signal paths short and of same length with equal termination impedance.
4. Signal traces should be 50 ohms microstrip or stripline transmission lines. Use multilayer, ground-plane printed circuit board for best high-frequency performance.
5. Use high-frequency, monolithic ceramic bypass capacitors and low series DC resistance inductors. Recommend use of surface-mount coil inductors and capacitors. In low noise power supply systems, ferrite bead inductors can be substituted for coil inductors. Locate power supply filter components close to their respective power supply pins. C7 is an optional bypass capacitor for improved, low-frequency noise power supply filter performance.
6. Device ground pins should be directly and individually connected to ground.
7. Caution: do not directly connect the fiber-optic module PECL outputs (data, data-bar, signal detect, signal detect-bar, V_{BB}) to ground without proper current limiting impedance.
8. (*) Optional metal ST optical port transmitter and receiver modules will have pins 8 and 9 electrically connected to the metal port only and not connected to the internal signal ground.

Figure 7. Recommended interface circuitry and power supply filter circuits.

Board Layout – Hole Pattern

The Avago transmitter and receiver hole pattern is compatible with other data link modules from other vendors. The drawing shown in Figure 8 can be used as a guide in the mechanical layout of your circuit board.

Regulatory Compliance

These data link modules are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. Additional information is available from your Avago sales representative.

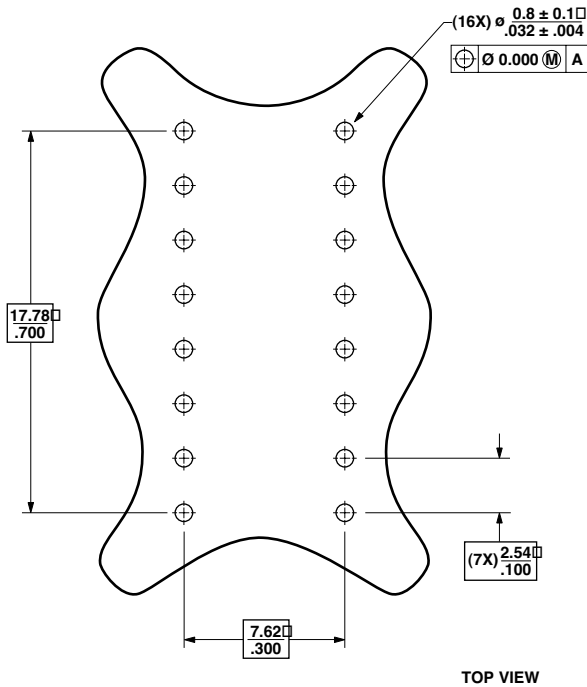
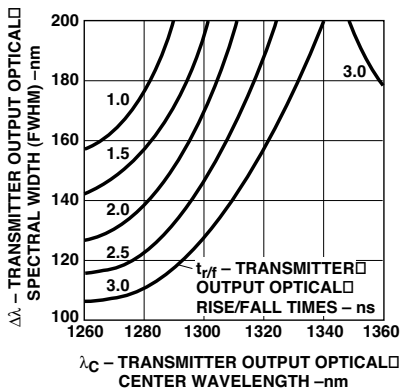


Figure 8. Recommended board layout hole pattern.

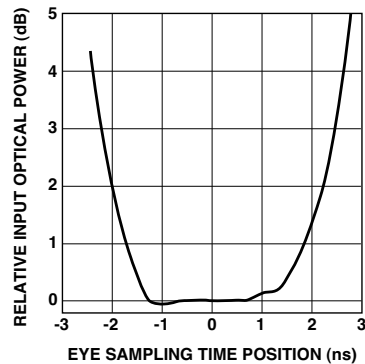
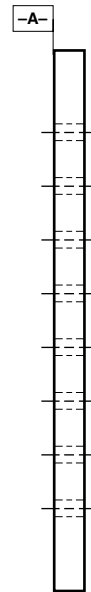


HFBR-1116T TRANSMITTER TEST RESULTS OF λ_c , $\Delta\lambda$ AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 9. HFBR-1116TZ transmitter output optical spectral width (FWHM) vs. transmitter output optical center wavelength and rise/fall times.

All HFBR-1116TZ LED transmitters are classified as IEC-825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. See Application Note 1094, *LED Device Classifications with Respect to AEL Values as Defined in the IEC 825-1 Standard and the European EN60825-1 Directive*.

The material used for the housing in the HFBR-1116TZ/-2116TZ series is Ultem 2100 (GE). Ultem 2100 is recognized for a UL flammability rating of 94V-0 (UL File Number E121562) and the CSA (Canadian Standards Association) equivalent (File Number LS88480).



CONDITIONS:
 1. $T_A = 25^\circ \text{C}$
 2. $V_{CC} = 5 \text{ Vdc}$
 3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
 4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
 5. NOTE 15 AND 16 APPLY.

Figure 10. HFBR-2116TZ receiver input optical power vs. eye sampling time position.

HFBR-1116TZ Transmitter Pin-Out Table

Pin	Symbol	Functional Description	Reference
1	NC	No internal connect, used for mechanical strength only	
2	V _{BB}	V _{BB} Bias output	
3	GND	Ground	Note 3
4	GND	Ground	Note 3
5	GND	Ground	Note 3
6	GND	Ground	Note 3
7	OMIT	No pin	
8	NC	No internal connect, used for mechanical strength only	Note 5
9	NC	No internal connect, used for mechanical strength only	Note 5
10	GND	Ground	Note 3
11	V _{CC}	Common supply voltage	Note 1
12	V _{CC}	Common supply voltage	Note 1
13	GND	Ground	Note 3
14	DATA	Data input	Note 4
15	$\overline{\text{DATA}}$	Inverted Data input	Note 4
16	NC	No internal connect, used for mechanical strength only	

HFBR-2116TZ Receiver Pin-Out Table

Pin	Symbol	Functional Description	Reference
1	NC	No internal connect, used for mechanical strength only	
2	$\overline{\text{DATA}}$	Inverted Data input	Note 4
3	DATA	Data input	Note 4
4	V _{CC}	Common supply voltage	Note 1
5	V _{CC}	Common supply voltage	Note 1
6	V _{CC}	Common supply voltage	Note 1
7	GND	Ground	Note 3
8	NC	No internal connect, used for mechanical strength only	Note 5
9	NC	No internal connect, used for mechanical strength only	Note 5
10	OMIT	No pin	
11	GND	Ground	Note 3
12	GND	Ground	Note 3
13	GND	Ground	Note 3
14	SD	Signal Detect	Note 2, 4
15	$\overline{\text{SD}}$	Inverted Signal Detect	Note 2, 4
16	OMIT	No pin	

Notes:

1. Voltages on V_{CC} must be from the same power supply (they are connected together internally).
2. Signal Detect is a logic signal that indicates the presence or absence of an input optical signal. A logic-high, V_{OH}, on Signal Detect indicates presence of an input optical signal. A logic-low, V_{OL}, on Signal Detect indicates an absence of input optical signal.
3. All GNDs are connected together internally and to the internal shield.
4. DATA, $\overline{\text{DATA}}$, SD, $\overline{\text{SD}}$ are open-emitter output circuits.
5. On metal-port modules, these pins are redefined as "Port Connection."

Specifications – Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Lead Soldering Temperature	T_{SOLD}			260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.5		5.5	V	
Data Input Voltage – Low	$V_{IL} - V_{CC}$	-1.810		-1.475	V	
Data Input Voltage – High	$V_{IH} - V_{CC}$	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 2

HFBR-1116TZ Transmitter Electrical Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		145	185	mA	Note 3
Power Dissipation	P_{DISS}		0.76	1.1	Ω	Note 5
Threshold Voltage	$V_{BB} - V_{CC}$	-1.42	-1.3	-1.24	V	Note 24
Data Input Current – Low	I_{IL}	-350	0		μs	
Data Input Current – High	I_{IH}		14	350	μs	

HFBR-1116TZ Receiver Electrical Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ to 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		82	145	mA	Note 4
Power Dissipation	P_{DISS}		0.3	0.5	Ω	Note 5
Data Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 6
Data Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 6
Data Output Rise Time	t_r	0.35		2.2	ns	Note 7
Data Output Fall Time	t_f	0.35		2.2	ns	Note 7
Signal Detect Output Voltage – Low (De-asserted)	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 6
Signal Detect Output Voltage – High (Asserted)	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 6
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 7
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 7

HFBR-1116TZ Transmitter Optical Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 μm , NA = 0.275 fiber	P_O , BOL	-19		-14	dBm avg.	Note 8
	P_O , EOL	-20		-14		
Output Optical Power 50/125 μm , NA = 0.20 fiber	P_O , BOL	-22.5		-14	dBm avg.	Note 8
	P_O , EOL	-23.5		-14		
Optical Extinction Ratio			0.001	0.03	%	Note 9
			-50	-35	dB	
Output Optical Power at Logic "O" State	P_O ("O")			-45	dBm avg.	Note 10
Center Wavelength	λ_C	1270	1310	1380	nm	Note 23 Figure 9
Spectral Width – FWHM – nm RMS	$\Delta\lambda$		137		nm	Note 11, 23 Figure 9
			58		nm RMS	
Optical Rise Time	t_r	0.6	1.0	3.0	ns	Note 12, 23 Figure 9
Optical Fall Time	t_f	0.6	2.1	3.0	ns	Note 12, 23 Figure 9
Systematic Jitter Contributed by the Transmitter	SJ		0.04	1.2	ns p-p	Note 13
Random Jitter Contributed by the Transmitter	RJ		0	0.52	ns p-p	Note 14

HFBR-2116TZ Receiver Optical Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	P_{IN} Min. (W)			-31	dBm avg.	Note 15, Figure 10
Input Optical Power Minimum at Eye Center	P_{IN} Min. (C)			-31	dBm avg.	Note 16, Figure 10
Input Optical Power Maximum	P_{IN} Max.	-14			dBm avg.	Note 15
Operating Wavelength	λ	1260		1360	nm	
Systematic Jitter Contributed by the Receiver	SJ		0.2	1.2	ns p-p	Note 17
Random Jitter Contributed by the Receiver	RJ		1	1.91	ns p-p	Note 18
Signal Detect – Asserted	P_A	$P_D + 1.5\text{ dB}$		-31	dBm avg.	Note 19
Signal Detect – De-asserted	P_D	-45			dBm avg.	Note 20
Signal Detect – Hysteresis	$P_A - P_D$	1.5			dB	
Signal Detect – Asserted Time (off to on)	t_{SDA}	0	55	100	μs	Note 21
Signal Detect – De-asserted Time (on to off)	t_{SDD}	0	110	350	μs	Note 22

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to $V_{CC} - 2 V$.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. This value is measured with the outputs terminated into 50 Ω connected to $V_{CC} - 2 V$ and an Input Optical Power level of -14 dBm average.
5. The power dissipation value is the power dissipated in the transmitter and receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
6. This value is measured with respect to $V_{CC} - 2 V$ with the output terminated into 50 Ω connected to $V_{CC} - 2 V$.
7. The output rise and fall times are measured between 20% and 80% levels with the output connected to $V_{CC} - 2 V$ through 50 Ω .
8. These optical power values are measured with the following conditions:
 - The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Avago Technologies's 1300 nm LED products is < 1dB, as specified in this data sheet.
 - Over the specified operating voltage and temperature ranges.
 - With 25 MBd (12.5 MHz square-wave), input signal.
 - At the end of one meter of noted optical fiber with cladding modes removed.The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
9. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a 25 MBd (12.5 MHz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.
10. The transmitter will provide this low level of Output Optical Power when driven by a logic "0" input. This can be useful in link troubleshooting.
11. The relationship between Full Width Half Maximum and RMS values for Spectral Width is derived from the assumption of a Gaussian shaped spectrum which results in a $2.35 \times \text{RMS} = \text{FWHM}$ relationship.
12. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by a 25 MBd (12.5 MHz square-wave) input signal. The ANSI T1E1.2 committee has designated the possibility of defining an eye pattern mask for the transmitter output optical power as an item for further study. Avago will incorporate this requirement into the specifications for these products if it is defined. The HFBR-1116TZ transmitter typically complies with the template requirements of CCITT (now ITU-T) G.957 Section 3.25, Figure 2 for the STM-1 rate, excluding the optical receiver filter normally associated with single-mode fiber measurements which is the likely source for the ANSI T1E1.2 committee to follow in this matter.
13. Systematic Jitter contributed by the transmitter is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. Systematic Jitter is measured at 50% threshold using a 155.52, $2^7 - 1$ pseudo-random bit stream data pattern input signal.
14. Random Jitter contributed by the transmitter is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
15. This specification is intended to indicate the performance of the receiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window timewidth) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit-Error-Ratio (BER) better than or equal to 2.5×10^{-10} .
 - At the Beginning of Life (BOL).
 - Over the specified operating voltage and temperature ranges.
 - Input is a 155.52 MBd, $2^{23} - 1$ PRBS data pattern with a 72 "1"s and 72 "0"s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix 1.
 - Receiver data window time-width is 1.23 ns or greater for the clock recovery circuit to operate in. The actual test window time-width is set to simulate the effect of worst-case input optical jitter based on the transmitter jitter values from the specification tables. The test window time-width is 3.32 ns.
16. All conditions of Note 15 apply except that the measurement is made at the center of the symbol with no window time-width.
17. Systematic Jitter contributed by the receiver is defined as the combination of Duty Cycle Distortion and Data Dependent Jitter. The input optical power level is at the maximum of "P_{IN} Min. (W)." Systematic Jitter is measured at 50% threshold using a 155.52 MBd (77.5 MHz square-wave), $2^7 - 1$ pseudo-random bit stream data pattern input signal.
18. Random Jitter contributed by the receiver is specified with a 155.52 MBd (77.5 MHz square-wave) input signal.
19. This value is measured during the transition from low to high levels of input optical power.
20. This value is measured during the transition from high to low levels of input optical power.
21. The Signal Detect output shall be asserted, logic-high (V_{OH}), within 100 μs after a step increase of the Input Optical Power.
22. Signal Detect output shall be deasserted, logic-low (V_{OL}), within 350 μs after a step decrease in the Input Optical Power.
23. The HFBR-1116TZ transmitter complies with the requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 9. This figure is derived from the FDDI PMD standard (ISO/IEC 9314-3: 1990 and ANSI X3.166 - 1990) per the description in ANSI T1E1.2 Revision 3. The interpretation of this figure is that values of Center Wavelength and Spectral Width must lie along the appropriate Optical Rise/Fall Time curve.
24. This value is measured with an output load $R_L = 10 k\Omega$.

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