HFC0511

Fixed-Frequency Flyback Controller with Ultra-Low, No-Load Power Consumption

DESCRIPTION

The HFC0511 is a fixed-frequency, current-mode controller with internal slope compensation specifically designed for medium-power, offline, flyback, switch-mode power supplies. The HFC0511 is a highly efficient green-mode controller. At light loads, the controller freezes the peak current and reduces its switching frequency down to 27kHz to achieve excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve very low standby power consumption.

The HFC0511 offers frequency jittering to help dissipate energy generated by the conducted noise.

The HFC0511 employs an over-power compensation function to narrow the difference of the over-power protection point between the low line and high line.

The HFC0511 also has an X-cap discharge function to discharge the X-capacitor when the input is unplugged. This helps lower the power at no load.

Full protection features include thermal shutdown, VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

The HFC0511 is available in a SOIC8-7A package.

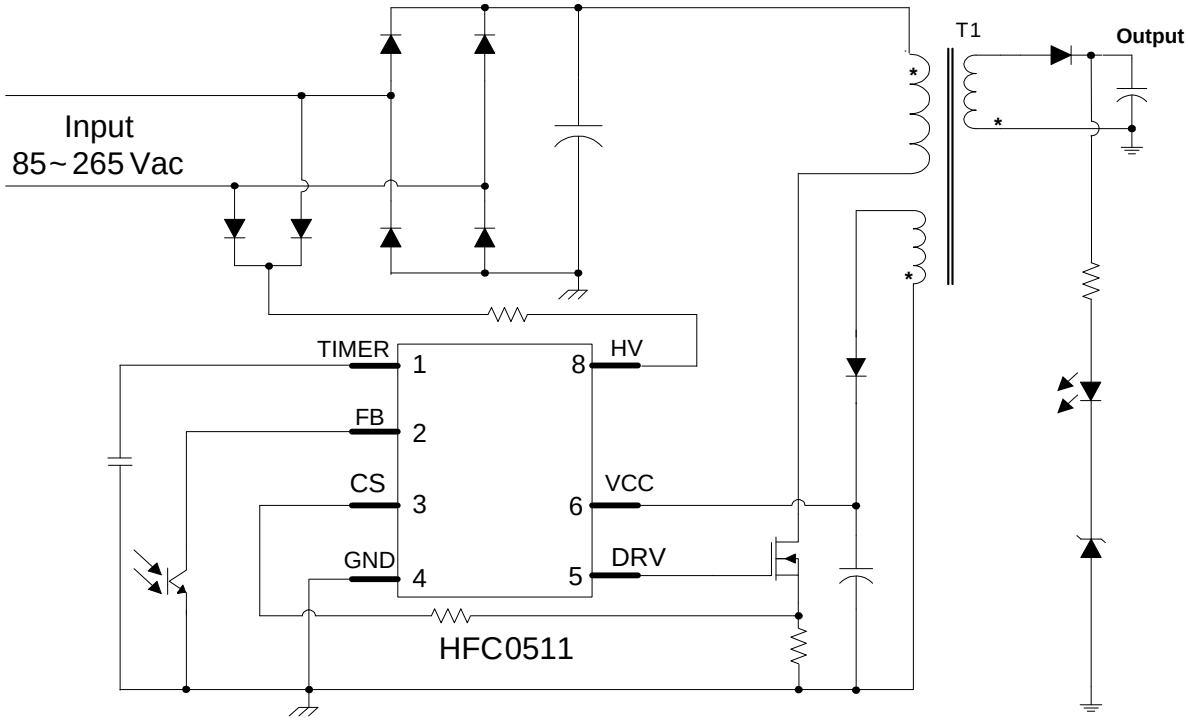
FEATURES

- Fixed-Frequency, Current-Mode Control with Internal Slope Compensation
- Frequency Foldback down to 27kHz at Light Load
- Burst Mode for Low Standby Power Consumption, Meeting EuP Lot 6
- Frequency Jitter to Reduce EMI Signature
- X-Cap Discharge Function
- Adjustable Over-Power Compensation
- Internal High-Voltage Current Source
- VCC Under-Voltage Lockout (UVLO) with Hysteresis
- Brown-Out Protection on HV
- Overload Protection with Programmable Delay
- Thermal Shutdown (Auto-Restart with Hysteresis)
- Latch-Off for External Over-Voltage Protection (OVP) and Over-Temperature Protection (OTP) on TIMER
- Latch-Off for VCC Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP)
- Programmable Soft Start (SS)
- Available in a SOIC8-7A Package

APPLICATIONS

- AC/DC Power for Small and Large Appliances
- AC/DC Adapters for Notebook Computers, Tablets, and Smart Phones
- Offline Battery Chargers
- LCD TVs and Monitors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
HFC0511GS	SOIC8-7A	*See Below*

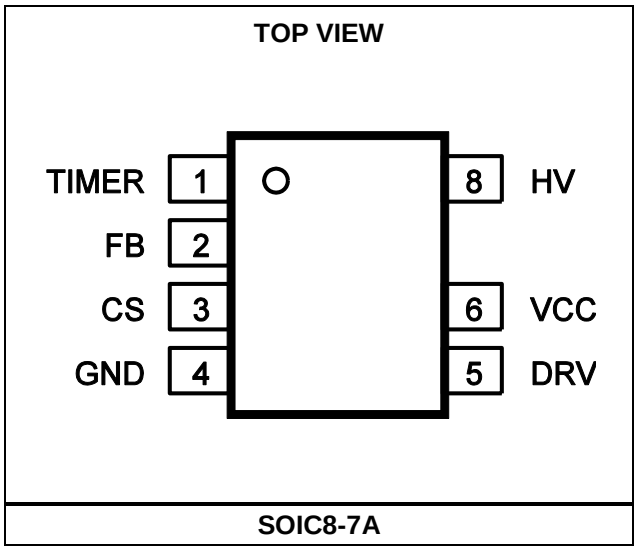
* For Tape & Reel, add suffix –Z (e.g. HFC0511GS–Z)

TOP MARKING

HFC0511
LLLLLLLL
MPSYWW

HFC0511: First seven digits of the part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

HV ..... -0.7V to 700V
VCC, DRV to GND..... -0.3V to 30V
FB, TIMER, CS to GND ..... -0.3V to 7V
Continuous power dissipation (T_A = +25°C) (2) 1.3W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -60°C to +150°C
ESD capability human body model (except HV and DRV) 4.0kV
ESD capability human body model (DRV) 3.5kV
ESD capability human body model (HV) ...1.0kV
ESD capability for machine mode 400V

Recommended Operation Conditions (3)

Operating junction temp. (T_J) ... -40°C to +125°C
Operating VCC range ..... 9V to 24V

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8-7A..... 96..... 45 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERICS

VCC = 18V, T_J = -40°C ~ 125°C, min and max values are guaranteed by characterization, typical value is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source (HV)						
Supply current from HV	I_{HV_400}	VCC = 12V, V_{HV} = 400V	1.5	2.8	3.9	mA
	I_{HV_120}	VCC = 12V, V_{HV} = 120V	1.5	2.7	3.7	
Leakage current from HV	I_{LK_400}	VCC increases to 18V, then decreases to 14V, V_{HV} = 400V	1	16	28	µA
	I_{LK_200}	VCC increases to 18V, then decreases to 14V, V_{HV} = 200V	1	13	25	µA
Break-down voltage	V_{BR}	T_J = 25°C	700	790		V
Supply Voltage Management (VCC)						
VCC increasing level at which the current source turns off	VCC_{OFF}		12.5	15.5	18	V
VCC decreasing level above which soft start takes place if HV > HV_{ON}	VCC_{SS}		10.5	12	13	V
VCC hysteresis for brown-in detection	VCC_{OFF} - VCC_{SS}		1.35	3.5		V
VCC decreasing level at which the current source turns on	VCC_{ON}		7.3	8.5	9.6	V
VCC UVLO hysteresis	VCC_{OFF} - VCC_{ON}		5	7		V
VCC recharge level when protection takes place	VCC_{PRO}		4.9	5.5	6.2	V
VCC decreasing level at which the latch-off phase ends	VCC_{LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 2V, C_L = 1nF, VCC = 12V	0.9	1.8	2.7	mA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC = VCC_{OFF} - 1V, T_J = 25°C	520	700	880	µA
Voltage on the VCC above which the controller latches off (OVP)	V_{OVP}		24	26.5	28.5	V
Blanking duration on the OVP comparator	T_{OVP}			60		µs
Brown-Out						
HV turn-on threshold voltage	HV_{ON}	V_{HV} going up, T_J = 25°C	95	107	119	V
HV turn-off threshold voltage	HV_{OFF}	V_{HV} going down, T_J = 25°C	86	97	110	V
Brown-out hysteresis	ΔHV	T_J = 25°C	6.5	10	13.5	V
Timer duration for line cycle dropout	T_{HV}	C_{TIMER} = 47nF	40			ms
Oscillator						
Oscillator frequency	f_{OSC}	V_{FB} > 1.85V, T_J = 25°C	125	130	135	kHz
Frequency jittering amplitude, in percentage of f_{OSC}	A_{jitter}	V_{FB} > 1.85V, T_J = 25°C	±5	±6.5	±8.3	%
Frequency jittering entry level	V_{FB_JITTER}				1.95	V
Frequency jittering modulation period	T_{jitter}	C_{TIMER} = 47nF		3.7		ms

ELECTRICAL CHARACTERICS *(continued)*

VCC = 18V, T_J = -40°C ~ 125°C, min and max values are guaranteed by characterization, typical value is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense						
Current-limit point	V_{ILIM}		0.93	1	1.07	V
Short-circuit protection point	V_{SCP}		1.3	1.47	1.63	V
Current limitation when frequency folds back	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limitation when entering burst	V_{IBURL}	V_{FB} = 0.7V		0.11		V
Current limitation when leaving burst	V_{IBURH}	V_{FB} = 0.8V		0.15		V
Leading edge blanking for V_{ILIM}	T_{LEB1}			350		ns
Leading edge blanking for V_{SCP}	T_{LEB2}			270		ns
Slope of the compensation ramp	S_{RAMP}		18	25	32	mV/µs
Feedback (FB)						
Internal pull-up resistor	R_{FB}		11.5	14	17	kΩ
Internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current set point division ratio	K_{FB1}	V_{FB} = 2V	2.55	2.8	3.05	--
V_{FB} to internal current set point division ratio	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	--
FB decreasing level at which the controller enters burst mode	V_{BURL}		0.63	0.7	0.77	V
FB increasing level at which the controller leaves burst mode	V_{BURH}		0.72	0.8	0.88	V
Overload Protection (OLP)						
FB level at which the controller enters the OLP after a dedicated time	V_{OLP}			3.7		V
Time duration before OLP when FB reaches protection point	T_{OLP}	C_{TIMER} = 47nF	40			ms
Over-Power Compensation						
V_{HV} to I_{OPC} ratio	K_{OPC}			0.45		µA/V
Current out of CS	I_{OPC}	V_{HV} = 120V, V_{FB} = 2.5V		0		µA
		V_{HV} = 155V, V_{FB} = 2.5V		13		
		V_{HV} = 310V, V_{FB} = 2.5V		85		
		V_{HV} = 380V, V_{FB} = 2.5V, T_J = 25°C	80	109	138	
FB voltage below which compensation is removed	$V_{OPC(OFF)}$		0.55			V
FB voltage above which compensation is applied fully	$V_{OPC(ON)}$				2.2	V
Frequency Foldback						
FB voltage threshold below which frequency foldback starts	$V_{FB(FOLD)}$			1.8		V
Minimum switching frequency	$F_{OSC(min)}$	T_J = 25°C	21	27	33	kHz
FB voltage threshold below which frequency foldback ends	$V_{FB(FOLDE)}$			1.0		V

ELECTRICAL CHARACTERICS *(continued)*

VCC = 18V, T_J = -40°C ~ 125°C, min and max values are guaranteed by characterization, typical value is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch-Off Input (Integration in TIMER)						
Threshold below which controller is latched	$V_{TIMER(LATCH)}$		0.7	1	1.3	V
Blanking duration on latch detection	T_{LATCH}			12		µs
DRV Voltage						
Driver voltage high level	V_{High}	C_L = 1nF, VCC = 12V		10.3		V
Driver voltage clamp level	V_{Clamp}	C_L = 1nF, VCC = 24V		13.4		V
Driver voltage low level	V_{Low}	C_L = 1nF, VCC = 24V		16		mV
Driver voltage rise time	T_R	C_L = 1nF, VCC = 16V		13		ns
Driver voltage fall time	T_F	C_L = 1nF, VCC = 16V		23		ns
Driver pull-up resistance	$R_{Pull-up}$	C_L = 1nF, VCC = 16V		8		Ω
Driver pull-down resistance	$R_{Pull-down}$	C_L = 1nF, VCC = 16V		10		Ω
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown hysteresis (5)				25		°C

NOTE:

5) This parameter is guaranteed by design.

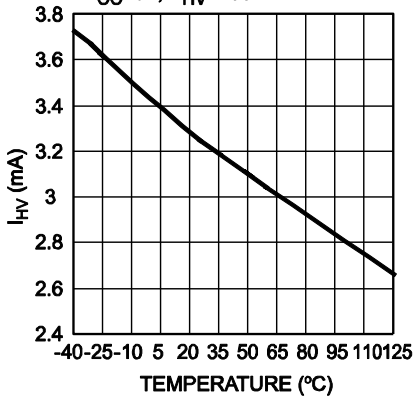
PIN FUNCTIONS

Pin #	Name	Description
1	TIMER	**Timer.** TIMER combines soft start, frequency jittering, and timer functions for overload protection (OLP), brown-out protection, and X-cap discharging. The HFC0511 can be latched off by pulling TIMER low.
2	FB	**Feedback.** Use a pull-down optocoupler to control the output regulation.
3	CS	**Current sense.** CS senses the primary-side current for current-mode operation and provides a mean for over-power compensation adjustment.
4	GND	**IC ground.**
5	DRV	**Drive signal output.**
6	VCC	**Power supply.**
8	HV	**High-voltage current source.** HV includes brown-out and X-cap discharge functions.

TYPICAL CHARACTERISTICS

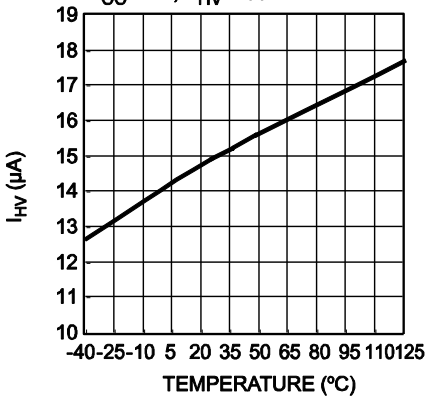
Supply Current from HV vs. Temperature

V_{CC}=6V, V_{HV}=400V

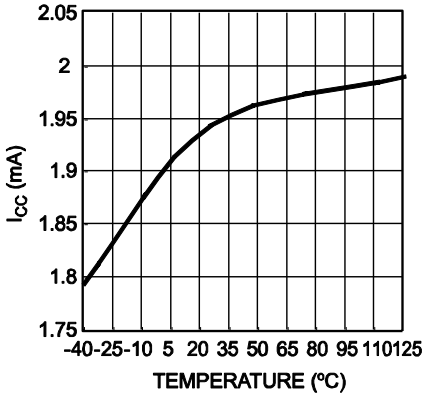


Leakage Current from HV vs. Temperature

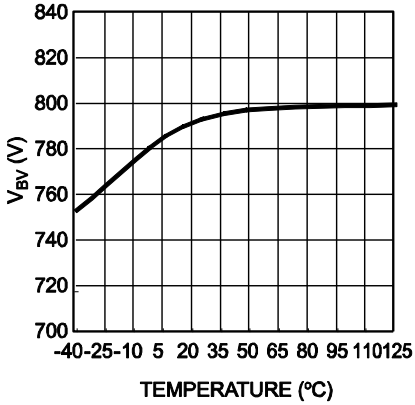
V_{CC}=14V, V_{HV}=400V



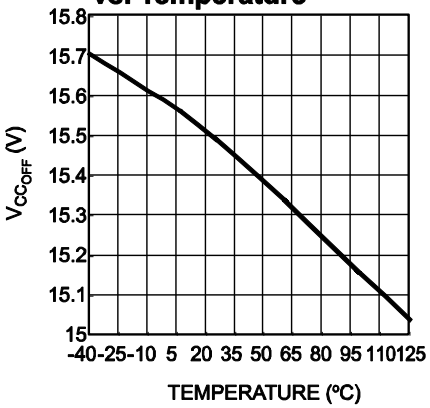
Internal IC Consumption vs. Temperature



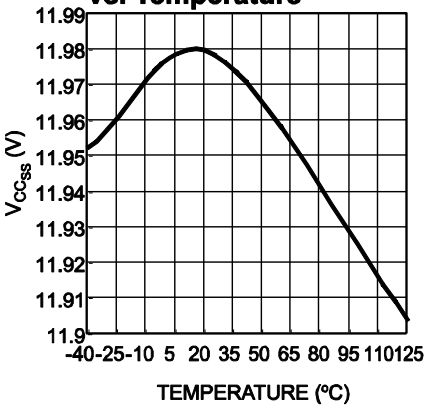
Break-Down Voltage vs. Temperature



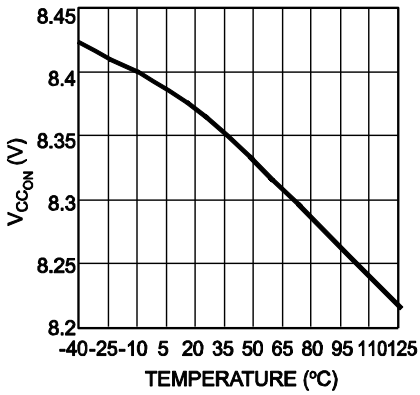
VCC Curent-Source Turn-Off Level, Rising vs. Temperature



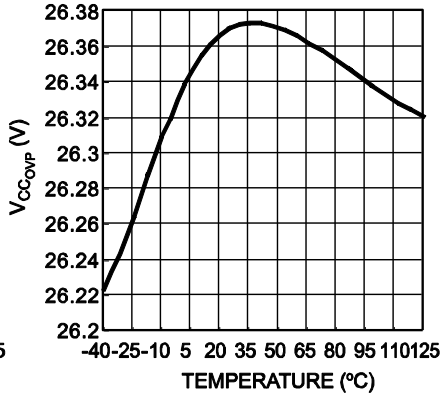
VCC Threshold for HV Turn-On Detection, Falling vs. Temperature



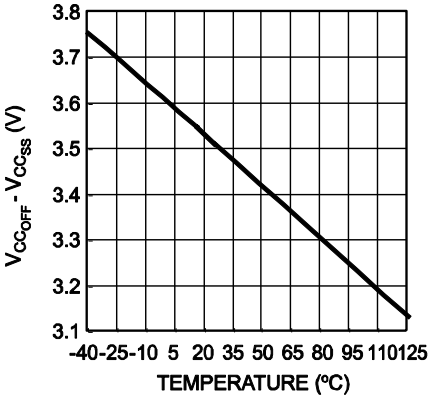
VCC Current Source Turn-On Level, Falling vs. Temperature



Voltage above VCC where the Controller Latchs Off (OVP) vs. Temperature

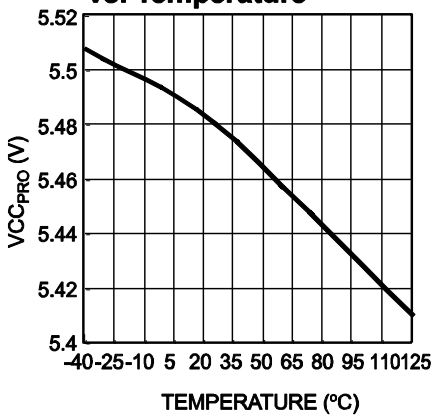


VCC Hysteresis for HV Turn-On Detection vs. Temperature

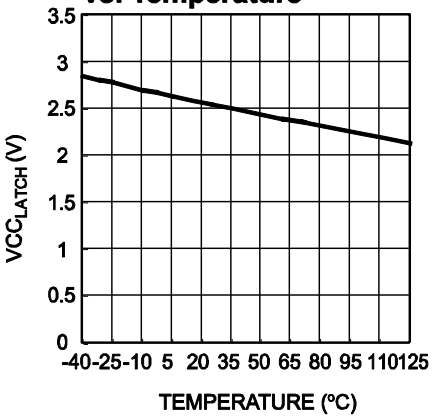


TYPICAL CHARACTERISTICS *(continued)*

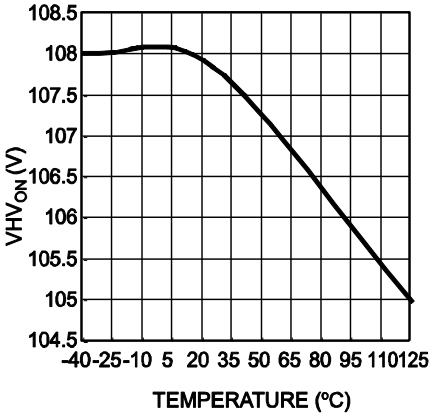
VCC Recharge Level where Protection Occurs vs. Temperature



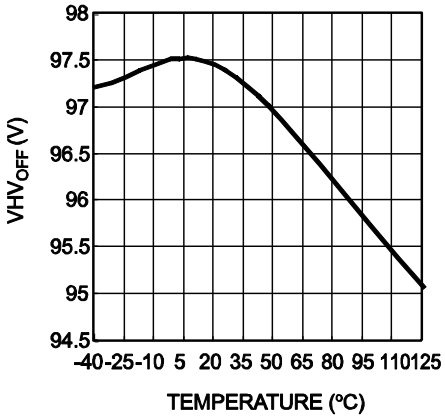
VCC Decreasing Level when Latch-Off Phase Ends vs. Temperature



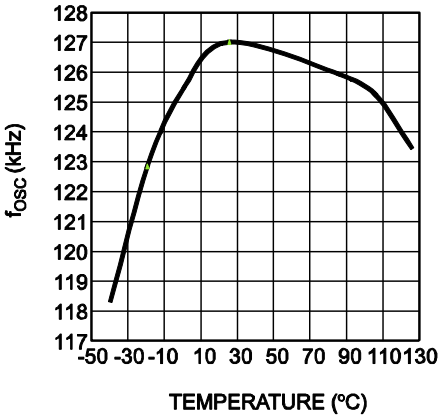
HV Turn-On Threshold vs. Temperature



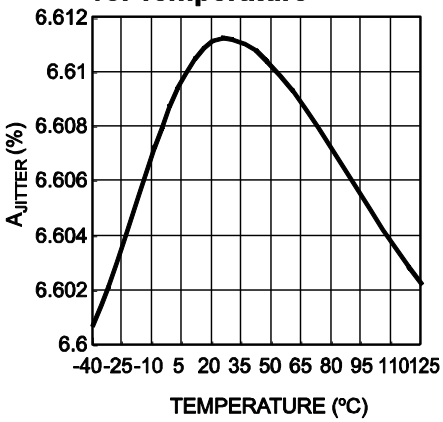
HV Turn-Off Threshold vs. Temperature



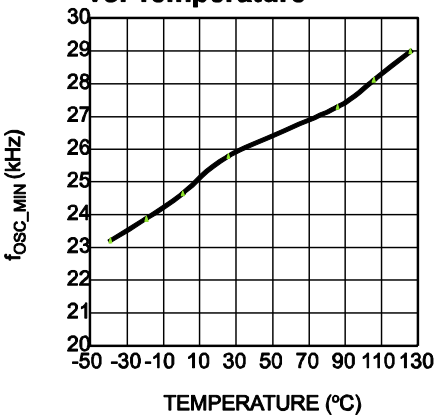
Oscillator Frequency vs. Temperature



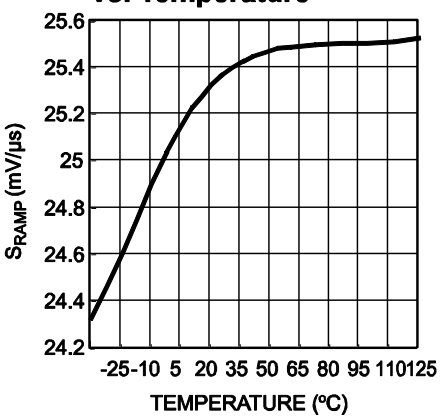
Frequency Jitter Amplitude in Percentage of f_{OSC} vs. Temperature



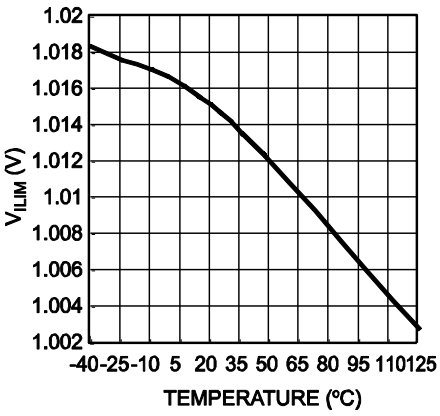
Minimum Switching Frequency vs. Temperature



Slope of the Compensation Ramp vs. Temperature

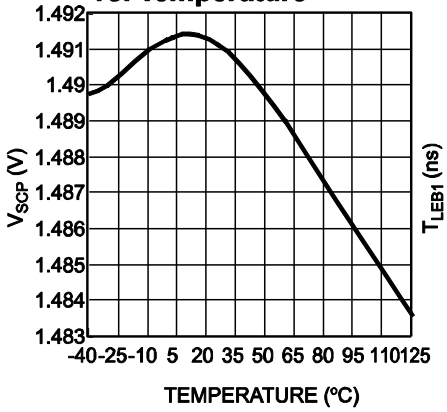


Current Limit vs. Temperature

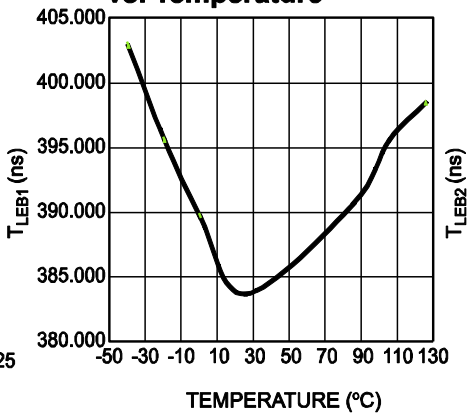


TYPICAL CHARACTERISTICS *(continued)*

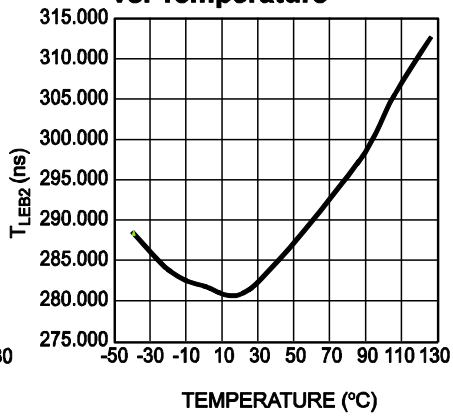
Short-Circuit Protection Level vs. Temperature



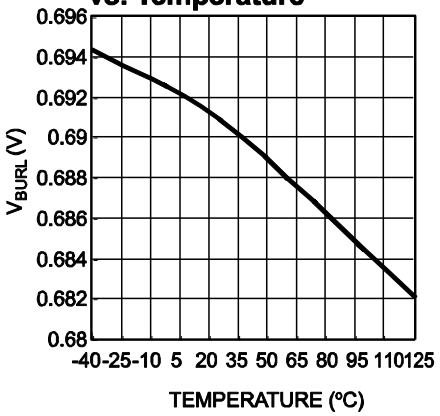
Leading Edge Blanking for V_{ILIM} vs. Temperature



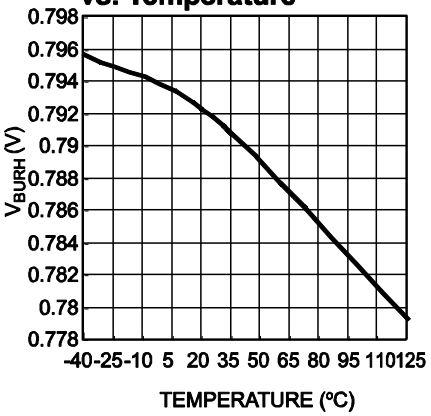
Leading Edge Blanking for V_{SCP} vs. Temperature



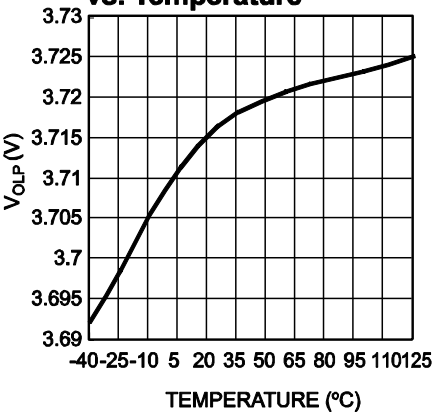
FB Level (Falling) at which Controller Enters Burst Mode vs. Temperature



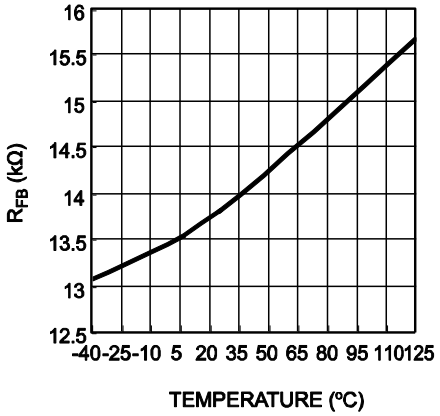
FB Level (Rising) at which Controller Exits Burst Mode vs. Temperature



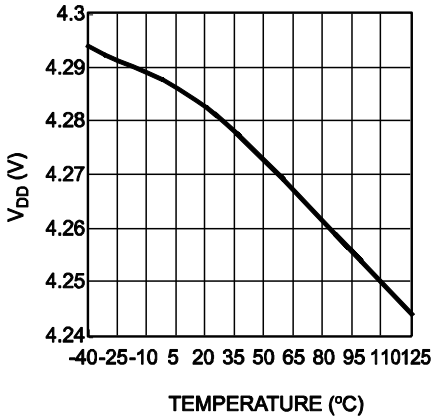
FB Level at which Controller Enters OLP after Blanking Time vs. Temperature



FB Internal Pull-Up Resistor vs. Temperature



FB Internal Pull-Up Voltage vs. Temperature

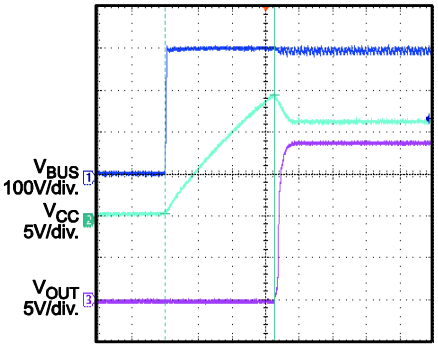


TYPICAL PERFORMANCE CHARACTERISICS

V_{IN} = 230V_{AC}, V_{OUT} = 19V, I_{OUT} = 2.35A, unless otherwise noted.

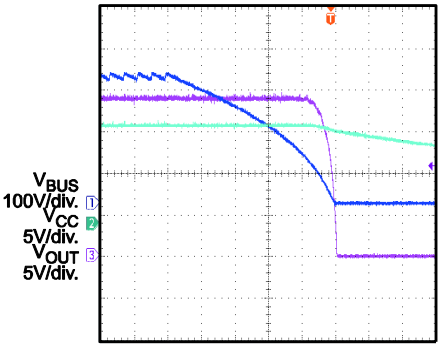
Input Power Start-Up

230V_{AC} Full Load

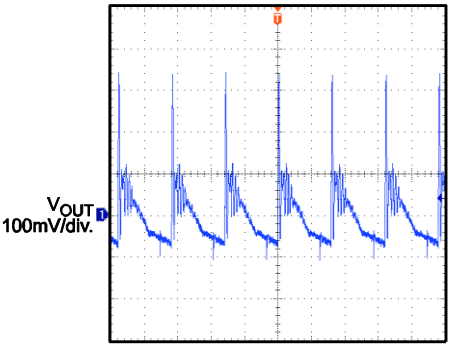


Input Power Shutdown

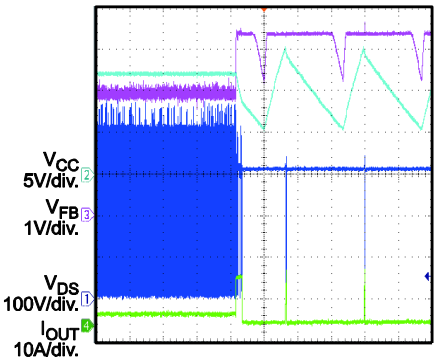
230V_{AC} Full Load



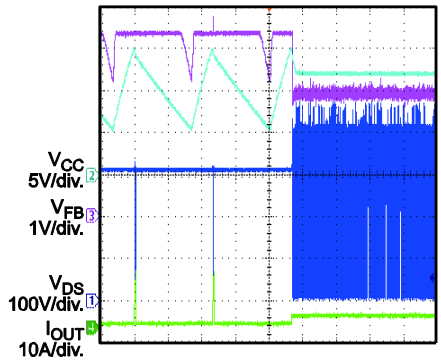
Output Ripple



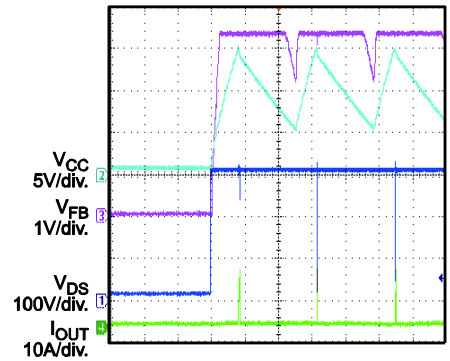
SCP Entry



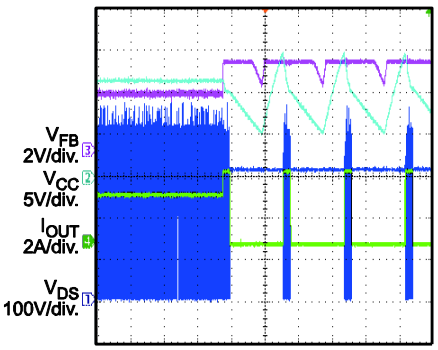
SCP Recovery



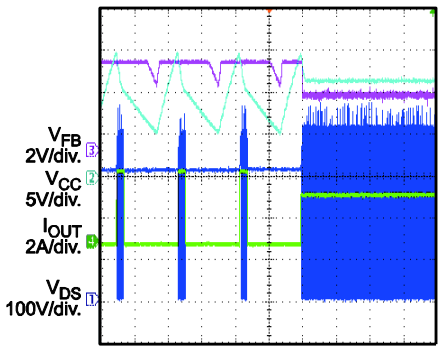
SCP Power-On



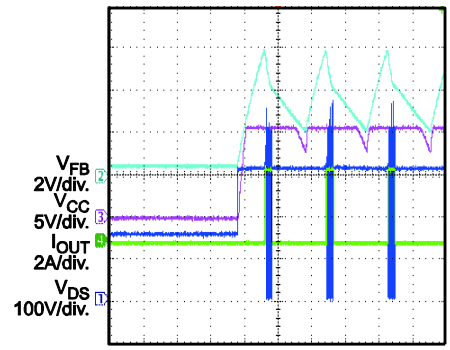
OLP Entry



OLP Recovery



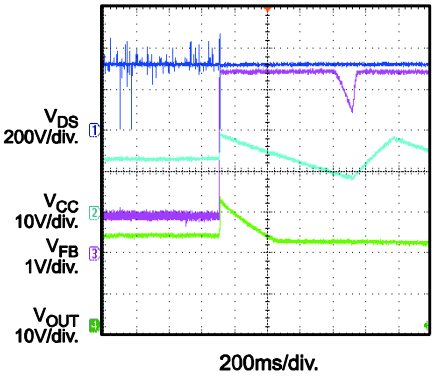
OLP Power-On



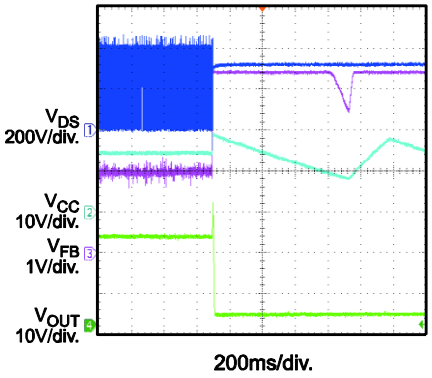
TYPICAL PERFORMANCE CHARACTERISICS *(continued)*

V_{IN} = 230V_{AC}, V_{OUT} = 19V, I_{OUT} = 2.35A, T_A = 25°C, unless otherwise noted.

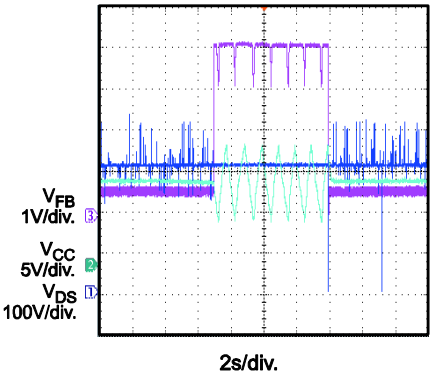
OVP
No Load



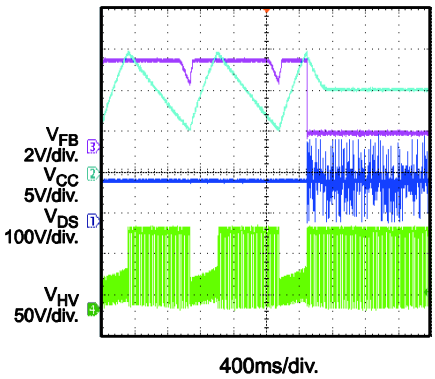
OVP
Full Load



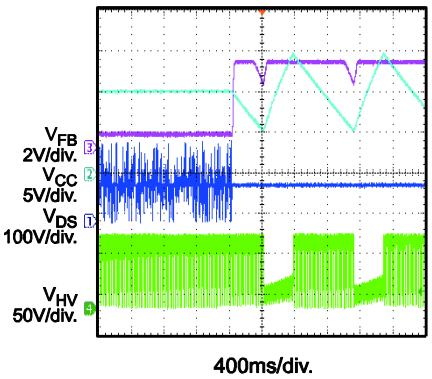
OTP
No Load



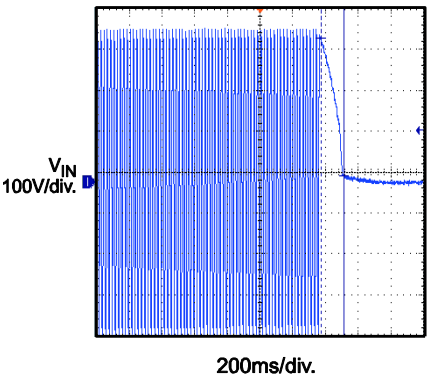
Brown-In



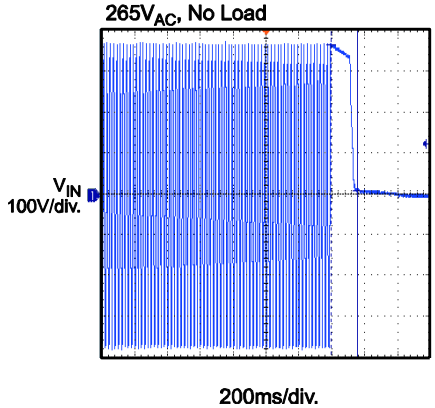
Brown-Out



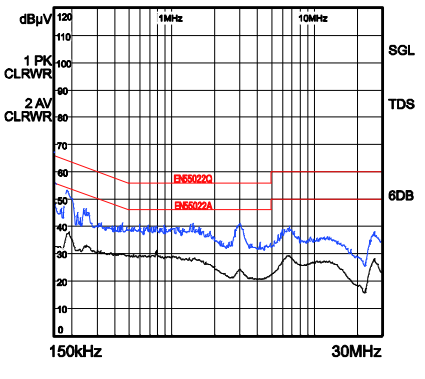
X-Cap Discharge
265V_{AC}, Full Load



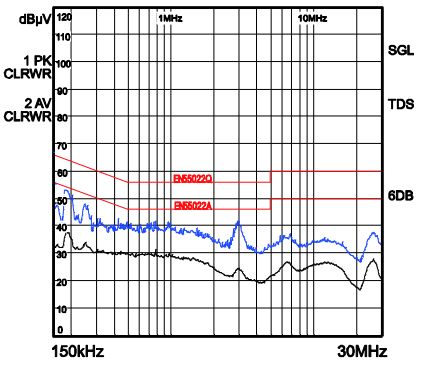
X-Cap Discharge
265V_{AC}, No Load



Conducted EMI
230V_{AC}, L Wire



Conducted EMI
230V_{AC}, N Wire



BLOCK DIAGRAM

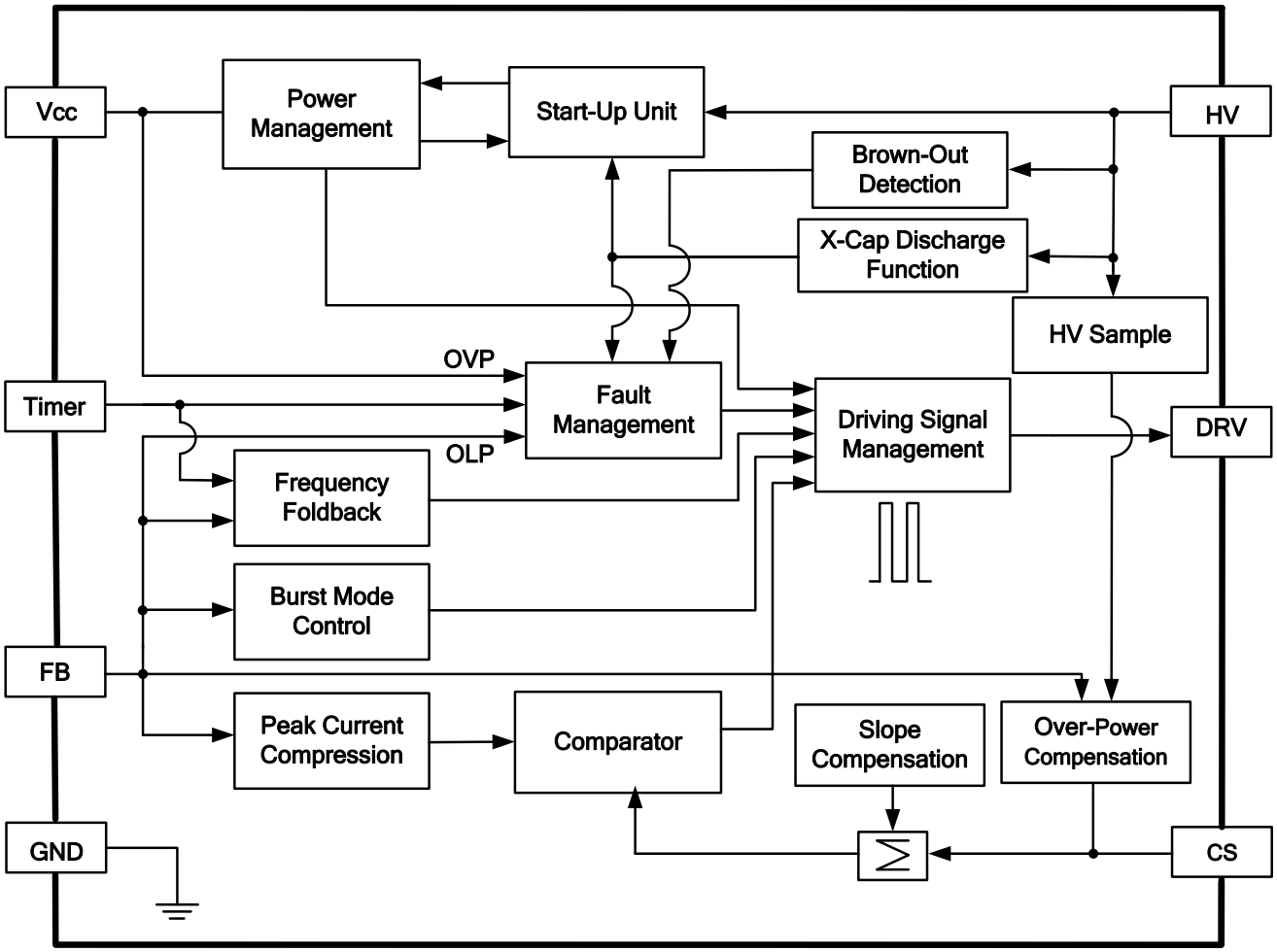


Figure 1: Functional Block Diagram

OPERATION

The HFC0511 incorporates all necessary features for building a reliable switch-mode power supply. The HFC0511 is a fixed-frequency, current-mode controller with internal slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 27kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. The HFC0511 also has excellent EMI performance due to frequency jittering. The HFC0511's high level of integration requires very few external components.

Fixed Frequency with Jitter

Frequency jitter reduces EMI by spreading the energy over the jitter frequency range. Figure 2 shows the circuit of the frequency jittering.

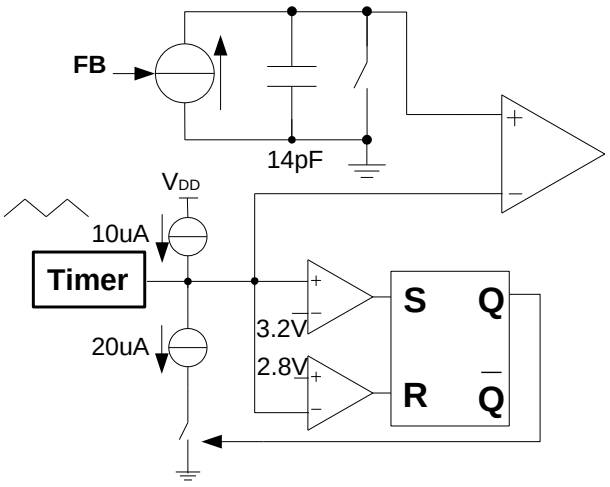


Figure 2: Frequency Jitter Circuit

A controlled current sourced (fixed at 2.72μA when V_{FB} = 2V) charges the internal C_{OSC} capacitor. Comparing the capacitor voltage to the TIMER voltage determines the switching frequency. Frequency jitter is accomplished by varying V_{TIMER} between 3.2V and 2.8V (see Figure 3). Determine T_{jitter} with Equation (1):

$$T_{jitter} = 2 \cdot \frac{C_{TIMER} \cdot (3.2V - 2.8V)}{10\mu A} \quad (1)$$

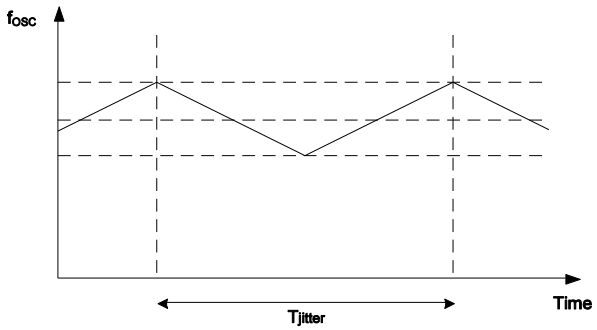


Figure 3: Frequency Jitter

Frequency Foldback

The HFC0511 implements frequency foldback at light load to improve overall efficiency.

When the load decreases to a given level (1.0V < V_{FB} < 1.8V), the controller freezes the peak current (as measured on CS, typically 0.7V) while reducing its switching frequency to 27kHz. This reduces switching loss. If the load continues to decrease, the peak current decreases with 27kHz of fixed frequency to avoid audible noise. Figure 4 shows the frequency vs. V_{FB} and peak current (V_{CS}) vs. V_{FB}.

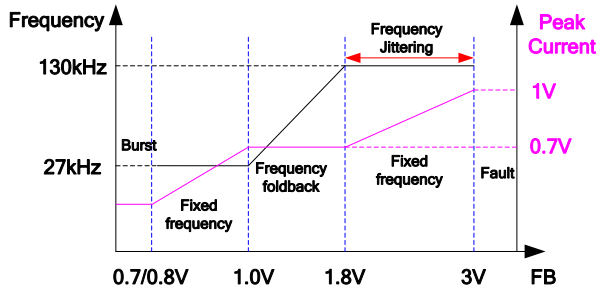


Figure 4: Frequency and Peak Current (V_{CS}) vs. V_{FB}

Current-Mode Operation with Slope Compensation

The feedback voltage (V_{FB}) controls the primary peak current. When the peak current reaches the level determined by V_{FB}, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because of its internal slope compensation (typically 25mV/μs), avoiding sub-harmonic oscillations above a 50% duty cycle.

High Voltage Start-Up Current Source with Brown-Out Detection

At start-up, the internal high-voltage current source from HV supplies the IC. The IC turns off the current source once VCC reaches VCC_{OFF} (typically 15.5V) and detects the voltage on HV. Once the HV voltage exceeds HV_{ON} before VCC drops down to VCC_{SS} (typically 12V), the controller begins switching. If the HV voltage does not exceed VH_{ON}, the system treats this as a brown-out and latches DRV low. When VCC drops to VCC_{PRO} (typically 5.5V), the high-voltage current source turns on to recharge VCC. The auxiliary transformer winding supplies the IC after the controller starts switching. If VCC falls below VCC_{ON} (typically 8.5V), the switching pulse stops, and the current source turns on again. Figure 5 shows the typical VCC under-voltage lockout (UVLO) waveform.

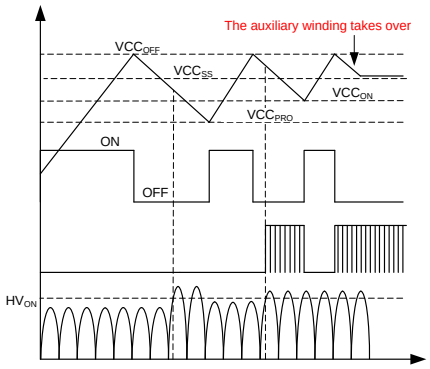


Figure 5: VCC Under-Voltage Lockout

The VCC lower threshold UVLO drops from VCC_{ON} to VCC_{PRO} under fault conditions such as overload protection (OLP), short-circuit protection (SCP), brown-out, and over-temperature protection (OTP).

Soft Start (SS)

Soft start is externally programmable with a capacitor on TIMER. As this capacitor charges from 1V to 1.75V with 1/4 of the normal charge current, the peak-current limit threshold increases gradually from 0.25V to 1V while increasing the switching frequency gradually. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the start-up duration as shown in Equation (2):

$$T_{Soft-start} = \frac{C_{TIMER} \cdot (1.75V - 1V)}{10/4\mu A} \quad (2)$$

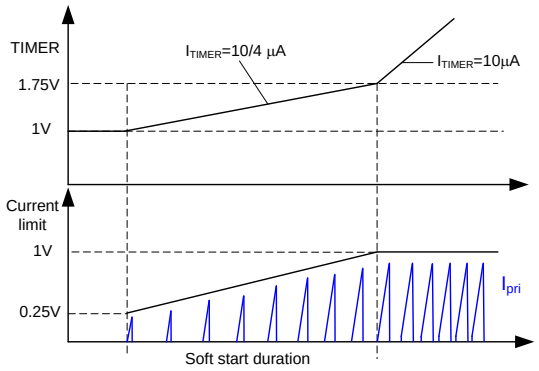


Figure 6: Soft Start

Burst Mode

To minimize power dissipation in no load or light load, the HFC0511 employs burst-mode operation. As the load decreases, V_{FB} decreases. The IC enters burst mode when V_{FB} drops below the lower threshold (V_{BURL}, typically 0.7V), stopping output switching. Then the output voltage starts to drop, which causes V_{FB} to increase again. Once V_{FB} exceeds V_{BURH} (typically 0.8V), switching resumes. Burst mode enables and disables MOSFET switching alternately, thereby reducing no-load or light-load switching losses.

Adjustable Over-Power Compensation

An offset current proportional to the input voltage is added to the current sense voltage. By choosing the value of the resistor to be in series with CS, the amount of compensation can be adjusted to the application for a more accurate output power limit at the total input range. Figure 7 and Figure 8 show the compensation current relation to FB and the peak voltage on HV respectively.

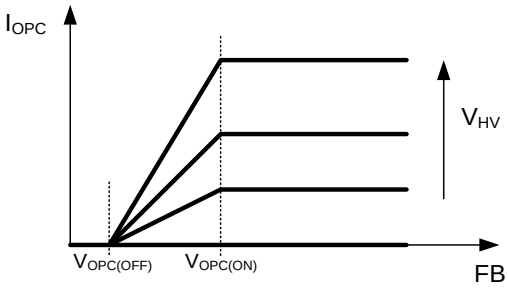


Figure 7: Compensation Current vs. FB and HV Voltage

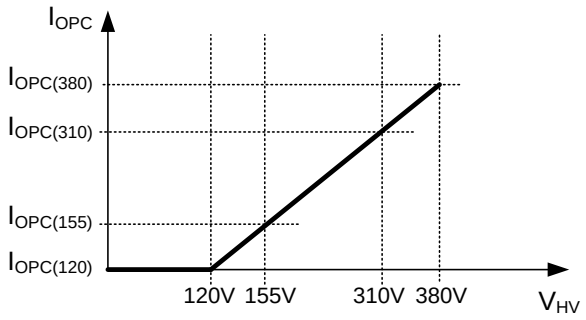


Figure 8: Compensation Current vs. Peak of Rectified Input Line AC Voltage

Timer-Based Overload Protection (OLP)

In a flyback converter, if the switching frequency is fixed, the maximum output power is limited by the peak current. The output voltage drops below the set value when the output power exceeds the power limit. This reduces the current through the optocoupler, pulling V_{FB} high.

When FB is higher than the OLP voltage (V_{OLP}) (typically 3.7V), which is considered to be an error flag, the timer begins counting. If the error flag is removed during the count, the timer resets. If the timer count reaches 17, OLP is triggered. This timer duration avoids triggering OLP during power supply start-up or short load transients. Figure 9 shows the OLP function.

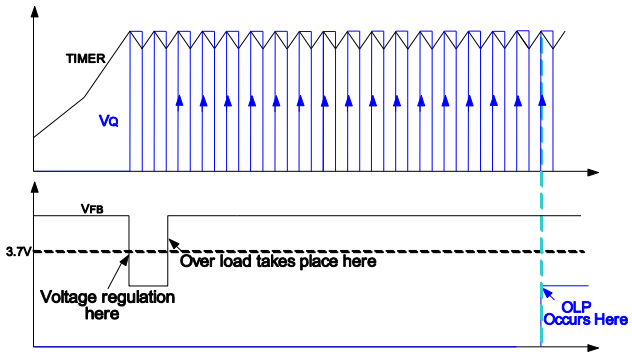


Figure 9: Overload Protection

Timer-Based Brown-Out Protection

The brown-out protection block is similar to the OLP block. When the HV voltage drops below HV_{OFF} (typically 97V), which is considered to be an error flag, the timer begins counting. Once the HV voltage is higher than HV_{OFF}, the timer resets. When the timer counts to 17, brown-out protection is triggered and switching stops.

Short-Circuit Protection (SCP)

The HFC0511 employs short-circuit protection (SCP) if V_{CS} reaches V_{SCP} (typically 1.47V) after a reduced leading-edge blanking time (T_{LEB2}). Once the fault disappears, the power supply resumes operation.

Thermal Shutdown

To prevent thermal damage, the HFC0511 stops switching when the temperature exceeds 150°C. Once the temperature drops below 125°C, the power supply resumes operation. During thermal shutdown, the VCC UVLO lower threshold drops from 8.5V to 5.5V.

VCC Over-Voltage Protection (OVP)

The HFC0511 enters a latched fault condition if VCC rises above V_{OVP} (typically 26.5V) for 60µs. The controller remains fully latched until VCC drops below VCC_{LATCH} (typically 2.5V), such as when the power supply is unplugged from the main input and is plugged in again. This situation usually occurs when the optocoupler fails, which results in the loss of output voltage regulation.

TIMER Latch-Off for OVP and OTP

Pulling TIMER below $V_{TIMER(LATCH)}$ (typically 1V) for 12µs can latch off the IC. This function can be used for external over-voltage protection (OVP) and OTP.

X-Cap Discharge Function

X-capacitors are typically positioned across a power supply's input terminals to filter differential mode EMI noise. These components pose a potential hazard since they can store unsafe levels of voltage energy after the AC line is disconnected. Generally, resistors in parallel with the X-caps provide a discharge path to meet safety standards, but these discharge resistors produce a constant loss while the AC is connected and contribute to no-load and standby input power consumption.

HV acts as a smart X-cap discharger. When AC voltage is applied, the internal high-voltage current source turns off to block HV current, and the IC monitors the HV voltage. When removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap energy. The first discharge duration is 16 cycles. After the first discharge, the IC turns off the current source for 16 cycles to detect whether the input is plugged into the AC line again. If the AC input remains disconnected, the IC turns on the current source for 48 cycles to discharge again, and then turn off for 16 cycles to detect repeatedly until the voltage on the X-cap drops to VCC. Once the reconnected AC input is detected, the high-voltage current source remains off until VCC drops to VCC_{PRO} (5.3V), and then restarts the system by recharging VCC. Figure 10 shows the discharge function waveforms.

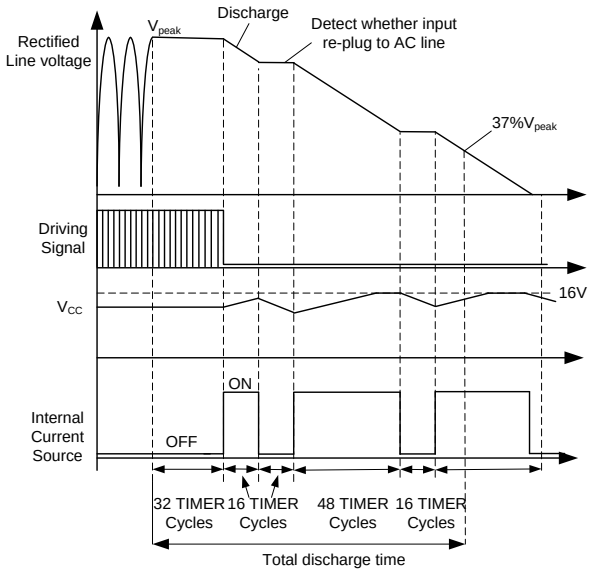


Figure 10: X-Cap Discharger

This approach provides an intelligent discharge path for the X-cap, eliminating power loss from the external discharge resistors.

Clamped Driver

DRV is clamped at V_{Clamp} (typically 13.4V) when VCC exceeds 16V, allowing for the use of any standard MOSFET.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS and the current comparator input to prevent premature switching pulse termination due to parasitic capacitances (see Figure 11). During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET.

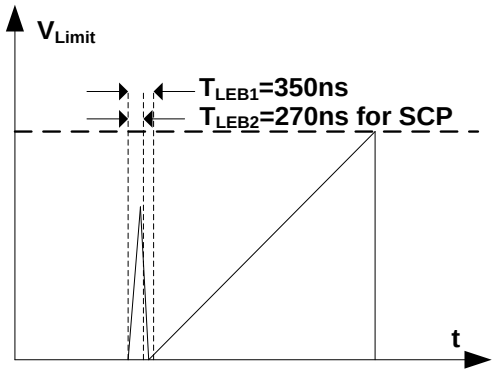


Figure 11: Leading-Edge Blanking

APPLICATION INFORMATION

VCC Capacitor Selection

Figure 12 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time. A larger R1 or C1 increases the start-up delay.

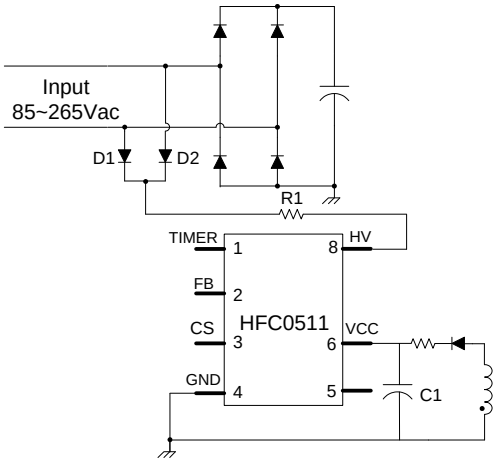


Figure 12: Start-Up Circuit

The VCC duration (from VCC_{OFF} to VCC_{SS}) for brown-out detection should exceed half of the input period. Estimate a value for the VCC capacitor with Equation (3):

$$C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot T_{input}}{VCC_{OFF} - VCC_{SS}} \quad (3)$$

Where $I_{CC(noswitch)}$ is the internal consumption (close to $I_{CClatch}$), and T_{input} is the period of the AC input. For most applications, choose a VCC capacitor value that exceeds 10μF.

A higher R1 value decreases the current of the internal high-voltage current source, especially at a low-input condition. Ensure that the practical supply current from HV is not smaller than the corresponding internal IC consumption current, which is the same as $I_{CCLATCH}$. For the universal input range, R1 should be smaller than 80kΩ. 20kΩ is generally recommended.

Primary-Side Inductor Design (L_m)

With internal slope compensation, the HFC0511 can support CCM when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude vs. the peak current value to $0 < K_P \leq 1$, where $K_P = 1$ for discontinuous conduction mode (DCM). Figure 13 shows the relevant waveforms.

A larger inductor leads to a smaller K_P, which can reduce RMS current, but increases transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for a $230V_{AC}$ input range.

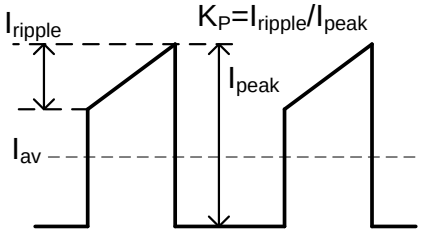


Figure 13: Typical Primary-Current Waveform

The input power (P_{in}) at the minimum input can be estimated with Equation (4):

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \quad (4)$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency, which is generally between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter duty cycle can be calculated with Equation (5):

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \quad (5)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turn ratio, and $V_{in(min)}$ is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time can be calculated with Equation (6):

$$T_{on} = D \cdot T_s \quad (6)$$

Where T_s is the switching period.

The average value of the primary current is calculated with Equation (7):

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \quad (7)$$

The peak value of the primary current is calculated with Equation (8):

$$I_{peak} = \frac{I_{av}}{\left(1-\frac{K_p}{2}\right)\cdot D} \quad (8)$$

The ripple value of the primary current is calculated with Equation (9):

$$I_{ripple} = K_P \cdot I_{peak} \quad (9)$$

The valley value of the primary current is calculated with Equation (10):

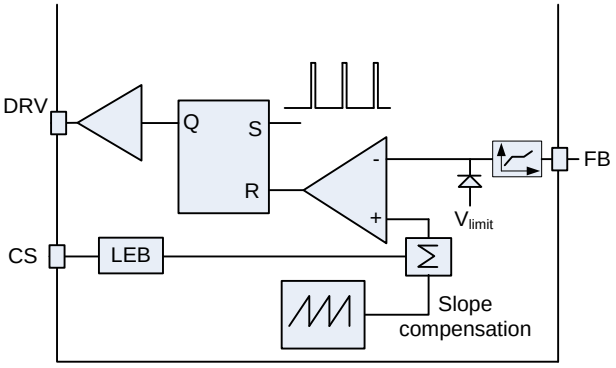
$$I_{valley} = (1-K_P)\cdot I_{peak} \quad (10)$$

L_m can be estimated with Equation (11):

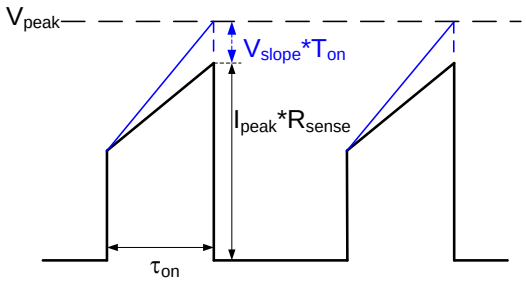
$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripples}} \quad (11)$$

Current-Sense Resistor

Figure 14 shows the peak-current comparator logic and the subsequent waveform.



Peak-Current Comparator Circuit



Typical Waveform

Figure 14: Peak-Current Comparator

When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes high to reset the RS flip-flop, and DRV is pulled down to turn off the MOSFET. The maximum current limit (V_{limit}, as measured by V_{CS}) is 0.95V. The slope compensator (V_{slope}) is ~25mV/µs. Given a certain margin, use 0.95xV_{limit} as V_{peak} at full load. Then the voltage on the sensing resistor can be obtained with Equation (12):

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot T_{on} \quad (12)$$

Then calculate the value of the sense resistor with Equation (13):

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (13)$$

Select the current sense resistor with an appropriate power rating. Then calculate the sense resistor power loss with Equation (14):

$$P_{sense} = \left[\left(\frac{I_{peak}+I_{valley}}{2}\right)^2 + \frac{1}{12}\left(I_{peak}-I_{valley}\right)^2\right]\cdot D \cdot R_{sense} \quad (14)$$

Low-Pass Filter on CS

A small capacitor connected to the CS with R_{series} forms a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 15).

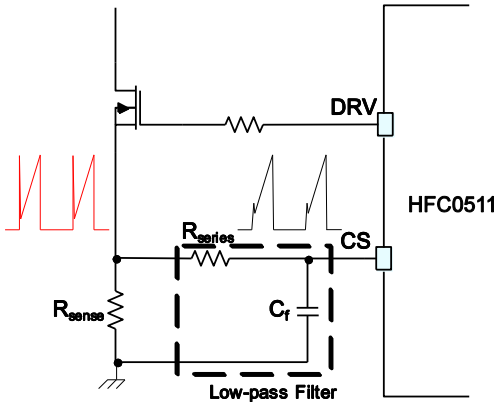


Figure 15: Low-Pass Filter on CS

The low-pass filter's RxC constant should not exceed 1/3 of the leading-edge blanking period for SCP (T_{LEB2}, typically 270ns), otherwise the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.

Over-Power Compensation (OPC)

The HFC0511 uses an over-power compensation function (OPC) by drawing current from CS. OPC minimizes the OLP difference caused by a different input voltage. The offset current is proportional to the input peak voltage sensed by HV.

Supposing that the resistor in the current sensing loop is R_{series}, and the input voltage is $220V_{AC}$, calculate the compensation voltage on CS with Equation (15):

$$V_{comp} = R_{series} \cdot I_{opc\_310V} \quad (15)$$

The compensation criterion is making the FB voltage under full-load condition similar whether in high line or low line.

Jitter Period

Frequency jitter is an effective method to reduce EMI by dissipating energy. The n^{th} order harmonic noise bandwidth is calculated with Equation (16):

$$B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter}) \quad (16)$$

Where Δf is the frequency jitter amplitude.

If B_{Tn} exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150kHz, 9kHz for noise frequency between 150kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on TIMER determines the period of the frequency jitter. A 10μA current source charges the capacitor. When the TIMER voltage reaches 3.2V, another 10μA current source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period in theory. A smaller f_{jitter} is more effective for EMI reduction. However, the measurement bandwidth requires that f_{jitter} be large compared to the spectrum analyzer RBW for effective EMI reduction. f_{jitter} should also be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. Simultaneously consider the practical application when selecting the TIMER capacitor. A capacitor that is too large may cause the start-up to fail at full load because of the long soft start-up duration shown in Equation (3). However, a TIMER capacitor that is too small causes the TIMER period to become smaller, so the TIMER count capability is overloaded, and some logic problems may occur. For most applications, a f_{jitter} value between 200Hz and 400Hz is recommended.

X-Cap Discharge Time

Figure 10 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input with no-load condition. The maximum discharge delay time is calculated with Equation (17):

$$T_{delay} = 32 \cdot T_{jitter} \quad (17)$$

The X-cap is discharged from a high-voltage constant current source (I_{HV_120V}, typically 2.5mA) into HV. The current-source discharge time for the X-cap to drop to 37% of the peak voltage can be estimated with Equation (18):

$$T_{discharge} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{ac(max)}}{I_{HV\_120V}} \quad (18)$$

Where C_X is the X-cap capacitance, and $V_{AC(max)}$ is the maximum AC input RMS value.

The first discharging period is $16xT_{jitter}$, with a subsequent period equal to $48xT_{jitter}$. Then the discharge sections times can be calculated approximately with Equation (19):

$$n = \frac{T_{discharge} - 16 \cdot T_{jitter}}{48 \cdot T_{jitter}} + 1 \quad (19)$$

For every discharge section, there is a certain period ($16xT_{jitter}$) for detection as shown in Equation (20):

$$T_{detect} = 16 \cdot T_{jitter} \cdot (n-1) \quad (20)$$

As a result, the total discharge time is determined with Equation (21):

$$T_{total} = T_{delay} + T_{discharge} + T_{detect} \quad (21)$$

The total discharge time is relative to T_{jitter}, which is dependent on C_{TIMER}. For example, if C_{TIMER} is 47nF, and T_{jitter} is 3.7ms, the X-cap discharge margin is 1s due to the X-cap value tolerance (±10% typically). It is recommended to select an X-cap less than 3.3μF.

Though the X-cap has been discharged, it may still retain a high voltage on the bulk capacitor. For safety, make sure it is released before debugging the board.

Ramp Compensation

When adopting peak current control, subharmonic oscillation occurs when D > 0.5 in CCM. The HFC0511 is equipped with internal ramp compensation to solve this problem. α is calculated with Equation (22):

$$\alpha = \frac{\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense} - m_a}{\frac{V_{in(min)}}{L_m} \cdot R_{sense} + m_a} \quad (22)$$

Where m_a = 18mV/μs is the minimum internal slope value of the compensation ramp, $\frac{V_{in(min)}}{L_m} \cdot R_{sense}$ is the slew rate of the primary-side sensed by the CS resistor, and $\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense}$ is the slew rate of the equivalent secondary-side voltage sensed by the CS resistor respectively. For stable operation, α must be less than 1.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 16 and follow the guidelines below.

1) Minimize the power stage loop area including the input loop (C1 - T1 - Q1 - R11/R12/R13 - C1), the auxiliary winding loop (T1 - D4 - R4 - C3 - T1), and the output loop (T1 - D6 - C10 - T1).
2) Keep the input loop GND and control circuit separate.
   Only connect them at C1.
3) Connect the Q1 heat sink to the primary GND plane to improve EMI.
4) Place the control circuit capacitors (such as those for FB, CS, and VCC) close to the IC to decouple noise.

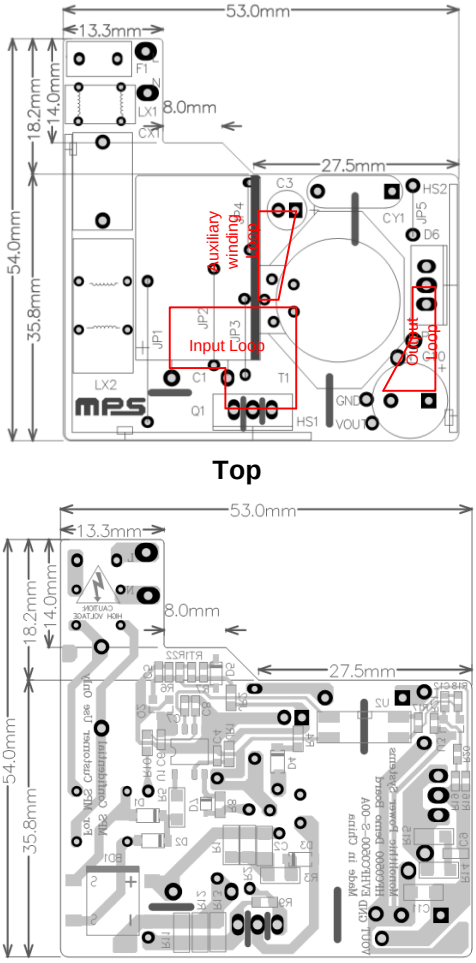


Figure 16: Recommended Layout

Design Example

Table 1 is a design example of the HFC0511 for power adapter applications.

Table 1: Design Example

V_{IN}	85 to 265V_{AC}
V_{OUT}	19V
I_{OUT}	2.35A

TYPICAL APPLICATION CIRCUIT

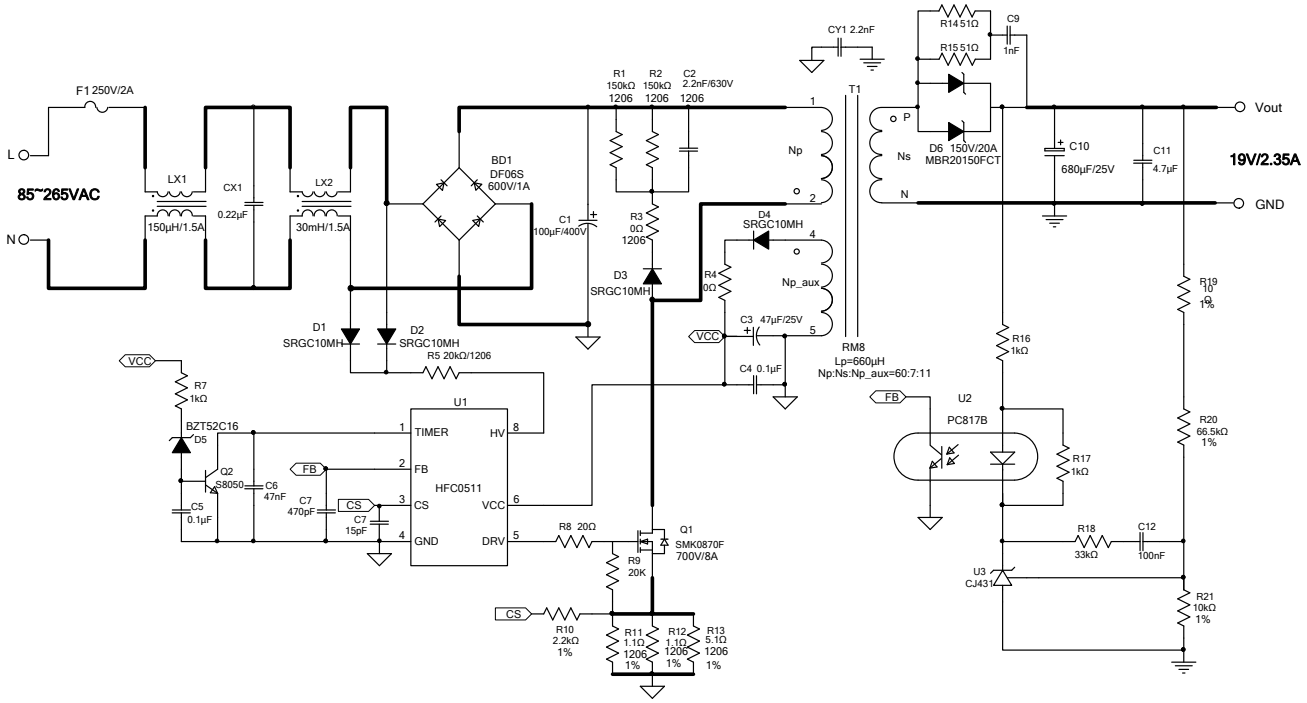
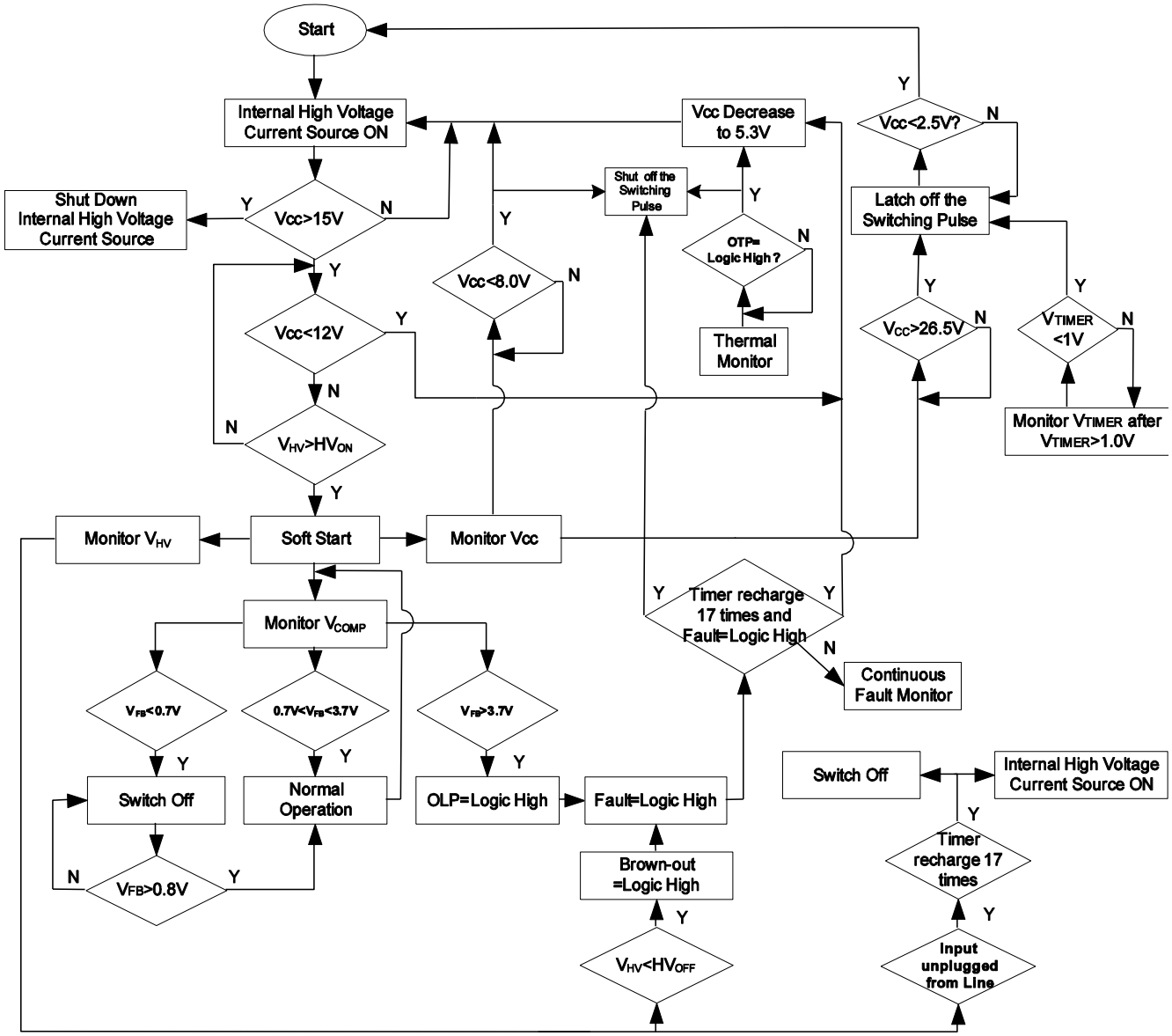


Figure 17: Typical Application

FLOW CHART



UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode

Release from the latch condition , need to unplug from the main input .

Figure 18: Control Flow Chart

EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

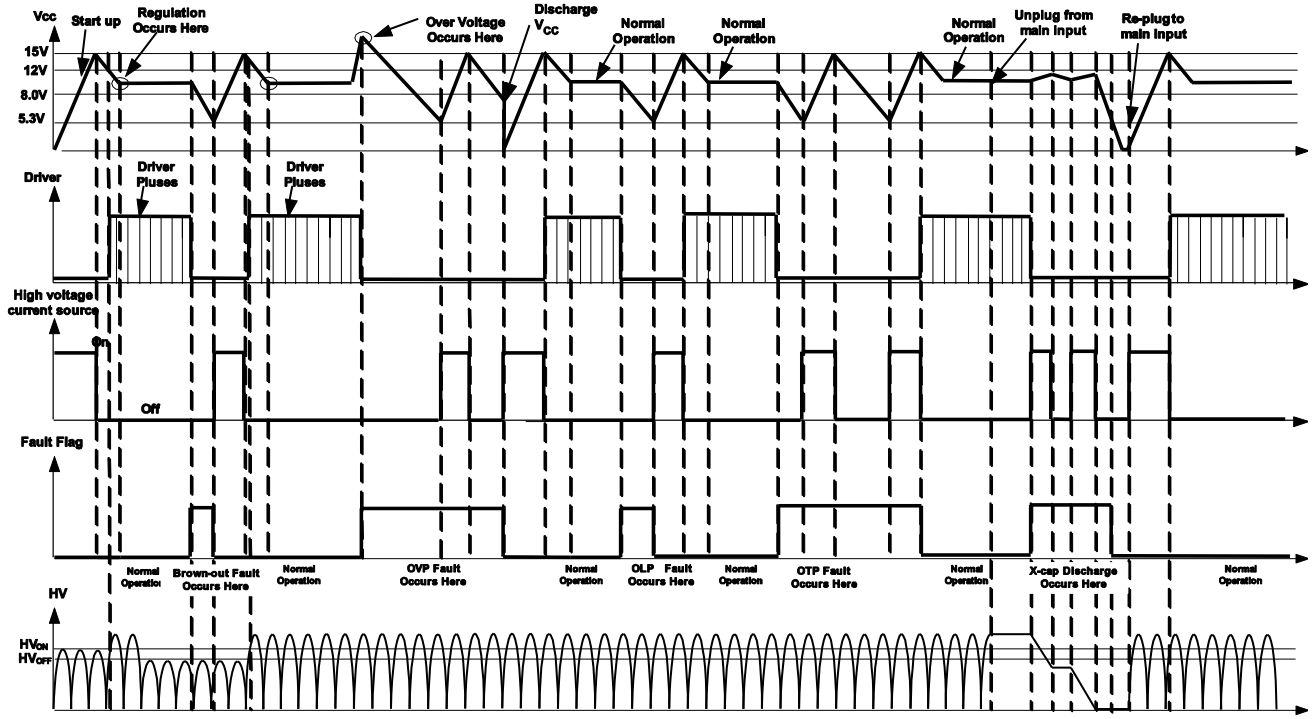
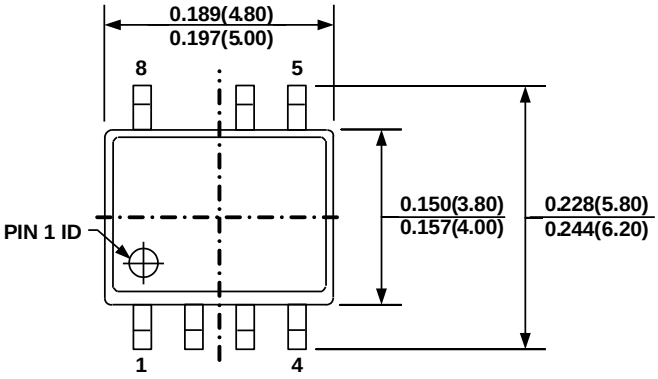


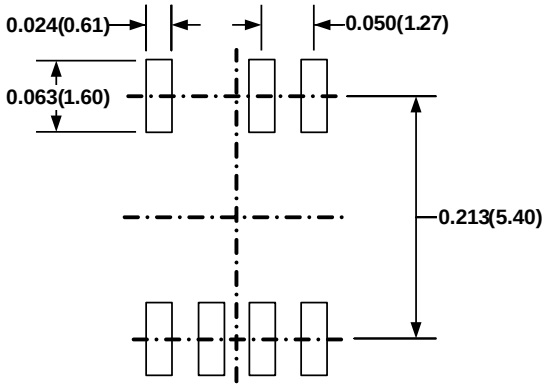
Figure 19: Signal Evolution in the Presence of Faults

PACKAGE INFORMATION

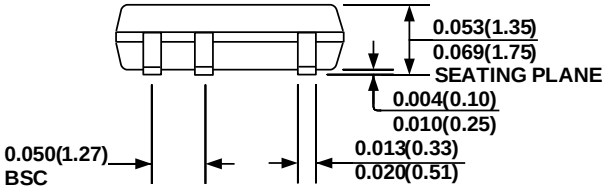
SOIC8-7A



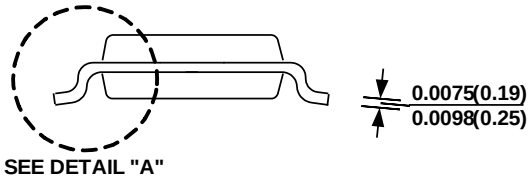
TOP VIEW



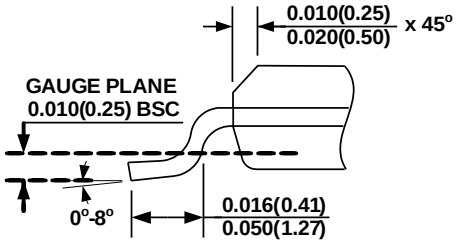
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE