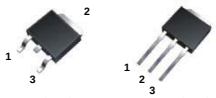
July 2015

SemiHow
Know-How for Semiconductor

HFD2N65F / HFU2N65F
600V N-Channel MOSFET

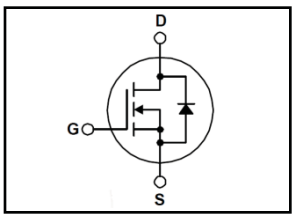
BV_{DSS} = 650 V
$R_{DS(on)\ typ}$ = 4 Ω
I_D = 2 A

D-PAK I-PAK



HFD2N65F HFU2N65F

1.Gate 2. Drain 3. Source



FEATURES

- ❑ Originative New Design
- ❑ Superior Avalanche Rugged Technology
- ❑ Robust Gate Oxide Technology
- ❑ Very Low Intrinsic Capacitances
- ❑ Excellent Switching Characteristics
- ❑ Unrivalled Gate Charge : 6.5 nC (Typ.)
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 4.0 Ω (Typ.) @V_{GS}=10V
- ❑ 100% Avalanche Tested

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		650	V
I_D	Drain Current – Continuous (T_C = 25℃)		2	A
	Drain Current – Continuous (T_C = 100℃)		1.3	A
I_{DM}	Drain Current – Pulsed	(Note 1)	8	A
V_{GS}	Gate-Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	110	mJ
I_{AR}	Avalanche Current	(Note 1)	2	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.2	mJ
P_D	Power Dissipation (T_A = 25℃)		2.5	W
	Power Dissipation (T_C = 25℃)		42	W
	- Derate above 25℃		0.34	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.98	℃/W
$R_{\theta JA}$	Junction-to-Ambient*	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1 A	--	4.0	5.0	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	10	μA
		V_{DS} = 520 V, T_C = 125℃	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	--	--	±100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	290	--	pF
C_{oss}	Output Capacitance		--	37	--	pF
C_{rss}	Reverse Transfer Capacitance		--	4.5	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 325 V, I_D = 2 A, R_G = 25 Ω (Note 4,5)	--	16	--	ns
t_r	Turn-On Rise Time		--	17	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	28	--	ns
t_f	Turn-Off Fall Time		--	20	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 2 A, V_{GS} = 10 V (Note 4,5)	--	6.5	--	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	2.2	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	2	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	8	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 2 A, V_{GS} = 0 V	--	--	1.4	V
trr	Reverse Recovery Time	I_S = 2 A, V_{GS} = 0 V, di_F/dt = 100 A/μs (Note 4)	--	200	--	ns
Qrr	Reverse Recovery Charge		--	0.7	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L=50mH, I_{AS}=2.0A, V_{DD}=50V, R_G=25Ω, Starting T_J =25°C
3. I_{SD}≤2.0A, di/dt≤200A/μs, V_{DD}≤BV_{DSS} , Starting T_J =25 °C
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Characteristics

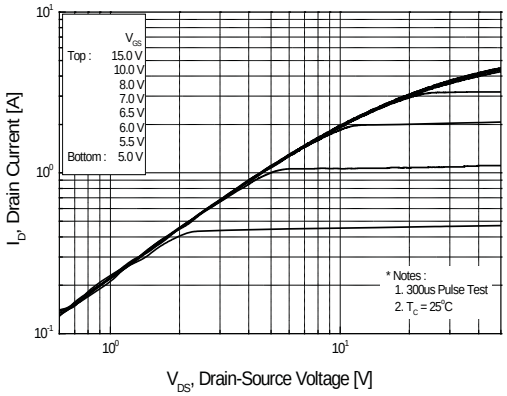


Figure 1. On Region Characteristics

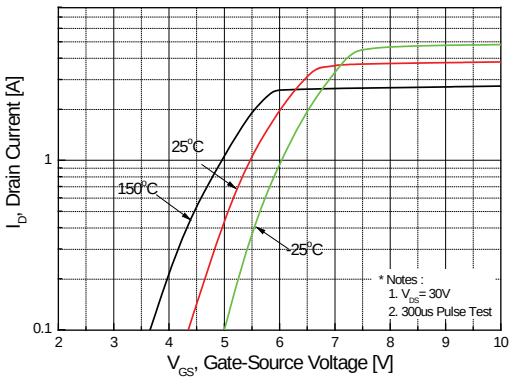


Figure 2. Transfer Characteristics

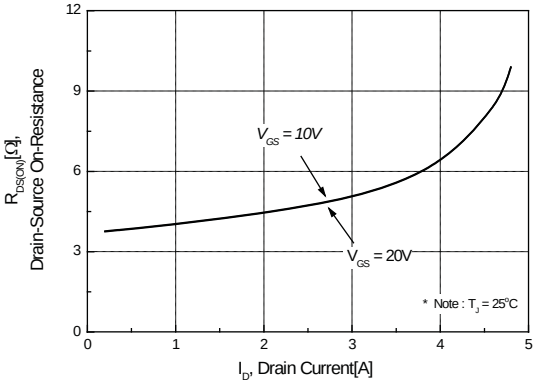


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

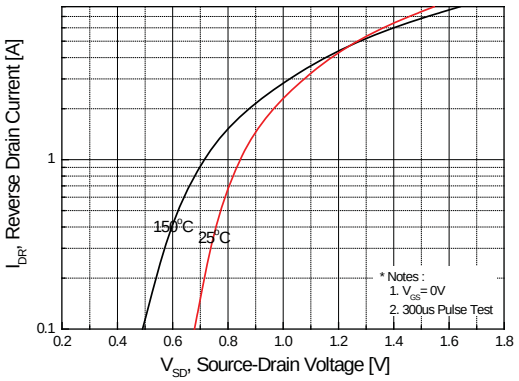


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

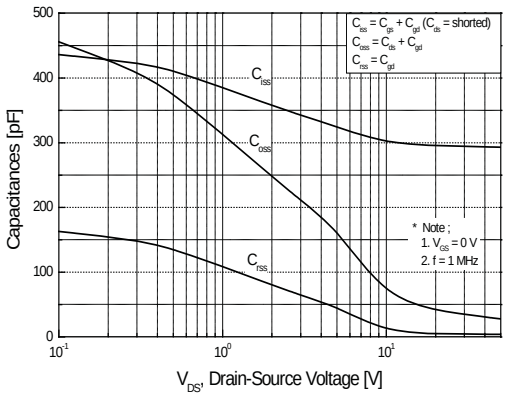


Figure 5. Capacitance Characteristics

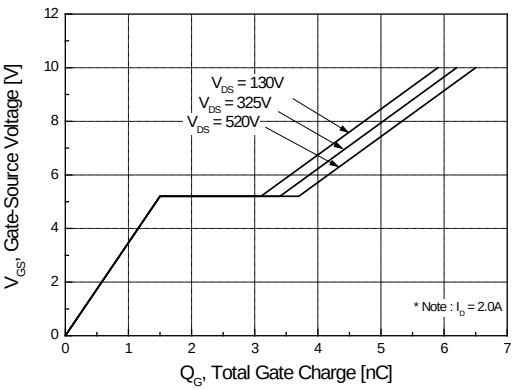


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

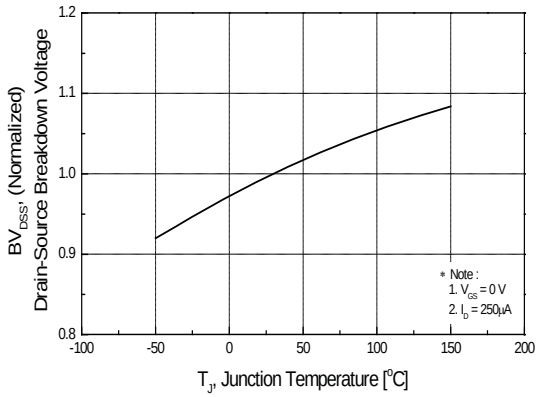


Figure 7. Breakdown Voltage Variation vs Temperature

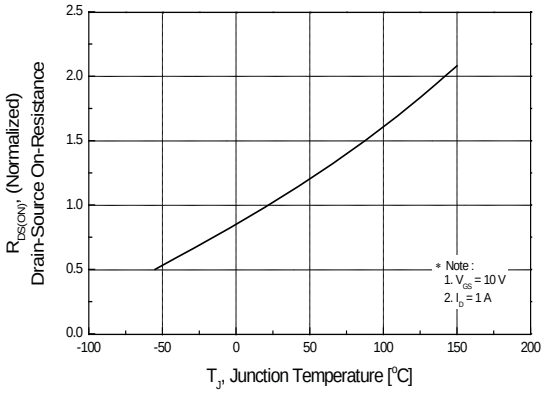


Figure 8. On-Resistance Variation vs Temperature

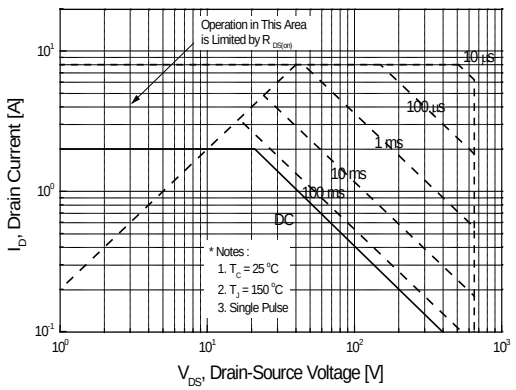


Figure 9. Maximum Safe Operating Area

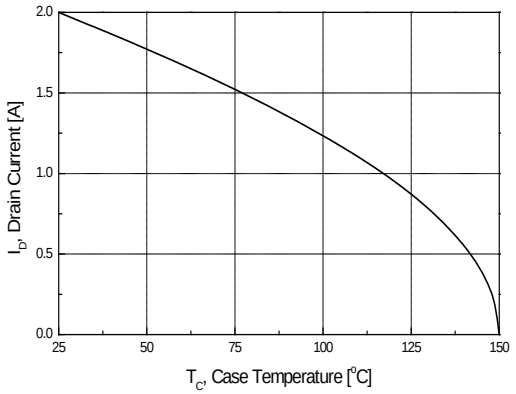


Figure 10. Maximum Drain Current vs Case Temperature

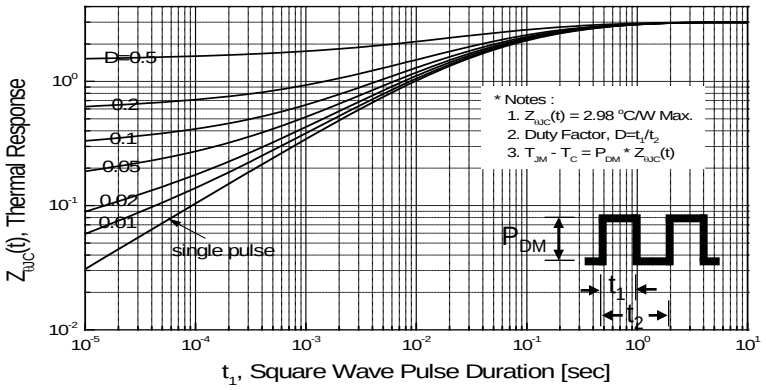


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

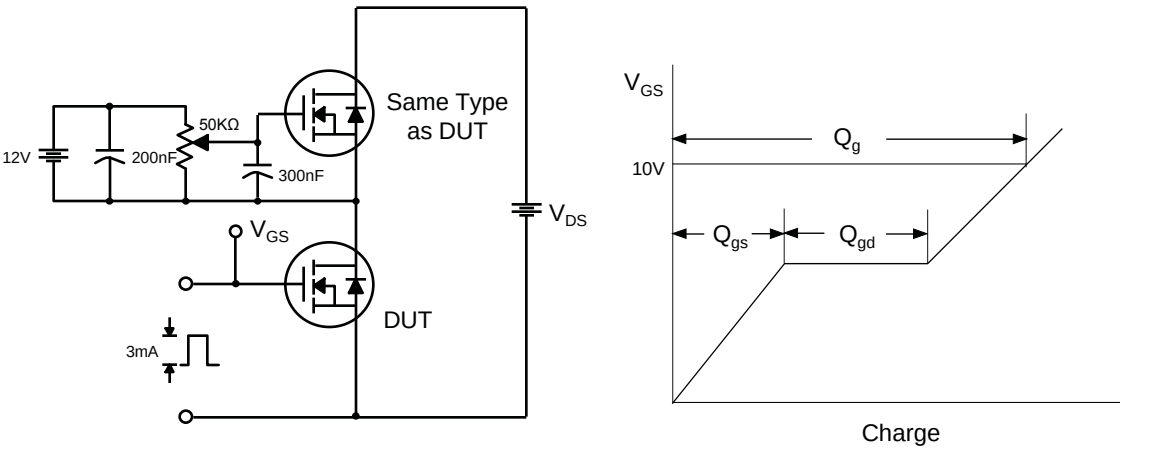


Fig 13. Resistive Switching Test Circuit & Waveforms

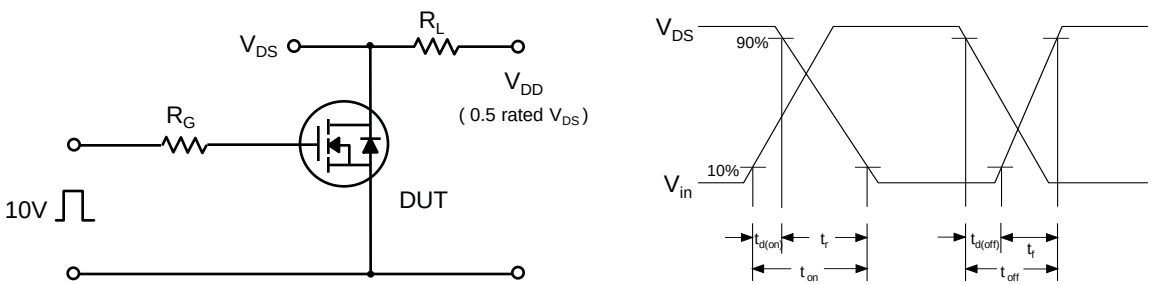


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

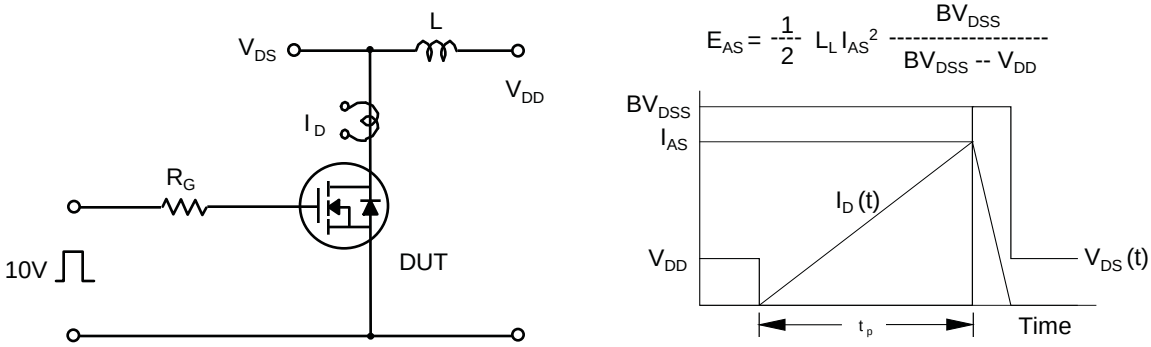
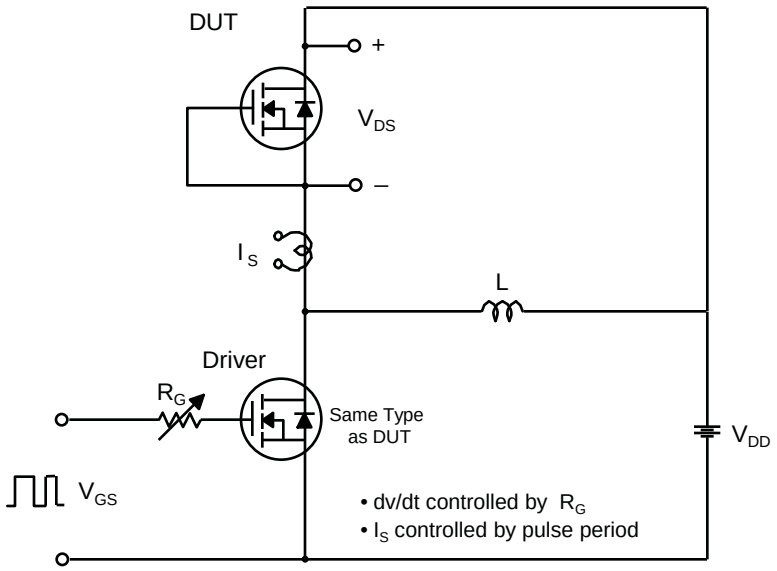
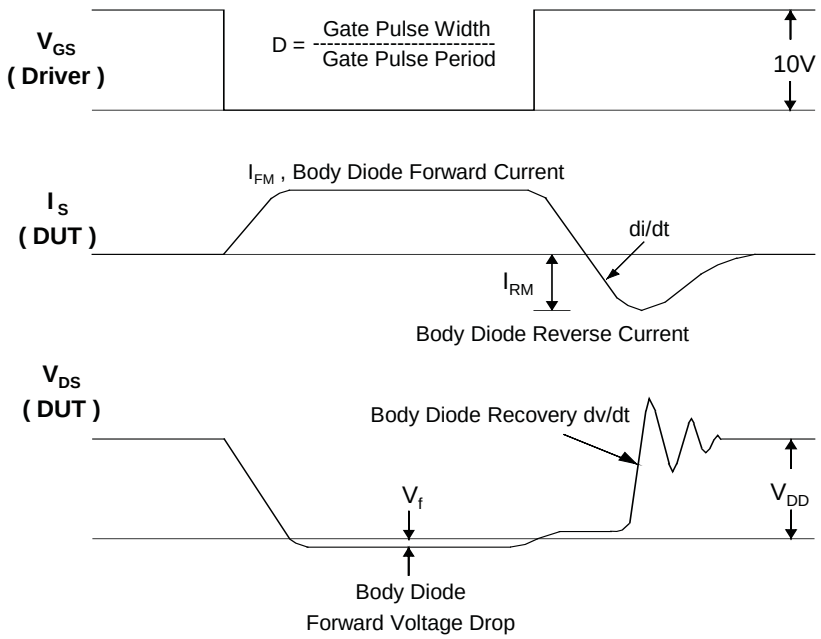


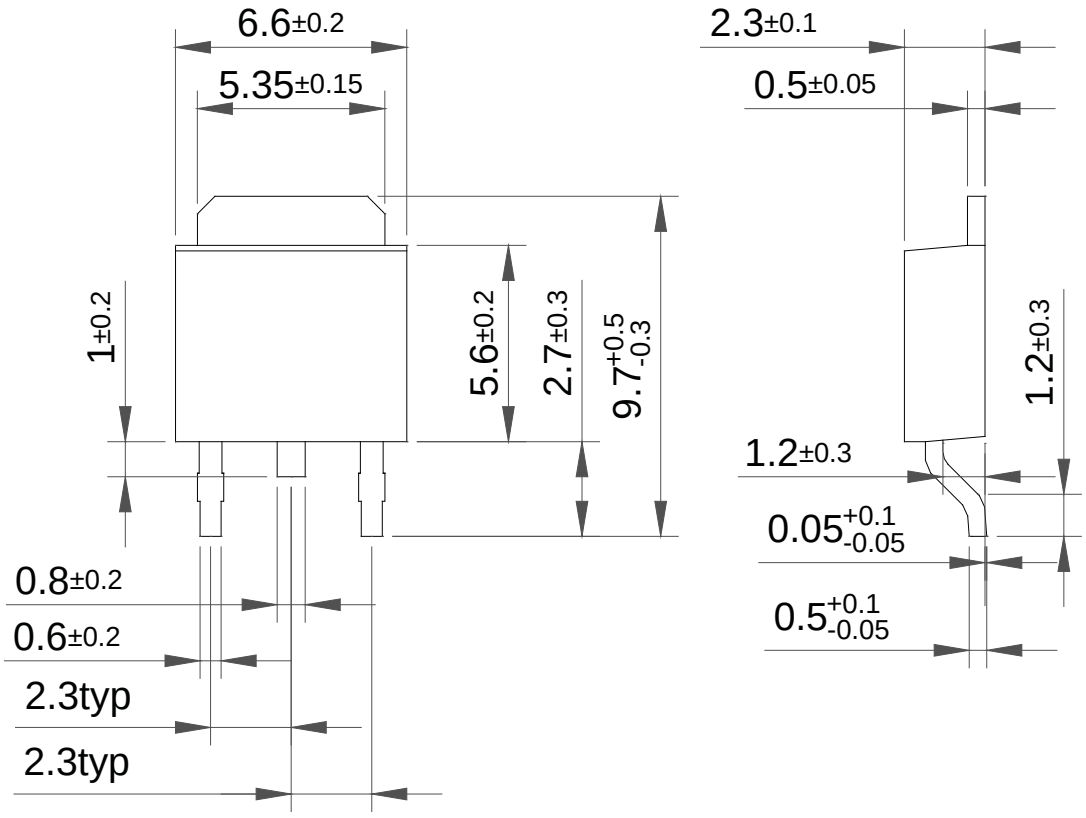
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimension

D-PAK
(TO-252)



Package Dimension

I-PAK
(TO-251)