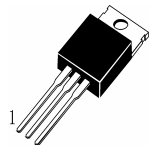
HFP13N10

N-Channel Enhancement Mode Field Effect Transistor

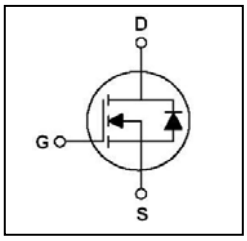
General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode . These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

TO-220



1- G 2- D 3- S



Features

- **13A, 100V, R_{DS}(on) <0.10Ω@V_{GS} = 10 V**
- **High density cell design for ultra low Rdson**
- **Fast switching**
- **100% avalanche tested**
- **Improved dv/dt capability**

Maximum Ratings (Ta=25℃ unless otherwise specified)

T_{stg}——Storage Temperature ---------- -55~150℃

T_j ——Operating Junction Temperature ---------- 150℃

V_{DSS} —— Drain-Source Voltage ----------100V

V_{GSS} —— Gate-Source Voltage ---------- ±20V

I_D —— Drain Current (Continuous)(T_c=25℃) ---------- 13A

I_{DM} —— Pulsed Drain Current (Note 1) ---------- 52A

P_D —— Maximum Power Dissipation (T_c=25℃) ---------- 65W

Derate Above 25℃ ---------- 0.43W/℃

E_{AS}—— Pulsed Avalanche Energy (Note 2) ---------- 250mJ

I_{AR}—— Avalanche Current (Note 1) ---------- 13A

E_{AR} —— Repetitive Avalanche Energy (Note 1) ---------- 6.5mJ

dv/dt —— Peak Diode Recovery dv/dt (Note 3) ----------6V/ns

Thermal Characteristics

Symbol	Items	TO-220	Unit
Rthj-case	Thermal Resistance Junction-case	Max 2.3	℃/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 62.5	℃/W

Electrical Characteristics (Ta=25℃ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	100			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	V_{DS} =100V, V_{GS}=0V
				10	μA	V_{DS} =80V, V_{GS}=0V,Tj=150℃
I_{GSS}	Gate – Body Leakage			±100	nA	V_{GS}= ±20V , V_{DS} =0V
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{DS} = V_{GS} , I_D=250μA
$R_{DS(on)}$	Static Drain-Source On-Resistance		0.06	0.10	Ω	V_{GS}=10V, I_D=6.5A
Dynamic Characteristics and Switching Characteristics						
Ciss	Input Capacitance		1350		pF	V_{DS} = 25 V, V_{GS} = 0V, f = 1.0 MHz
Coss	Output Capacitance		240		pF	
Crss	Reverse Transfer Capacitance		180		pF	
$t_{d(on)}$	Turn - On Delay Time		13.8		nS	V_{DD} = 30V, I_D=2A, V_{GS} = 10 V R_G= 2.5 Ω (Note 4,5)
tr	Rise Time		9.3		nS	
$t_{d(off)}$	Turn - Off Delay Time		43.8		nS	
t_f	Fall Time		11.4		nS	
Qg	Total Gate Charge		31		nC	V_{DS}=30V, ID=3A, V_{GS} = 10 V (Note 4,5)
Qgs	Gate–Source Charge		6.4		nC	
Qgd	Gate–Drain Charge		9.4		nC	
Drain-Source Diode Characteristics and Maximun Ratings						
I_S	Continuous Source–Drain Diode Forward Current			13	A	
I_{SM}	Pulsed Drain-Source Diode Forward Current			52	A	
V_{SD}	Source–Drain Diode Forward On–Voltage			1.5	V	I_S=13A,V_{GS}=0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=0.5mH, V_G=10V, V_{DD}=50V, R_G=25 Ω ,T_J=25℃
3. I_{SD}≤13.0A, di/dt≤300A/μS,V_{DD}≤BVDSS, Starting T_J=25℃
4. Pulse Test: Pulse width≤300μS, Duty Cycle≤2%
5. Essentially independent of operating temperature

Typical Characteristics

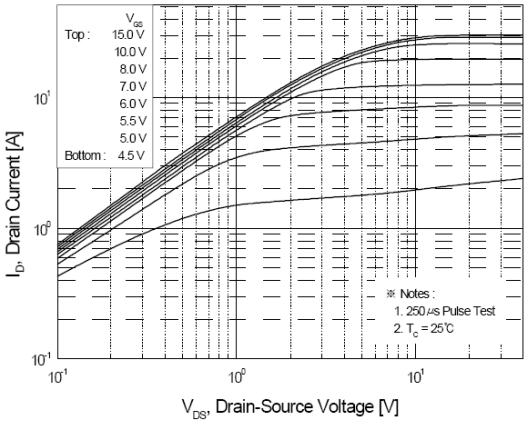


Figure 1. On-Region Characteristics

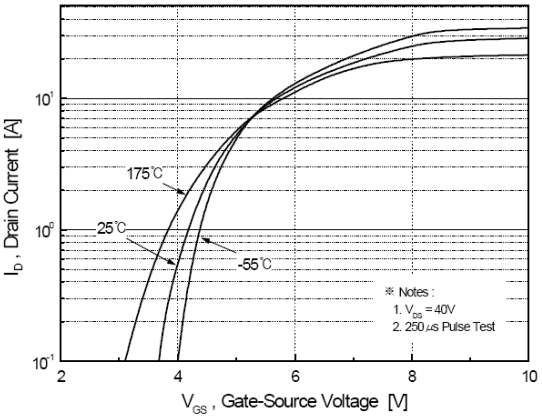


Figure 2. Transfer Characteristics

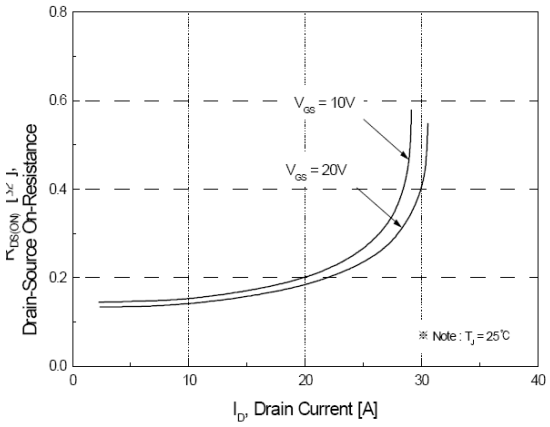


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

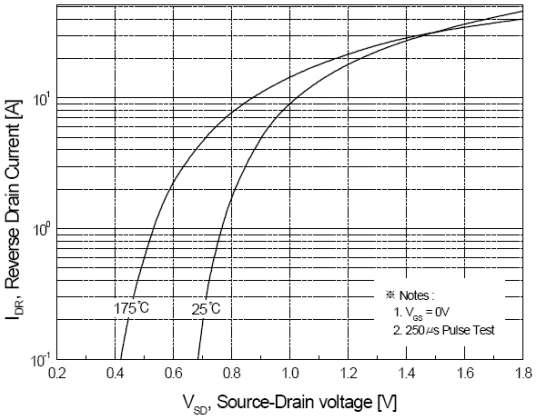


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

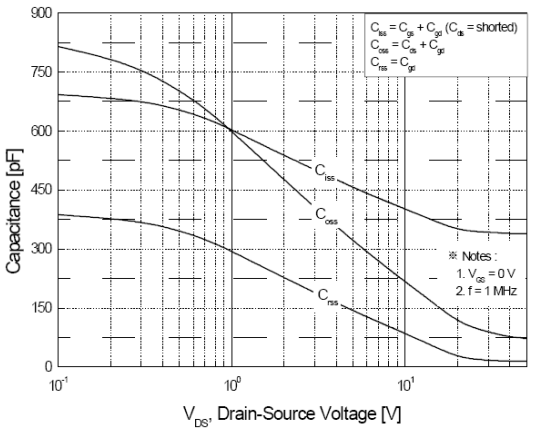


Figure 5. Capacitance Characteristics

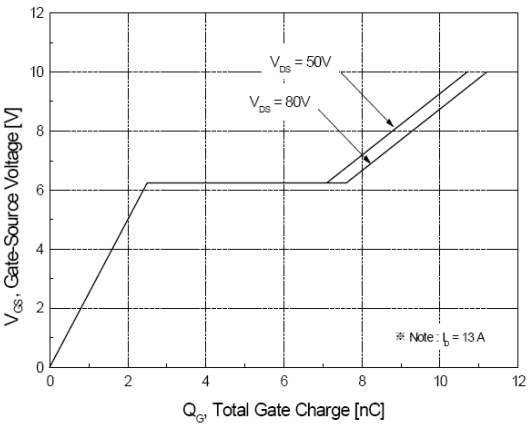


Figure 6. Gate Charge Characteristics

Typical Characteristics

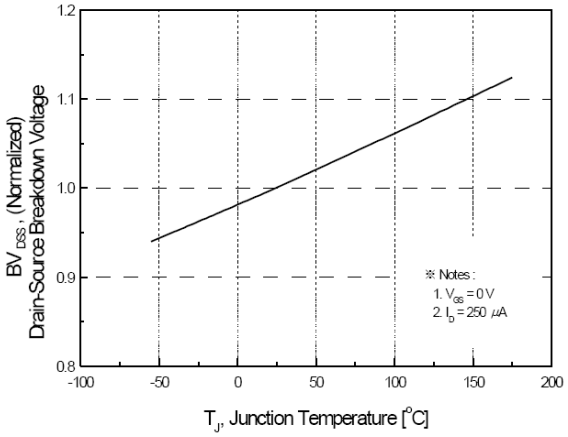


Figure 7. Breakdown Voltage Variation vs. Temperature

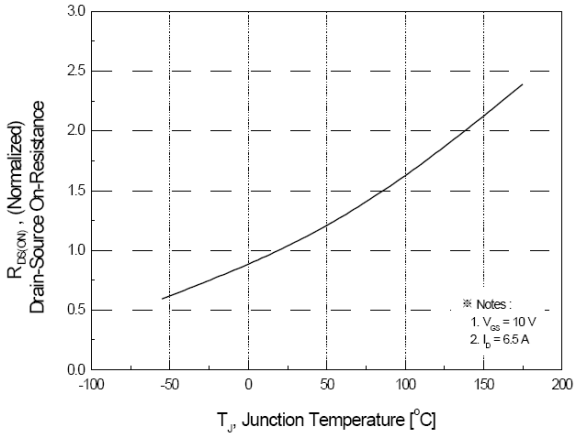


Figure 8. On-Resistance Variation vs. Temperature

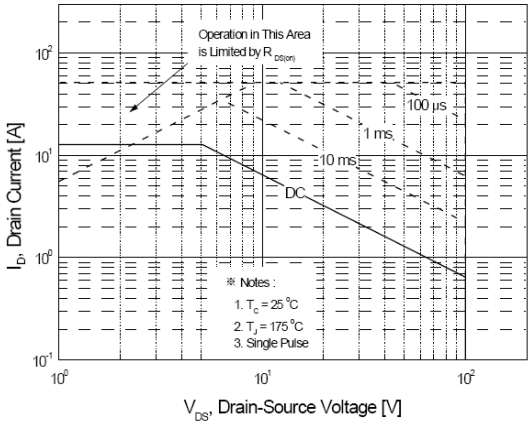


Figure 9. Maximum Safe Operating Area

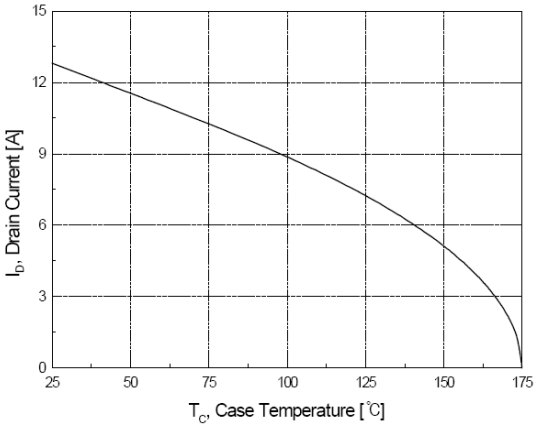


Figure 10. Maximum Drain Current vs. Case Temperature

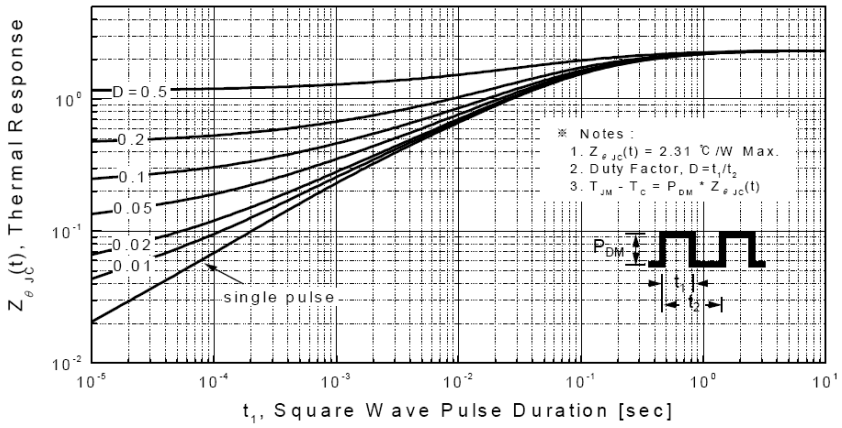


Figure 11. Transient Thermal Response Curve

Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

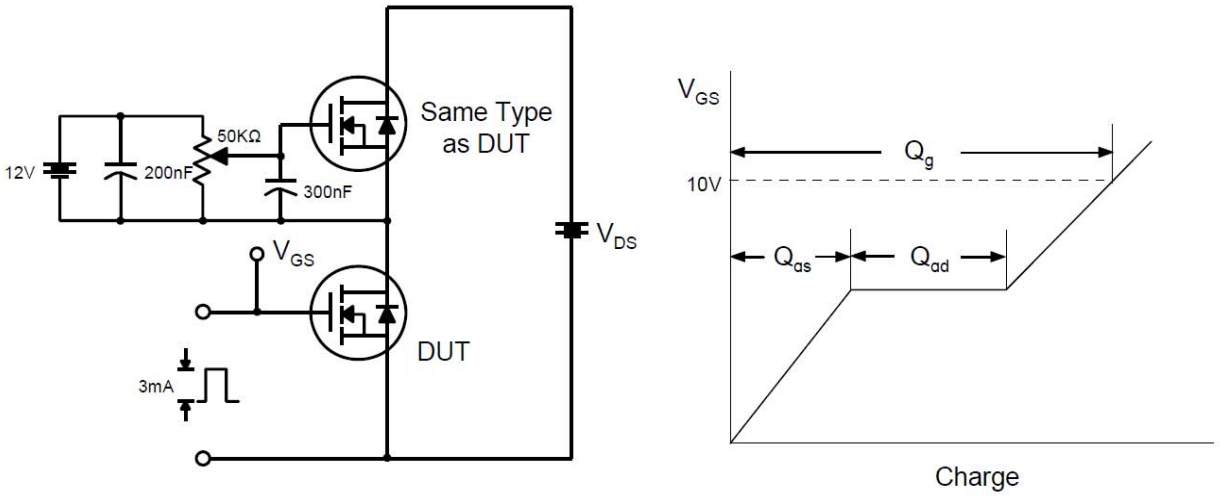


Fig 13. Resistive Switching Test Circuit & Waveforms

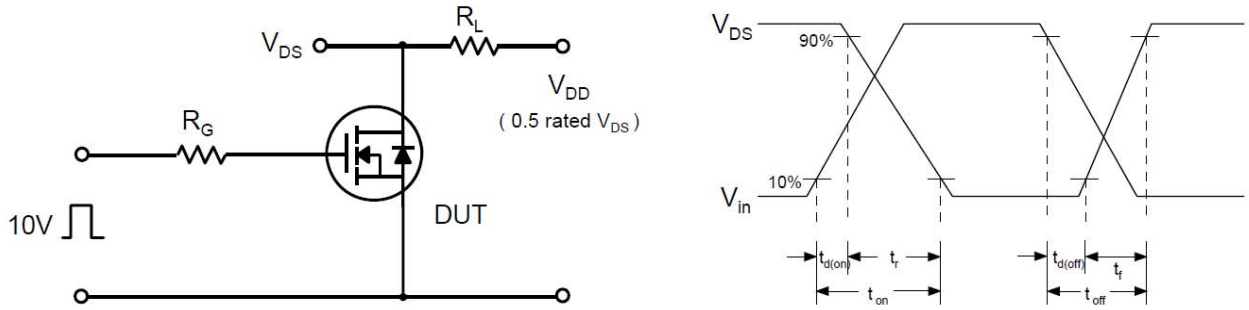
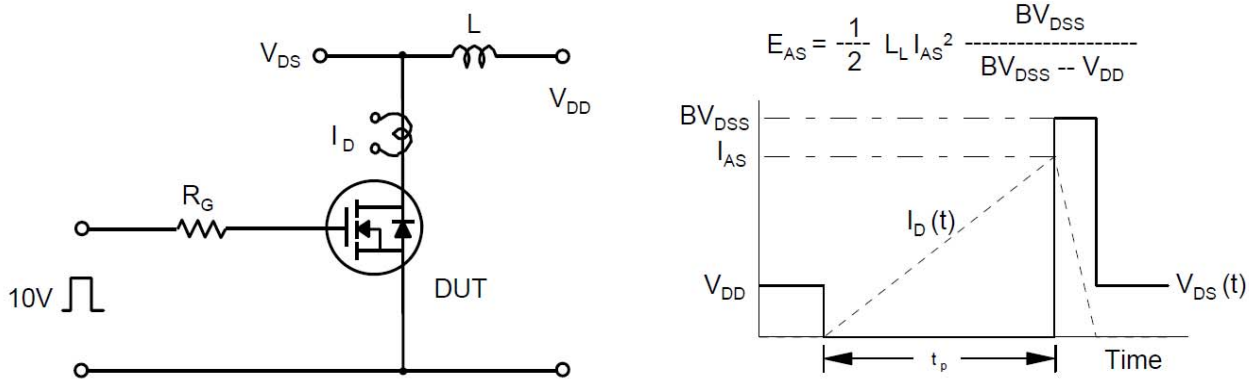
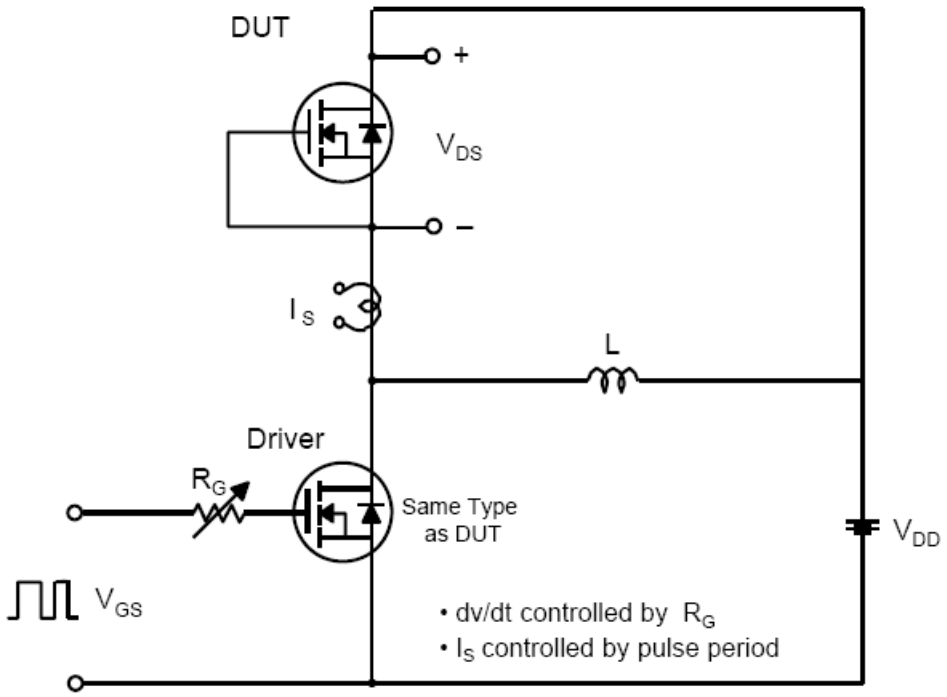


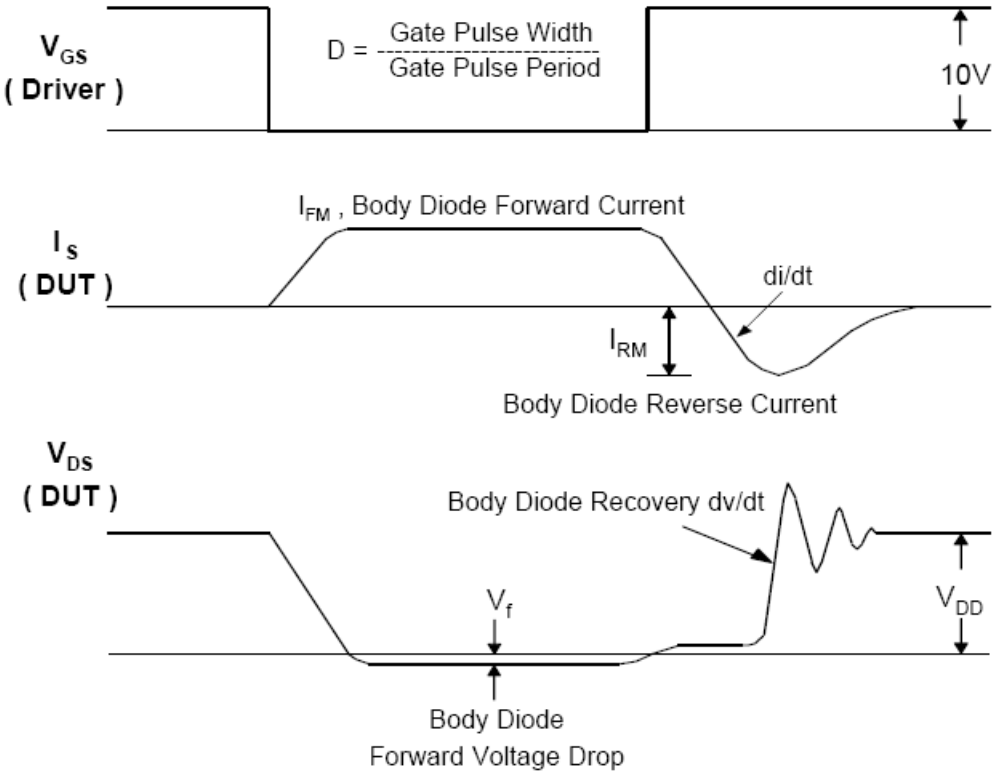
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



Typical Characteristics

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions