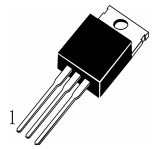
HFP17N10

N-Channel Enhancement Mode Field Effect Transistor

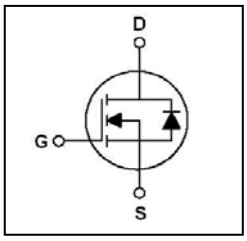
General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode . These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

TO-220



1- G 2- D 3- S



Features

- **17A, 100V, R_{DS}(on) <70mΩ@V_{GS} = 10 V**
- **High density cell design for ultra low Rdson**
- **Fast switching**
- **100% avalanche tested**
- **Improved dv/dt capability**

Maximum Ratings (Ta=25℃ unless otherwise specified)

T_{stg}——Storage Temperature ---------- -55~150℃

T_j ——Operating Junction Temperature ---------- 150℃

V_{DSS} —— Drain-Source Voltage ----------100V

V_{GSS} —— Gate-Source Voltage ---------- ±20V

I_D —— Drain Current (Continuous)(T_c=25℃) ---------- 17A

I_{DM} —— Pulsed Drain Current (Note 1) ---------- 60A

P_D —— Maximum Power Dissipation (T_c=25℃) ---------- 55W

Derate Above 25℃ ---------- 0.43W/℃

E_{AS}—— Pulsed Avalanche Energy (Note 2) ---------- 250mJ

I_{AR}—— Avalanche Current (Note 1) ---------- 17A

Thermal Characteristics

Symbol	Items	TO-220	Unit
Rthj-case	Thermal Resistance Junction-case	Max 2.27	℃/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 62.5	℃/W

Electrical Characteristics (Ta=25℃ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	100			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	V_{DS} =100V, V_{GS}=0V
				10	μA	V_{DS} =80V, V_{GS}=0V,Tj=150℃
I_{GSS}	Gate – Body Leakage			±100	nA	V_{GS}= ±20V , V_{DS} =0V
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{DS} = V_{GS} , I_D=250μA
$R_{DS(on)}$	Static Drain-Source On-Resistance			80	mΩ	V_{GS}=10V, I_D=8.5A
Dynamic Characteristics and Switching Characteristics(Note 3)						
Ciss	Input Capacitance		1350		pF	V_{DS} = 25 V, V_{GS} = 0V, f = 1.0 MHz
Coss	Output Capacitance		240		pF	
Crss	Reverse Transfer Capacitance		180		pF	
$t_{d(on)}$	Turn - On Delay Time		13.8		nS	V_{DD} = 30V, I_D=2A, V_{GS} = 10 V R_G= 2.5 Ω (Note 4,5)
tr	Rise Time		9.3		nS	
$t_{d(off)}$	Turn - Off Delay Time		43.8		nS	
t_f	Fall Time		11.4		nS	
Qg	Total Gate Charge		31		nC	V_{DS}=30V, ID=3A, V_{GS} = 10 V (Note 4,5)
Qgs	Gate–Source Charge		6.4		nC	
Qgd	Gate–Drain Charge		9.4		nC	
Drain-Source Diode Characteristics and Maximun Ratings						
I_S	Continuous Source–Drain Diode Forward Current			17	A	
I_{SM}	Pulsed Drain-Source Diode Forward Current			60	A	
V_{SD}	Source–Drain Diode Forward On–Voltage			1.2	V	I_S=9A,V_{GS}=0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=0.5mH, V_G=10V, V_{DD}=50V, R_G=25 Ω ,T_J=25℃
3. Guaranteed by design, not subject to production
4. Pulse Test: Pulse width≤300μS, Duty Cycle≤2%
5. Essentially independent of operating temperature

Typical Characteristics

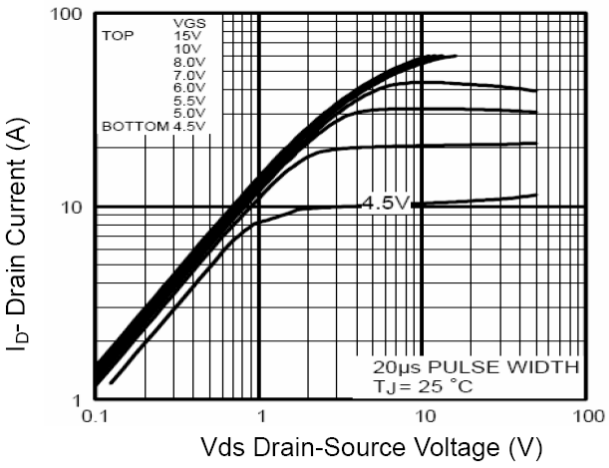


Figure 1 Output Characteristics

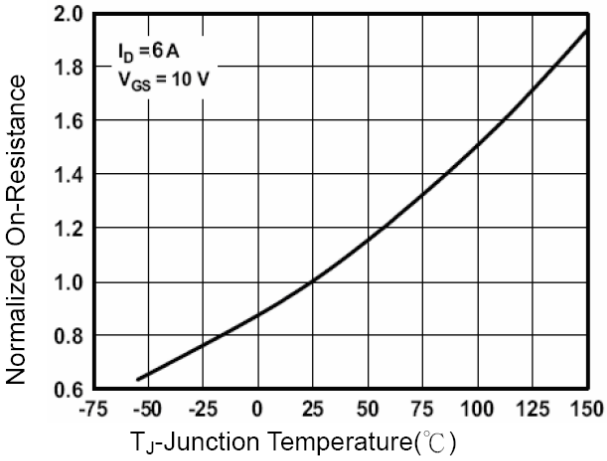


Figure 4 Rdson-JunctionTemperature

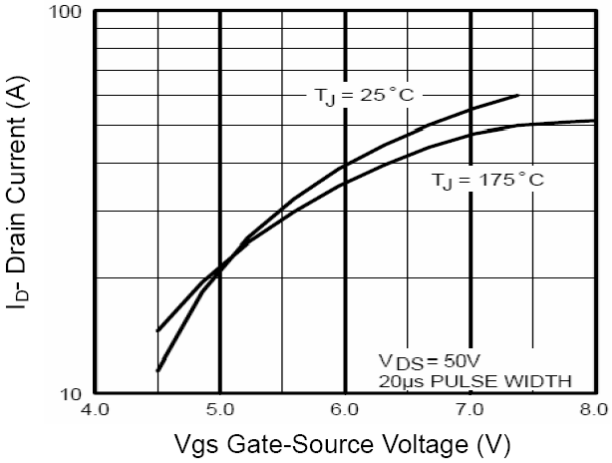


Figure 2 Transfer Characteristics

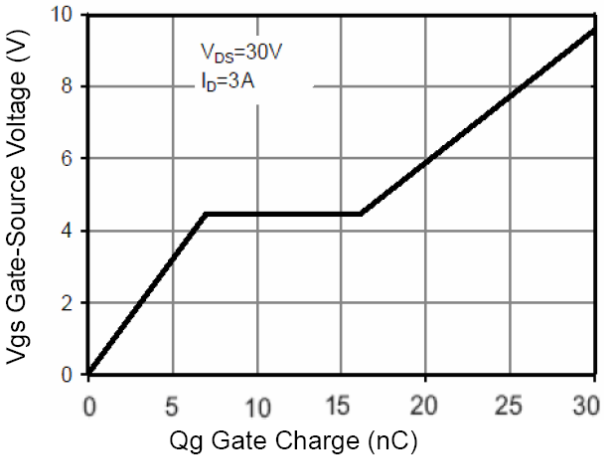


Figure 5 Gate Charge

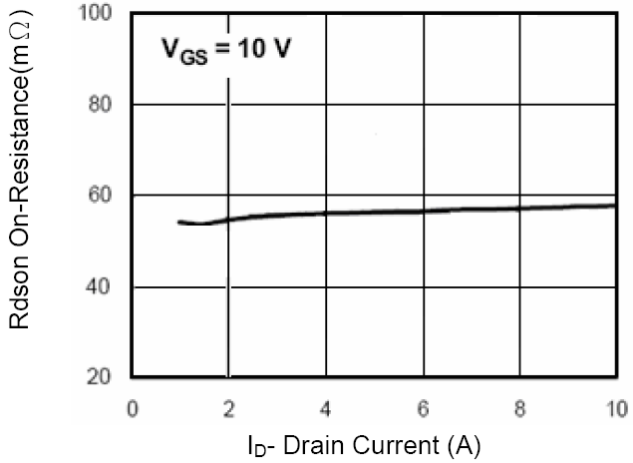


Figure 3 Rdson- Drain Current

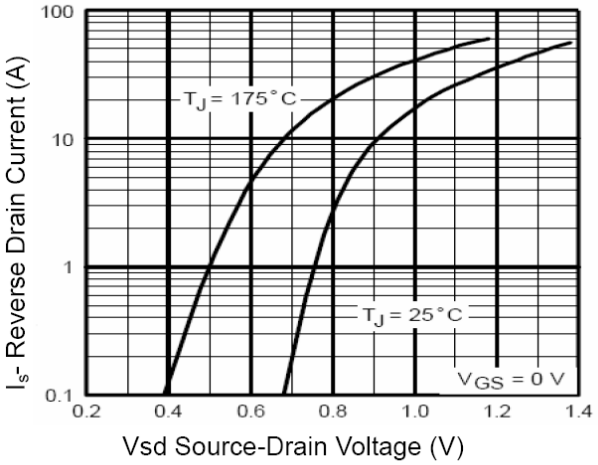


Figure 6 Source- Drain Diode Forward

Typical Characteristics

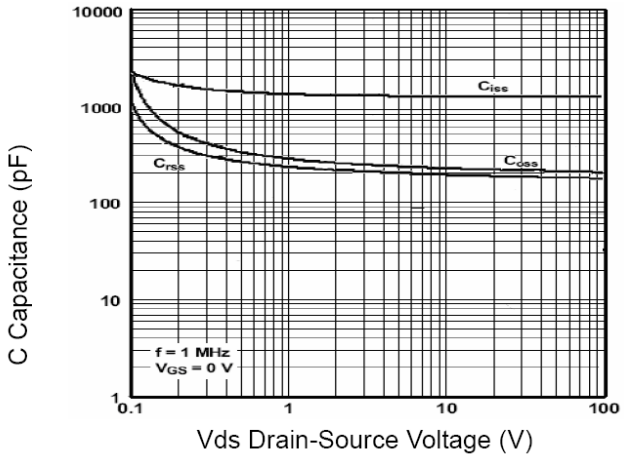


Figure 7 Capacitance vs Vds

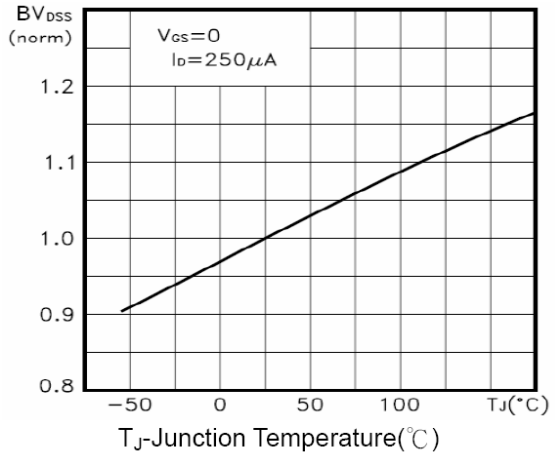


Figure 9 BV_{DSS} vs Junction Temperature

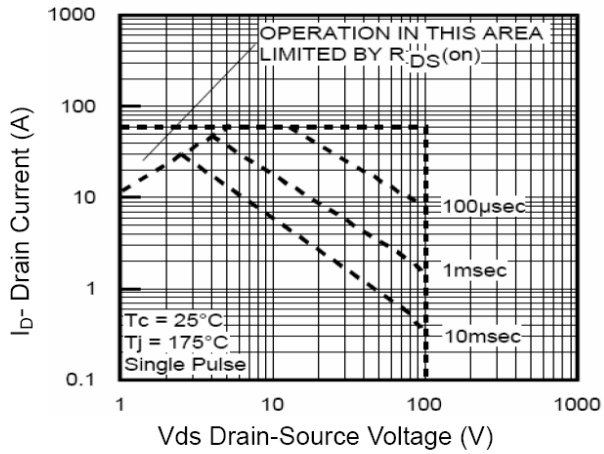


Figure 8 Safe Operation Area

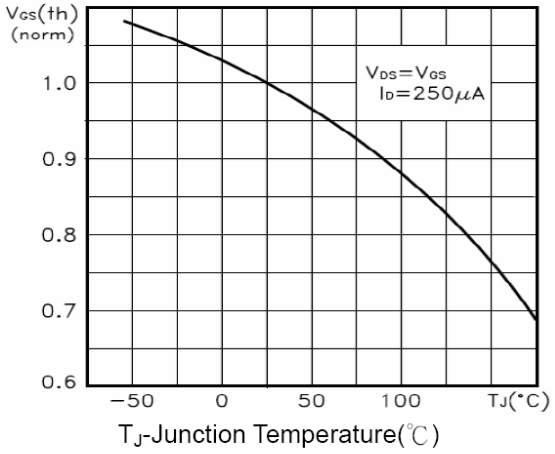


Figure 10 $V_{GS(th)}$ vs Junction Temperature

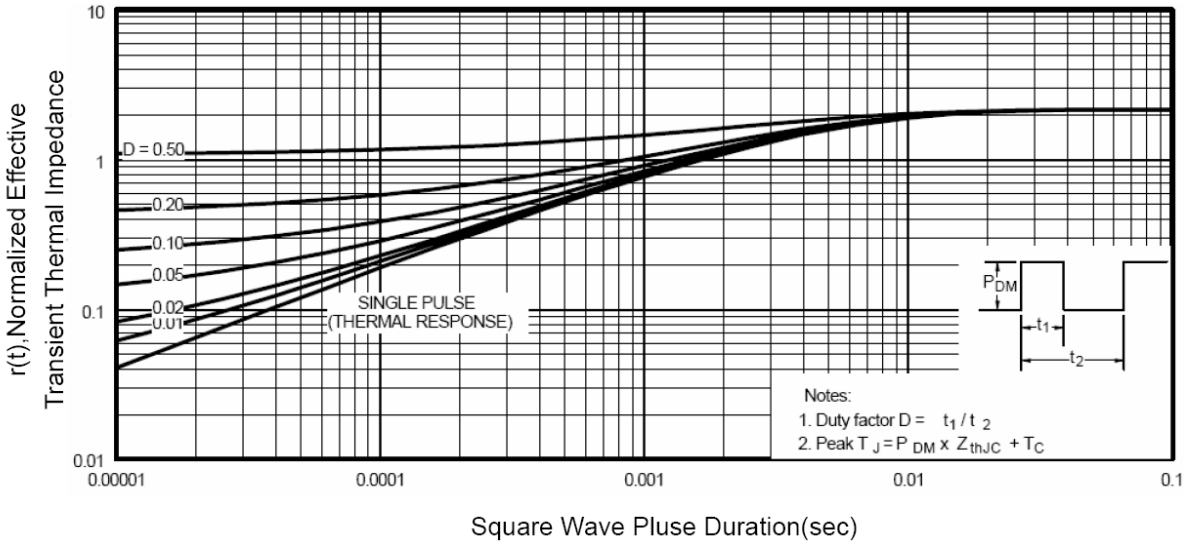


Figure 11 Normalized Maximum Transient Thermal Impedance

Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

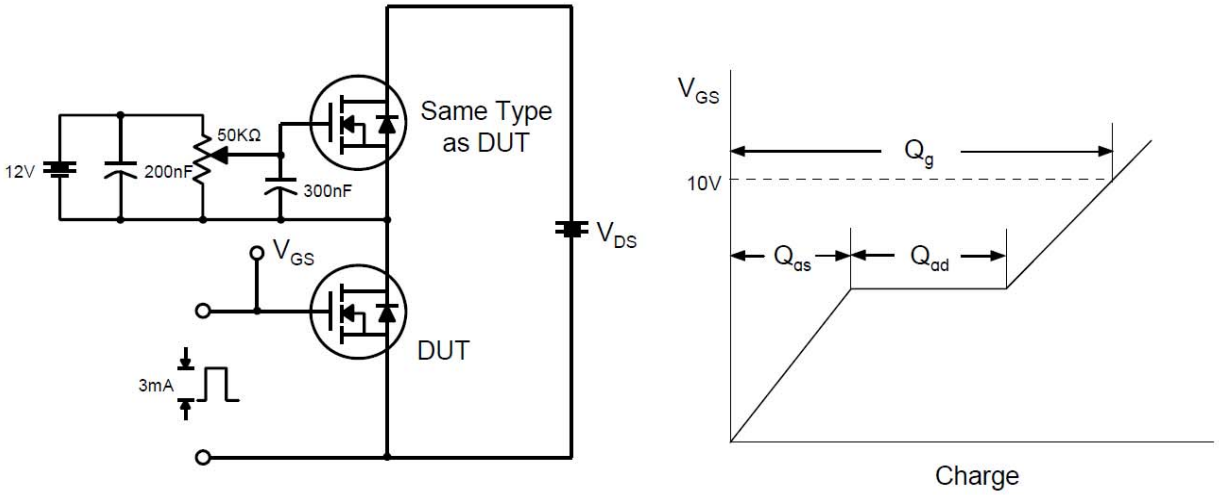


Fig 13. Resistive Switching Test Circuit & Waveforms

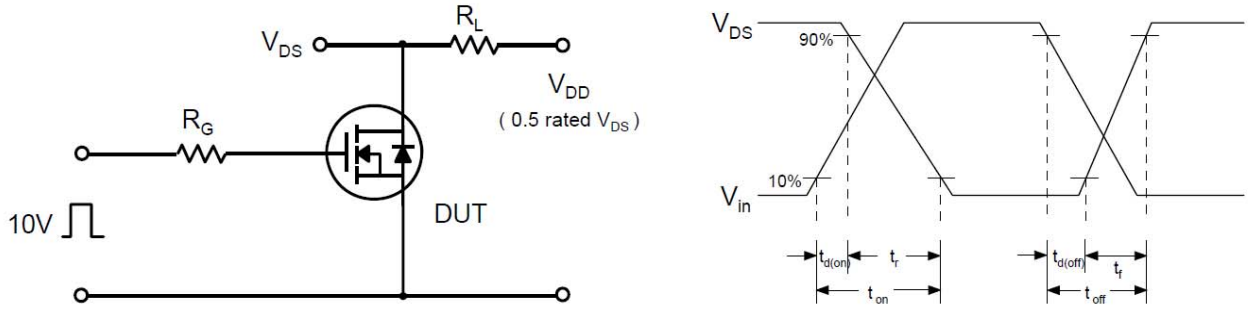
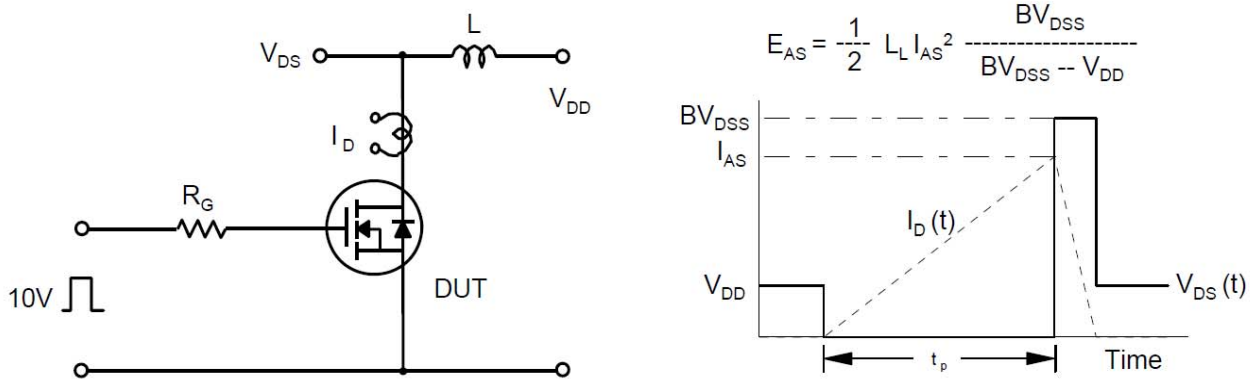
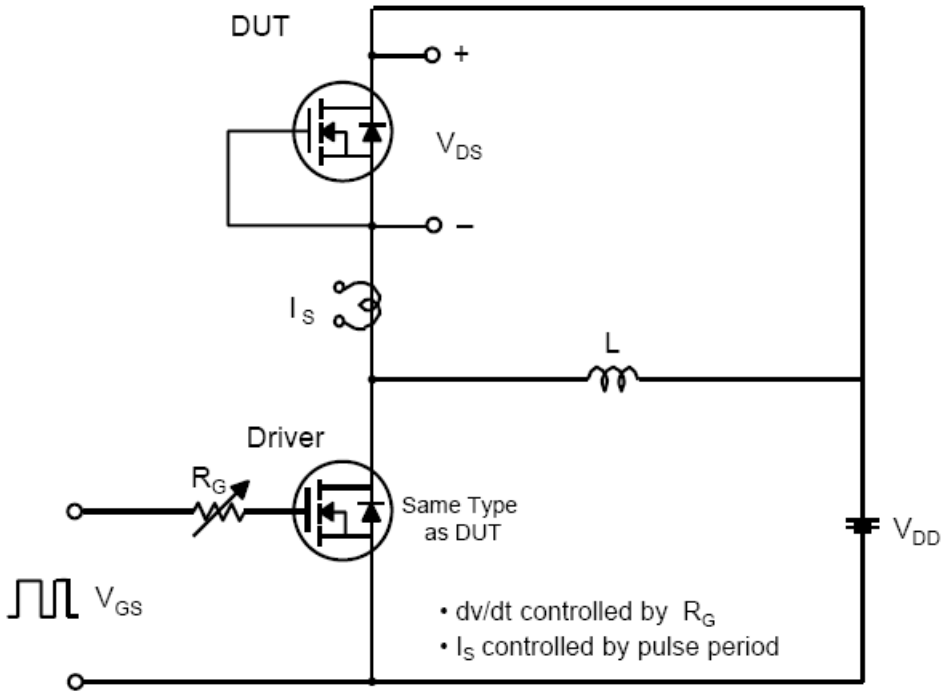


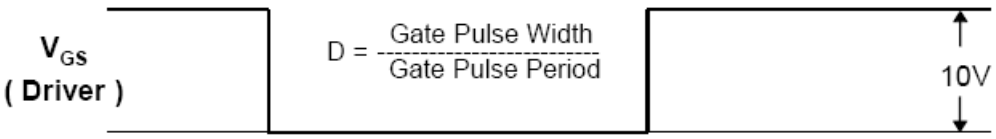
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

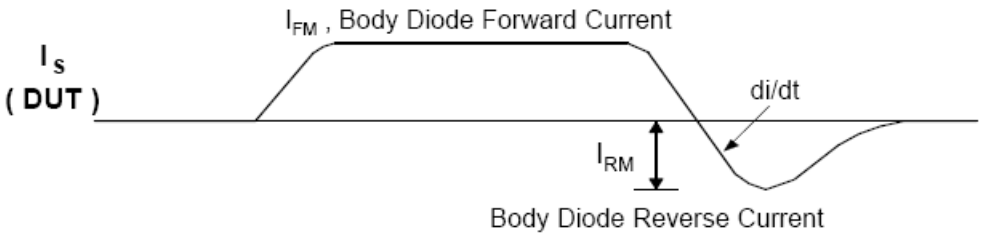


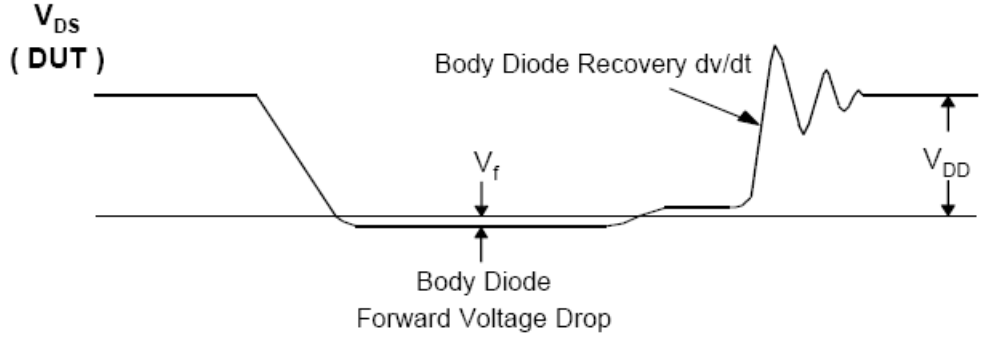
Typical Characteristics

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms









Package Dimensions