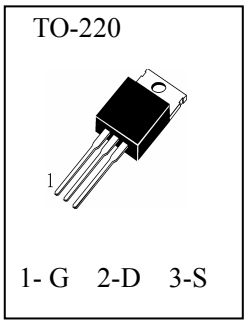
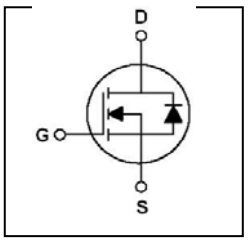
HFP5N80

N-Channel Enhancement Mode Field Effect Transistor

General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode . These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.





Features

- **4.8A, 800V(See Note), R_{DS}(on) <2.6Ω@V_{GS} = 10 V**
- **Fast switching**
- **100% avalanche tested**
- **Improved dv/dt capability**
- **Equivalent Type:FQP5N80**

Maximum Ratings (Ta=25℃ unless otherwise specified)

T_{stg}——Storage Temperature ---------- -55~150℃

T_j ——Operating Junction Temperature ---------- 150℃

V_{DSS} —— Drain-Source Voltage ----------800V

V_{GSS} —— Gate-Source Voltage ---------- ±30V

I_D —— Drain Current (Continuous)(T_c=25℃) ---------- 4.8A

I_{DM} —— Pulsed Drain Current (Note 1)---------- 19.2A

P_D —— Maximum Power Dissipation (T_c=25℃) ---------- 140W

Derate Above 25℃ ---------- 1.12W/℃

E_{AS}—— Pulsed Avalanche Energy (Note 2) ---------- 590mJ

I_{AR}—— Avalanche Current (Note 1) ---------- 4.8A

E_{AR} —— Repetitive Avalanche Energy (Note 1) ---------- 14mJ

dv/dt —— Peak Diode Recovery dv/dt (Note 3) ----------4.0V/ns

Thermal Characteristics

Symbol	Items	TO-220	Unit
Rthj-case	Thermal Resistance Junction-case	Max 0.89	℃/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 62.5	℃/W

Electrical Characteristics (Ta=25℃ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	800			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} =800V, V_{GS}=0V
				100	μA	V_{DS} =640V, V_{GS}=0V,Tj=125℃
I_{GSS}	Gate – Body Leakage			±100	nA	V_{GS}= ±30V , V_{DS} =0V
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	3.0		5.0	V	V_{DS} = V_{GS} , I_D=250μA
$R_{DS(on)}$	Static Drain-Source On-Resistance		2.0	2.6	Ω	V_{GS}=10V, I_D=2.4A
Dynamic Characteristics and Switching Characteristics						
Ciss	Input Capacitance		950	1250	pF	V_{DS} = 25 V, V_{GS} = 0V, f = 1.0 MHz
Coss	Output Capacitance		95	125	pF	
Crss	Reverse Transfer Capacitance		11	15	pF	
$t_{d(on)}$	Turn - On Delay Time		22	55	nS	V_{DS} = 400V, I_D=4.8A, R_G= 25 Ω (Note 4,5)
tr	Rise Time		60	130	nS	
$t_{d(off)}$	Turn - Off Delay Time		55	120	nS	
t_f	Fall Time		40	90	nS	
Qg	Total Gate Charge		25	33	nC	V_{DS}=640V, ID=4. 8A, V_{GS} = 10 V (Note 4,5)
Qgs	Gate–Source Charge		5.6		nC	
Qgd	Gate–Drain Charge		12		nC	
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Continuous Source–Drain Diode Forward Current			4.8	A	
I_{SM}	Pulsed Drain-Source Diode Forward Current			19.2	A	
V_{SD}	Source–Drain Diode Forward On–Voltage			1.4	V	I_S=4.8A,V_{GS}=0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=48mH,I_{AS}=4.8A, V_{DD}=50V, R_G=25 Ω ,Starting T_J=25℃
3. I_{SD}≤4.8A, di/dt≤200A/μS,V_{DD}≤BVDSS, Starting T_J=25℃
4. Pulse Test: Pulse width≤300μS, Duty Cycle≤2%
2. Essentially independent of operating temperature

Typical Characteristics

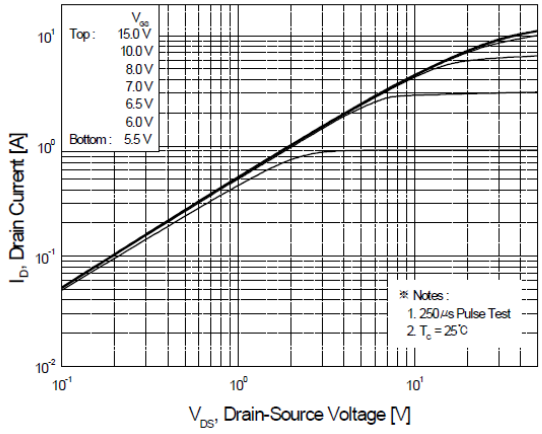


Figure 1. On-Region Characteristics

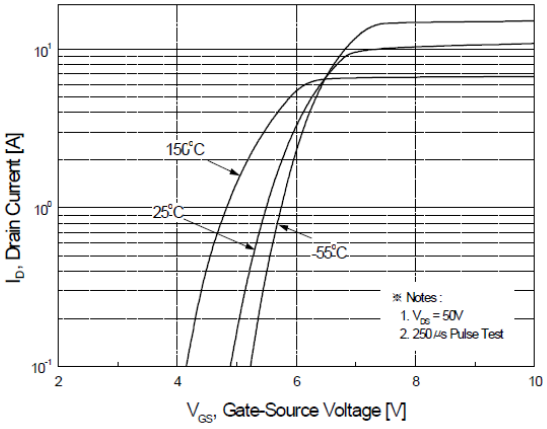


Figure 2. Transfer Characteristics

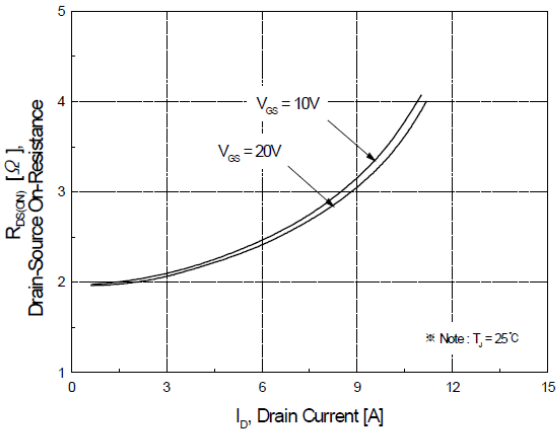


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

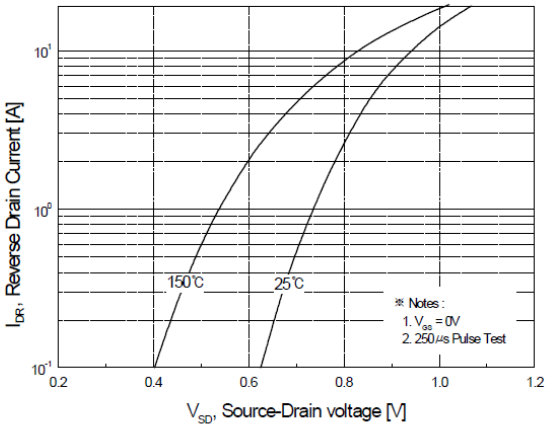


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

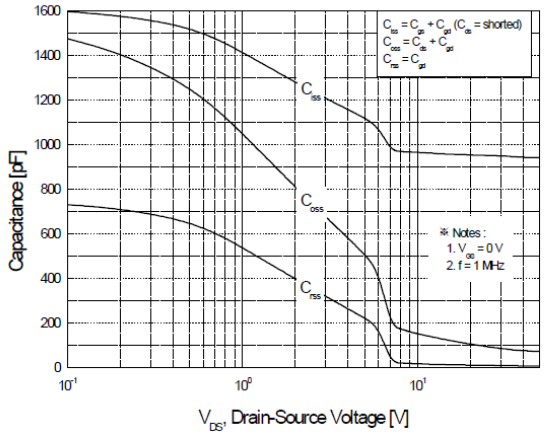


Figure 5. Capacitance Characteristics

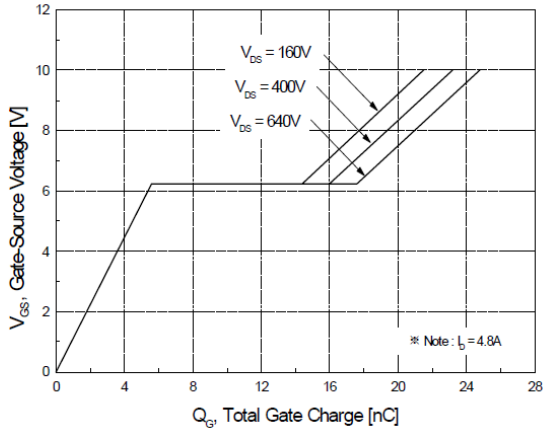


Figure 6. Gate Charge Characteristics

Typical Characteristics

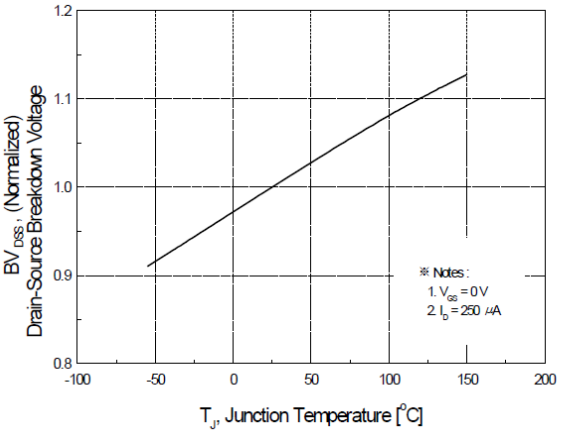


Figure 7. Breakdown Voltage Variation vs Temperature

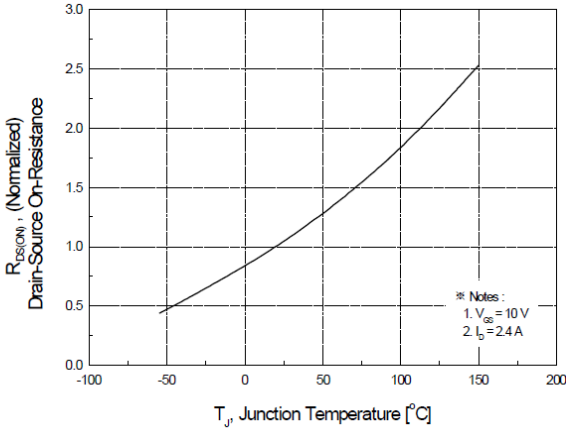


Figure 8. On-Resistance Variation vs Temperature

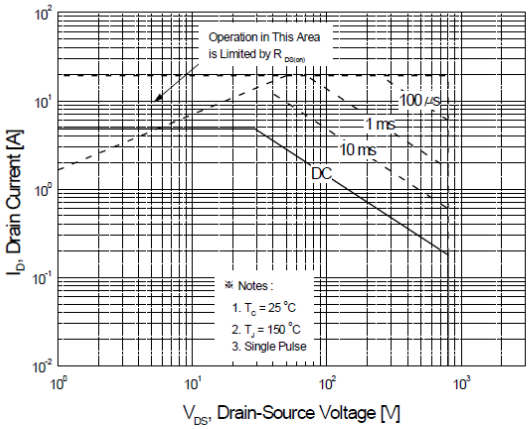


Figure 9. Maximum Safe Operating Area

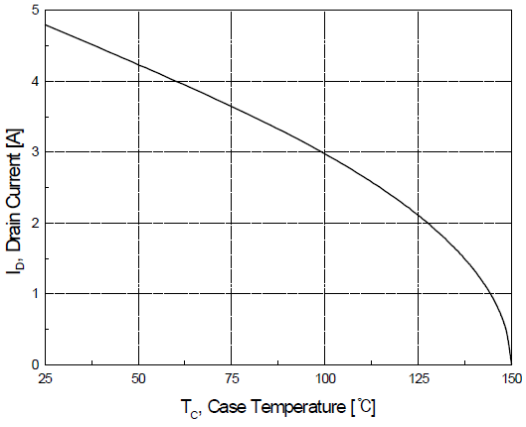


Figure 10. Maximum Drain Current vs Case Temperature

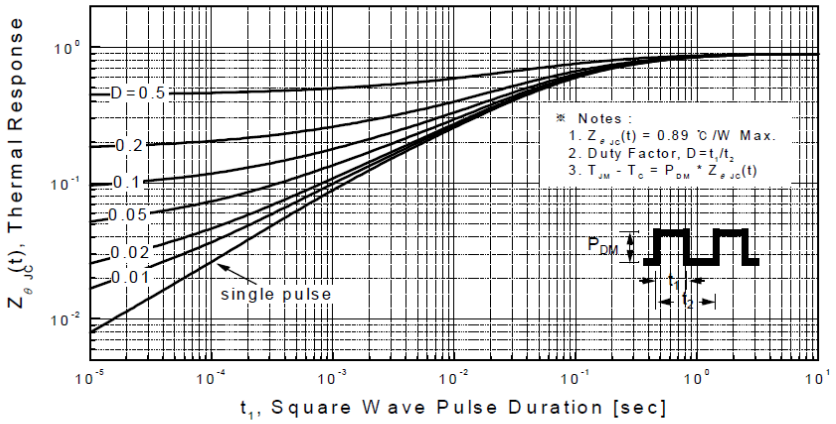


Figure 11. Transient Thermal Response Curve

Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

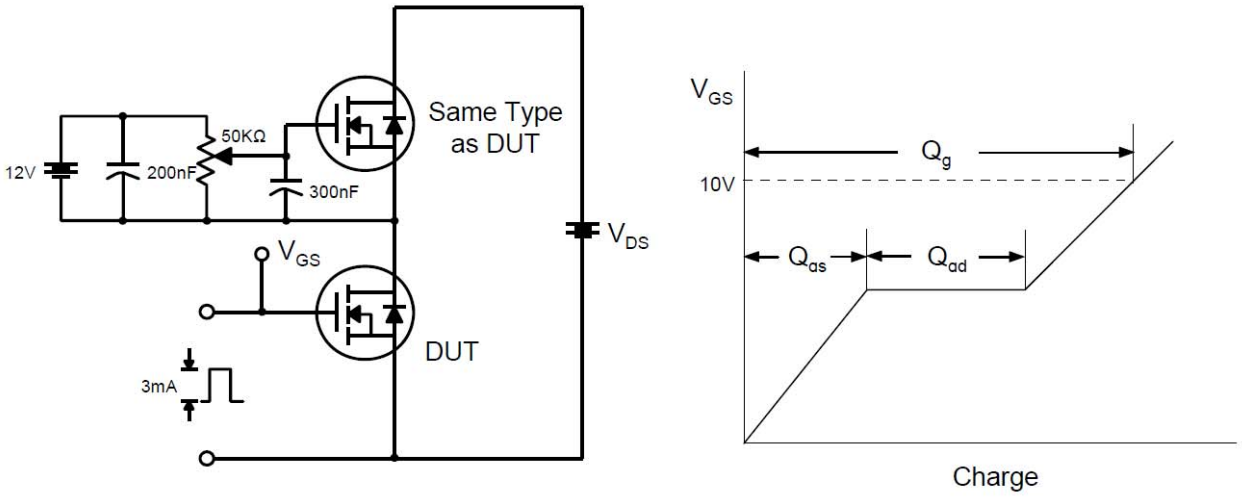


Fig 13. Resistive Switching Test Circuit & Waveforms

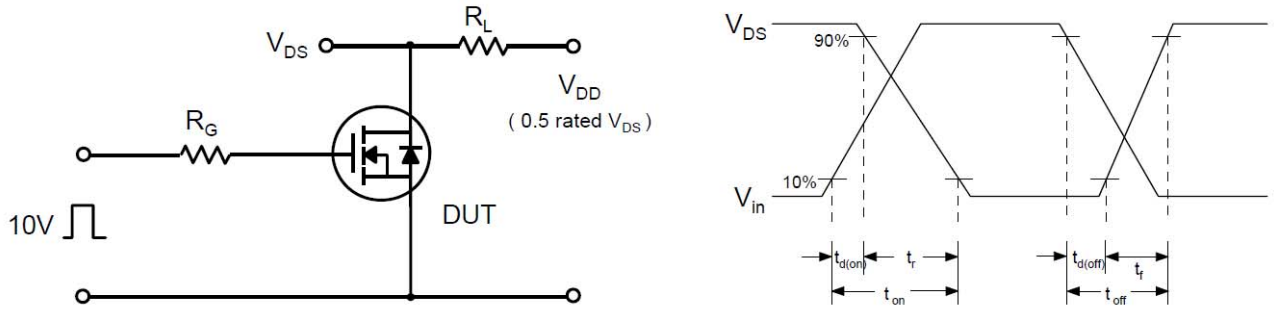
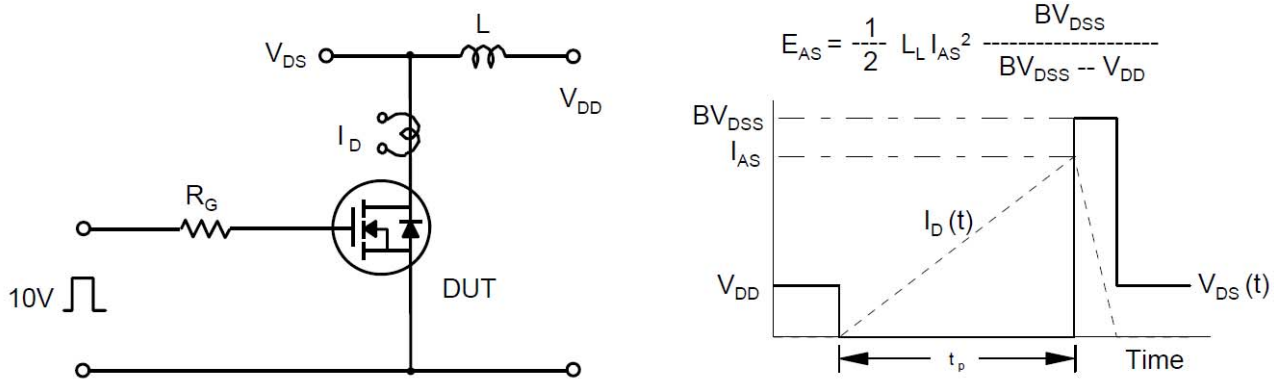


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



Typical Characteristics

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms