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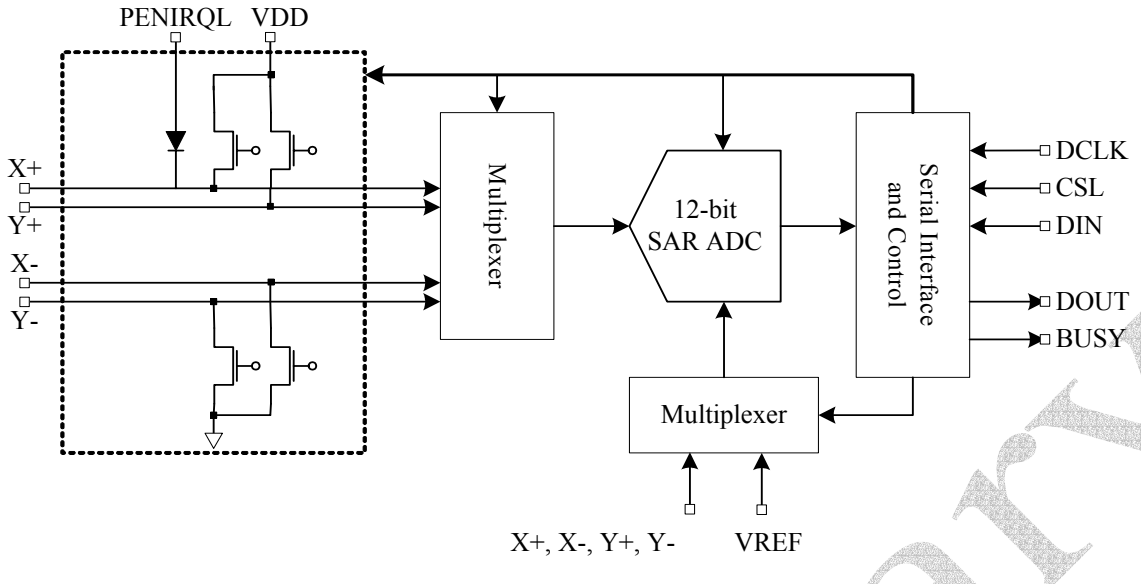
1. General Description

The HFT012 integrates a 12-bit SAR type Analog-to-Digital converter, a synchronous serial interface and low on-resistance switches on a chip. The X/Y driver is automatically configured for X/Y position, X-plate resistance and touch pressure measurements for a 4-wire resistive type touch screen. With the built-in X/Y drivers and the low power design techniques the chip is suitable for battery-operated system and other portable equipment application. The HFT012 features direct battery measurement, temperature measurement and touch-pressure measurement. When not in use, the internal reference can be shut down to conserve power. An external reference can also be applied and can be varied from 1 V to VDD, while the analog input range is from 0 V to VREF. The device includes a shutdown mode that reduces the current consumption to less than 1 μA.

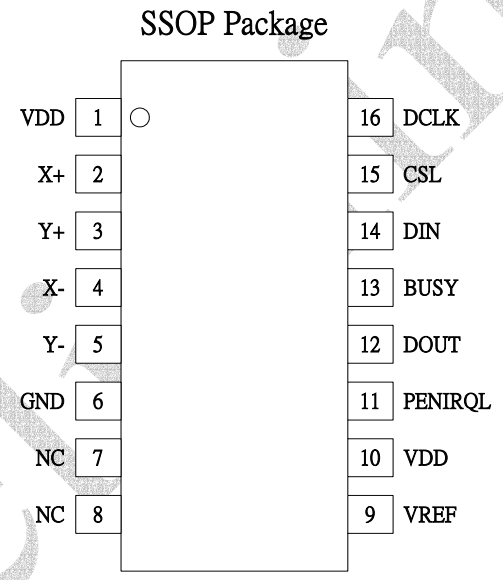
2. Features

- ✓ Wide Supply Range: 2.4V to 5.5V
- ✓ 4-Wire Touch Screen Interface
- ✓ 125 kSPS Sampling Rate
- ✓ 8/12Bit Resolution Selection
- ✓ Serial Input Control
- ✓ Serial Data Output
- ✓ Single Ended/Differential Reference
- ✓ Fully Power Down Control
- ✓ Position Measurement for X/Y
- ✓ X-Plate Sheet Resistance Measurement
- ✓ Touch Pressure Measurement

3. Block Diagram



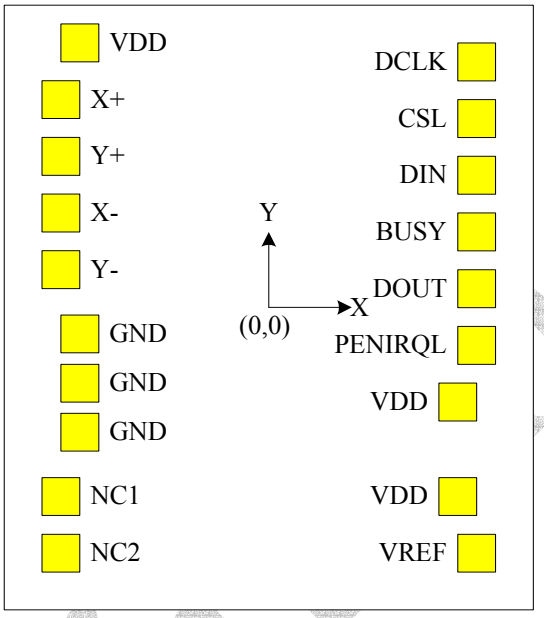
4. Pin Description



Pin Name	I/O	Description
X+	I	X+ position input, ADC input channel 1
Y+	I	Y+ position input, ADC input channel 2
X-	I	X- position input
Y-	I	Y- position input
NC	I	No Connect
VREF	I	Voltage Reference Input: 1V to VDD
PENIRQL	I	Pen Interrupt (requires 10k~100k ohms pull up resistor externally
DOUT	O	Serial Data output. High impedance when CSL is high
BUSY	O	Busy Output. High impedance when CSL is high.
DIN	I	Serial Data Input

Pin Name	I/O	Description
CSL	I	Chip Select Input (Active Low); this pin is used to initialize the transmission and ADC conversion, **don't tied to GND directly.**
DCLK	I	Serial Interface Clock Input
VDD	P	Power Supply: 2.4V to 5.5V
GND	P	

5. Pads Locations



Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	VDD	-474.2	506.5	11	VREF	503.7	-505.5
2	X+	-503.7	396.5	12	VDD	474.2	-395
3	Y+	-503.7	286.5	13	VDD	474.2	-183.8
4	X-	-503.7	176.5	14	PENIRQL	503.7	-73.3
5	Y-	-503.7	66.5	15	DOUT	503.7	36.7
6	GND	-474.2	-53.9	16	BUSY	503.7	146.7
7	GND	-474.2	-163.9	17	DIN	503.7	256.7
8	GND	-474.2	-273.9	18	CSL/RST	503.7	366.7
9	NC1	-503.7	-399.5	19	DCLK	503.7	476.7
10	NC2	-503.7	-509.5				

6. Configuration of ADC

Serial Interface

The CSL signal initiates the data transfer and conversion process, user shall don't tie this pin to ground directly. The falling edge of CSL takes the BUSY output and the serial bus out of three-state. The first eight DCLK cycles are used to write to the Control Register via the DIN pin. The Control Register is updated in stages as each bit is clocked in and once the converter has enough information about the following conversion to set the input multiplexer and switches appropriately,

The converter enters the acquisition mode and if required, the internal switches are turned on. During the acquisition mode the reference input data is updated. After the three DCLK cycles of acquisition, the control word is complete (the power management bits are now updated) and the converter enters the conversion mode. At this point the track and hold goes into hold mode and the input signal is sampled and the BUSY output goes high (BUSY will return low on the next falling edge of DCLK). The internal switches may also turn off at this point if in single-ended mode or temperature measurement mode. The next 12 DCLK cycles are used to perform the conversion and to clock out the conversion result. If the conversion is ratiometric (SER/#*DFR* Low), the internal switches are on during the conversion. A thirteenth DCLK cycle is needed to allow the DSP/MCU to clock the LSB in. Three more DCLK cycles will clock out the three trailing zeroes and complete the 24 DCLK transfer. The 24 DCLK cycles may be provided from a DSP or via three bursts of eight clock cycles from a microcontroller.

Control Byte Description

The following diagram shows the typical operation of the HFT012 digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input. The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer, switches, and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the internal switches are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the internal switches may turn off. The next 12th clock cycles accomplish the actual A/D conversion. If the conversion is ratiometric (SER/#DFR Low), the internal switches are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

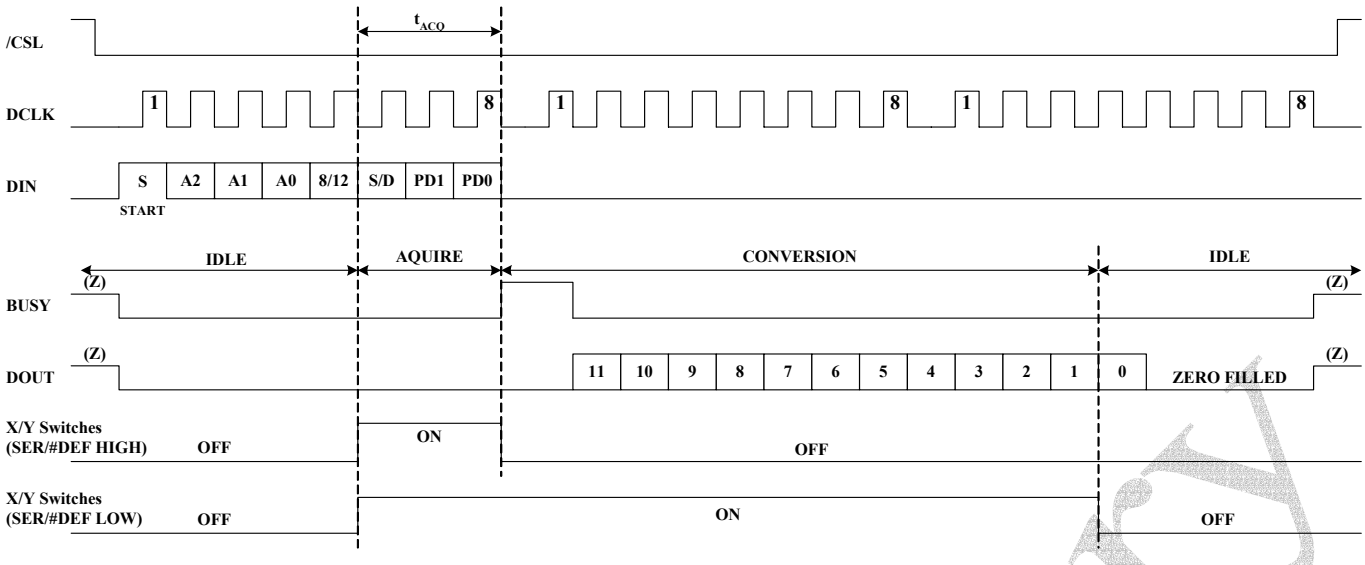


Diagram: Conversion Timing, *24 DCLKS* per Conversion Cycle, 8-bit Bus Interface. No *DCLK* delay required with dedicated series port.

See the above diagram for the placement and order of the control bits within the control byte. The following table gives detailed information about these bits. The first bit, the 'S' bit, must always be "HIGH" and indicates the start of the control byte. The HFT012 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer. The MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH). The SER/#DFR bit controls the reference mode: either single ended (HIGH) or differential (LOW). (The differential mode is also referred to as the ratiometric conversion mode). In single ended mode, the converter's reference voltage is always the difference between the VREF and GND pins. In differential mode, the reference voltage is the difference between the currently enabled switches. The last two bits (PD1-PD0) select the power-down mode. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid. There are two power-down modes: one where PENIRQ is disabled and one where it is enabled.

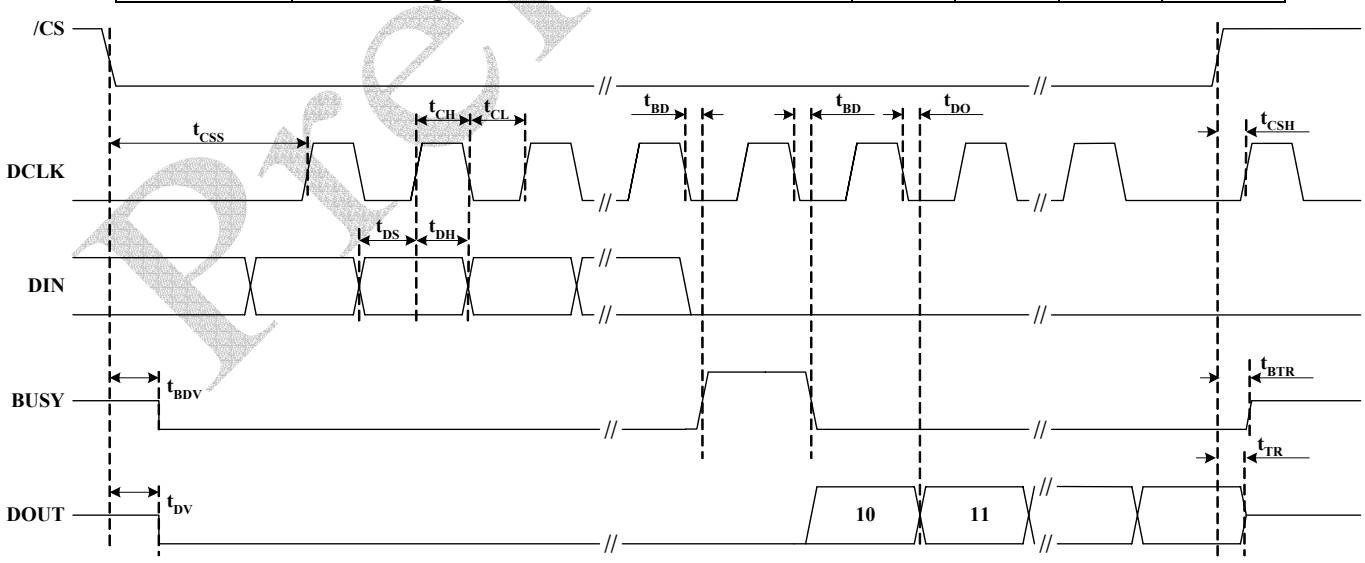
Bits	Name	Description
7	S	Start Bit Control bit starts with first high bit on DIN. A new control byte can start every 16 cycles for 12-bit conversion mode or 12 cycles for 8-bit conversion mode.
6:4	A[2:0]	Measurement Mode Selection Bits [111]: Reserved [110]: Reserved [101]: X Position / Y+ channel input for single-ended mode [100]: Reserved [011]: Reserved [010]: Reserved [001]: Y Position / X+ channel input for single-ended mode [000]: Reserved

Bits	Name	Description
3	8/12	8/12 Bits Output Format Selection Bit [1]: Select 8-bit conversion mode [0]: Select 12-bit conversion mode
2	S/D	Single/Differential Mode Selection Bit [1]: Select single ended reference [0]: Select differential reference
1:0	PD[1:0]	Power Down Control Bits [11]: No power down between conversions [10]: Reserved [01]: Power down between conversions. PENIRQ Disable when power down. [00]: Power down between conversions. PENIRQ enable when power down.

Digital Timing

The following diagram and table provide detailed timing for the digital interface of the HFT012.

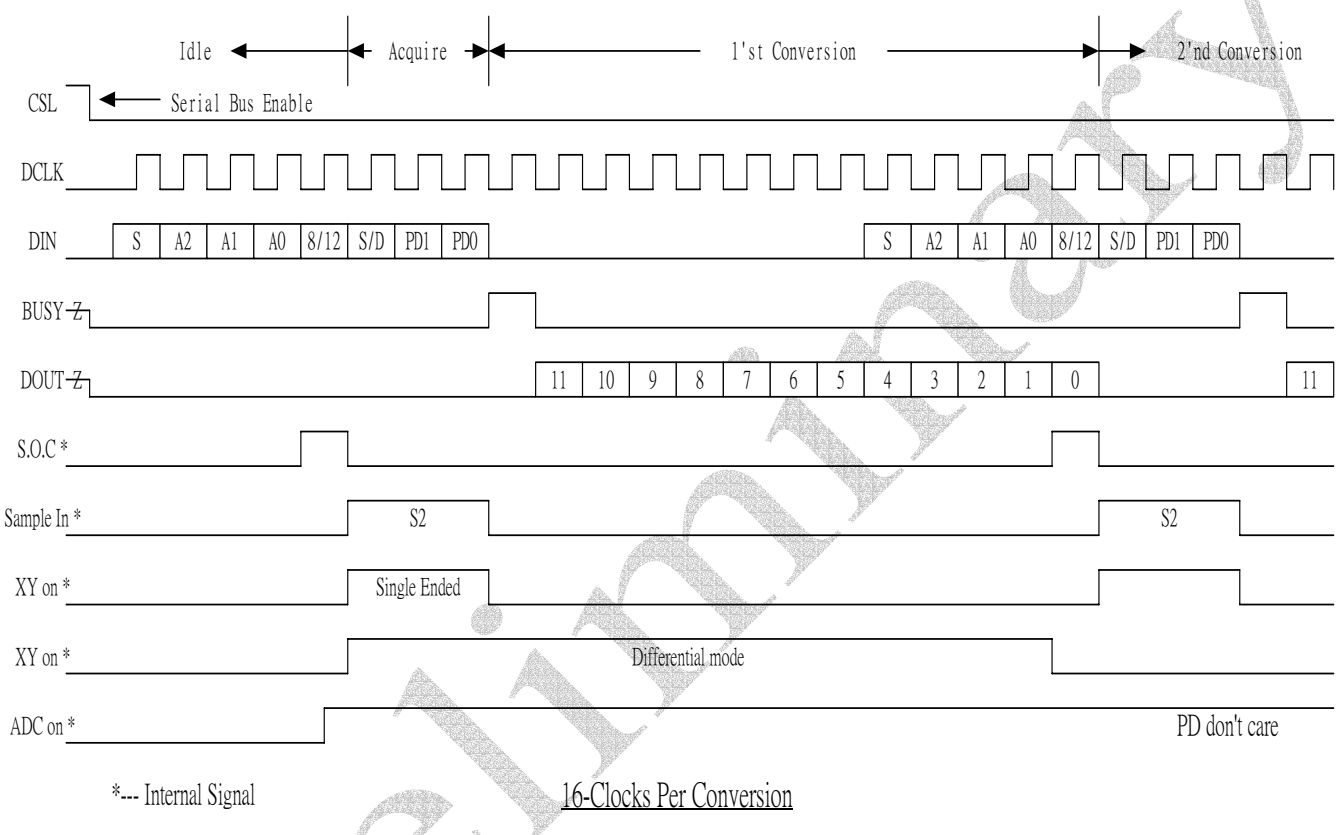
SYMBOL	Description	Min.	Typ.	Max.	Units
t_{ACQ}	Acquisition Time	1.5			μ s
t_{DS}	DIN valid prior to DCLK Rising	100			ns
t_{DH}	DIN Hold after DCLK High	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	/CS Falling to DOUT Enabled			200	ns
t_{TR}	/CS Rising to DOUT Disabled			200	ns
t_{CSS}	/CS Falling to First DCLK Rising	100			ns
t_{CSH}	/CS Rising to DCLK Ignored	0			ns
t_{CH}	DCLK High	200			ns
t_{CL}	DCLK Low	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	/CS Falling to BUSY Enabled			200	ns
T_{BTR}	/CS Rising to BUSY Disabled			200	ns



Detailed Timing Diagram

16 Clocks per Cycle

The control bits for the next conversion can be overlapped with the current conversion to allow for a conversion every 16 DCLK cycles, as shown in following diagram. This timing diagram also allows for the possibility of communication with other serial peripherals between each byte (eight DCLK) transfer between the processor and the converter. However the conversion must complete within a short enough time frames to avoid capacitive droop effects which may distort the conversion result. It should also be noted that the HFT012 will be fully powered while other serial communications may be taking place between byte transfers.



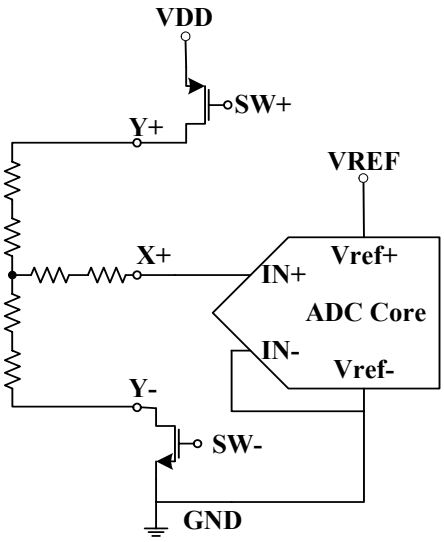
8-Bit Conversion

The HFT012 can be set up to operate in an 8-bit mode rather than 12 bits, by setting the MODE bit in the control register to 1. This mode allows a faster throughput rate to be achieved assuming 8-bit resolution is sufficient. When using the 8-bit mode, a conversion is complete four clock cycles earlier than in the 12-bit mode. This could be used with serial interfaces that provide 12 clock transfers, or two conversions could be completed with three eight-clock transfers. The throughput rate will increase by 25% as a result of the shorter conversion cycle, but the conversion itself can occur at a faster clock rate because the internal settling time of the HFT012 is not as critical, as settling to eight bits is all that is required. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide double the conversion rate.

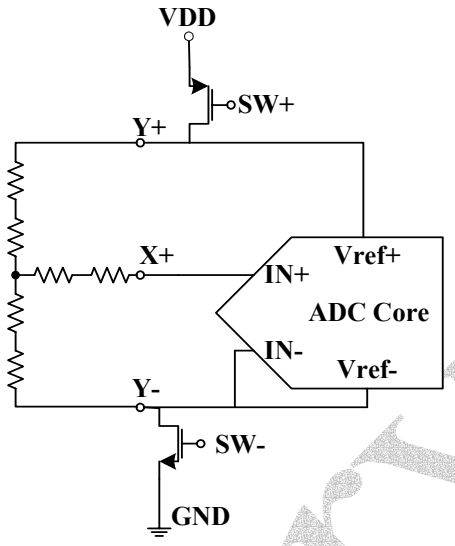
Reference Input

The voltage difference between Vref+ and Vref - (shown in following) sets the analog input range. The HFT012 will operate with a reference in the range of 1V to +VCC. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced.

There is also a critical item regarding the reference when making measurements where the switch drivers are on. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+. For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern). However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error. By setting the SER/DFR bit LOW, the Vref+ and Vref- inputs are connected directly to Y+ and Y–. This makes the A/D conversion ratiometric (difference mode). The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. As a final note about the differential reference mode, it must be used with +VDD as the source of the Vref+ voltage and cannot be used with VREF. It is possible to use a high precision reference on VREF and single-ended reference mode for measurements which do not need to be ratiometric. Or, in some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the HFT012, but they might not be able to supply enough current for the external load (such as a resistive touch screen).



Single-Ended Reference Mode (SER/#*DFR* = 1)



Differential Reference Mode (SER/#*DFR* = 0)

Measurement Modes

There are two measurement modes are available for the HFT012 which are single-ended/differential modes. The differential mode is usually used for touch screen application and the single-ended mode is used for the general measurements, like as temperature, pressure, etc. The selection of modes is through the control bit SER/#DFR, and input channel is selected by the control bits A[2:0].

The input configurations for X/Y drivers and ADC are listed as follow:

A[2:0]	NAME	ADC input	X Driver	Y Driver	Vref+ (Single Ended)	Vref- (Single Ended)
101	X Position (X+ input)	Y+	ON	OFF	X+ (VREF)	X- (GND)
001	Y Position (Y+ input)	X+	OFF	ON	Y+ (VREF)	Y- (GND)

Pen Interrupt

The *PENIRQL* pin is implemented to detect a touch. By connecting a 10k~100k ohms pulled up resistor to VDD. The *PENIRQL* pin output will remain high normally, if *PENIRQL* has been enabled; when the touch screen connected to the HFT012 is touched via a pen or finger, the *PENIRQL* pin output will go low, initiating an interrupt to a microprocessor which may then instruct a control word to be written to the HFT012 to initiate a conversion.

This output can also be enabled between conversions during power-down (PD[1:0]=”00”) allowing power-up to be initiated only when the screen is touched. The result of the first touch screen coordinate conversion after power-up will be valid assuming any external reference is settled to the 12- or 8-bit level as required.

7. Absolute Maximum Rating

Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 6.0V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

8. Recommended Operating Conditions

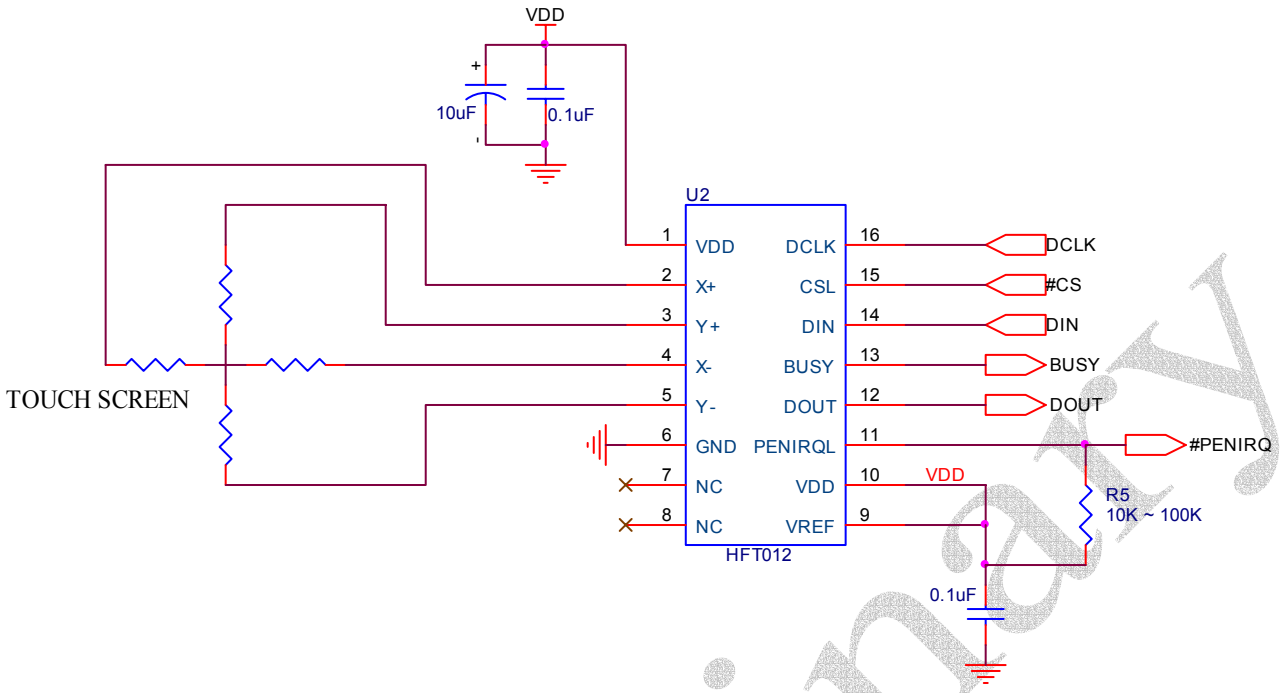
Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ 5.5V	
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

9. AC/DC Characteristics

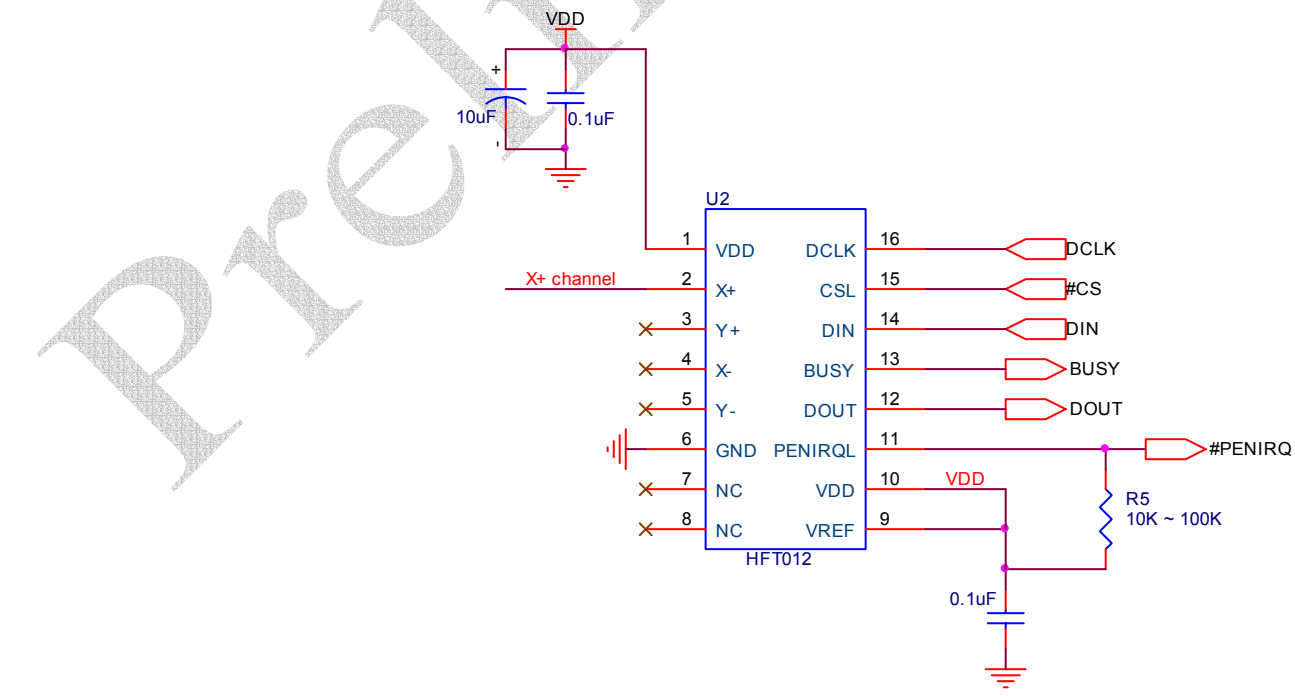
Testing Condition: TEMP=25℃, V_{DD} =3V±10%

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Operation Voltage	V_{DD}	2.4		5.5	V	
Operation Current	I_{OP}		220		μA	
Standby current	I_{STB}			1	μA	
Throughput Rate			125		kSPS	
Input Voltage Ranges		0		VREF	V	
Reference Input Range		1.0		V_{DD}	V	
Resolutions			12		Bits	
No Missing Codes			TBD		Bits	
INL			TBD		LSB	
DNL			TBD		LSB	
Offset Errors			TBD		LSB	
Gain Errors			TBD		LSB	
X+/Y+ Resistance			TBD		Ω	
X-/Y- Resistance			TBD		Ω	
Logical High Output Voltage	V_{OH}		0.8V_{DD}		V	
Logical Low Output Voltage	V_{OL}			0.8	V	
PENIRQL Low Output Voltage	V_{OL}			0.8	V	
Operation Temperature		0		70	℃	

10. Application Circuit



Differential Mode Application



Single-ended Mode Application

11. Updated History

Version	Date	Update History
V0.9	6/18/03	Preliminary version
V1.0	8/18/03	Add the detailed timing diagram.