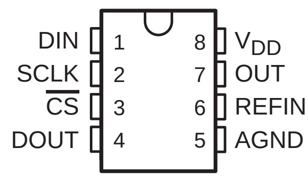
HGC5615 10-BIT DIGITAL-TO-ANALOG CONVERTERS

- **10-Bit CMOS Voltage Output DAC in an 8-Terminal Package**
- **5-V Single Supply Operation**
- **3-Wire Serial Interface**
- **High-Impedance Reference Inputs**
- **Voltage Output Range . . . 2 Times the Reference Input Voltage**
- **Internal Power-On Reset**
- **Low Power Consumption . . . 1.75 mW Max**
- **Update Rate of 1.21 MHz**
- **Settling Time to 0.5 LSB . . . 12.5 µs Typ**
- **Monotonic Over Temperature**
- **Pin Compatible With the Maxim MAX515**

applications

- **Battery-Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

N OR M PACKAGE
(TOP VIEW)



ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
HGC5615IN	DIP8L	C5615I	TUBE	2000pcs/box
HGC5615CN	DIP8L	C5615C	TUBE	2000pcs/box
HGC5615IM/TR	SOP8L	C5615I	REEL	2500pcs/reel
HGC5615CM/TR	SOP8L	C5615C	REEL	2500pcs/reel

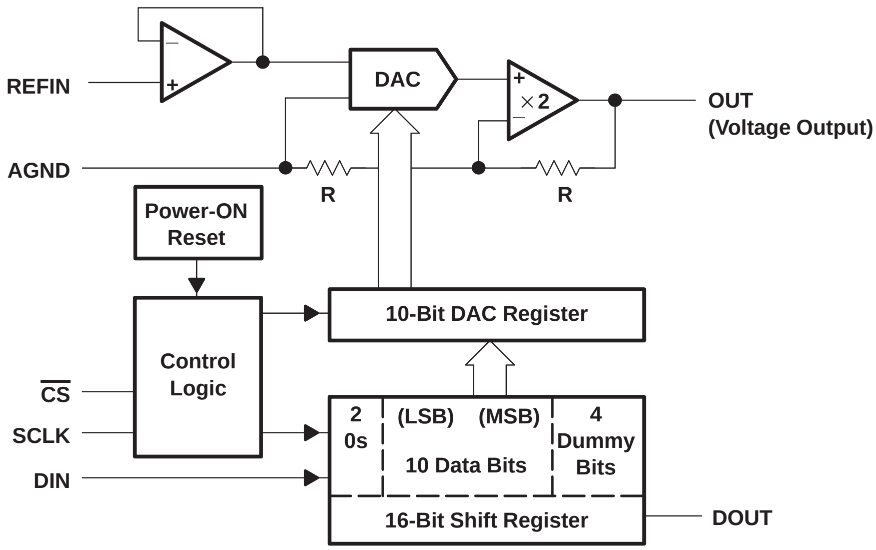
description

The HGC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5 V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the HGC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The HGC5615C is characterized for operation from 0°C to 70°C. The HGC5615I is characterized for operation from –40°C to 85°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
$\overline{CS}$	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V_{DD}	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . 7 V
Digital input voltage range to AGND . . . – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range to AGND . . . – 0.3 V to V_{DD} + 0.3 V
Output voltage at OUT from external source . . . V_{DD} + 0.3 V
Continuous current at any terminal . . . ±20 mA
Operating free-air temperature range, T_A: HGC5615C . . . 0°C to 70°C
HGC5615I . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	$V_{DD}-2$	V
Load resistance, R_L		2			kΩ
Operating free-air temperature, T_A	HGC5615C	0		70	°C
	HGC5615I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\ V \pm 5\%$, $V_{ref} = 2.048\ V$ (unless otherwise noted)

static DAC specifications

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10			bits
	Integral nonlinearity, end point adjusted (INL)		V_{ref} = 2.048 V, See Note 1			±1	LSB
	Differential nonlinearity (DNL)		V_{ref} = 2.048 V, See Note 2		±0.1	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		V_{ref} = 2.048 V, See Note 3			±3	LSB
	Zero-scale-error temperature coefficient		V_{ref} = 2.048 V, See Note 4		3		ppm/°C
E_G	Gain error		V_{ref} = 2.048 V, See Note 5			±3	LSB
	Gain-error temperature coefficient		V_{ref} = 2.048 V, See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See Notes 7 and 8	80			dB
		Gain		80			
	Analog full scale output		R_L = 100 kΩ		$2V_{ref}(1023/1024)$		V

NOTES:
1. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).
2. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).
4. Zero-scale-error temperature coefficient is given by: $E_{ZS}\ TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
5. Gain error is the deviation from the ideal output (V_{ref} – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-scale error.
6. Gain temperature coefficient is given by: $E_G\ TC = [E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
7. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

voltage output (OUT)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ	0		V_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 2 V, R_L = 2 kΩ			0.5	LSB
I_{OSC}	Output short circuit current	OUT to V_{DD} or AGND		20		mA
$V_{OL(low)}$	Output voltage, low-level	$I_{O(OUT)} \le 5$ mA			0.25	V
$V_{OH(high)}$	Output voltage, high-level	$I_{O(OUT)} \le -5$ mA	4.75			V

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted) (continued)

reference input (REFIN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		0		V_{DD}−2	V
r_i	Input resistance		10			MΩ
C_i	Input capacitance			5		pF

digital inputs (DIN, SCLK, $\overline{CS}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level digital input voltage		2.4			V
V_{IL}	Low-level digital input voltage				0.8	V
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±1	µA
I_{IL}	Low-level digital input current	$V_I = 0$			±1	µA
C_i	Input capacitance			8		pF

digital output (DOUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage, high-level	I_O = –2 mA	V_{DD}–1			V
V_{OL}	Output voltage, low-level	I_O = 2 mA			0.4	V

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	V_{ref} = 0		150	250	µA
		V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	V_{ref} = 2.048 V		230	350	µA

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, S/(N+D)	V_{ref} = 1 V_{pp} at 1 kHz + 2.048 Vdc, code = 11 1111 1111, See Note 9	60			dB

NOTE 9: The limiting frequency value at 1 Vpp is determined by the output-amplifier slew rate.

digital input timing requirements (see Figure 1)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK high	45			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK high	0			ns
$t_{su(CSS)}$	Setup time, $\overline{CS}$ low to SCLK high	1			ns
$t_{su(CS1)}$	Setup time, $\overline{CS}$ high to SCLK high	50			ns
$t_{h(CSH0)}$	Hold time, SCLK low to $\overline{CS}$ low	1			ns
$t_{h(CSH1)}$	Hold time, SCLK low to $\overline{CS}$ high	0			ns
$t_{w(CS)}$	Pulse duration, minimum chip select pulse width high	20			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns

output switching characteristic

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd(DOUT)}$	Propagation delay time, DOUT	C_L = 50 pF			50	ns

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Output slew rate	C_L = 100 pF, T_A = 25°C	R_L = 10 kΩ,	0.3	0.5		V/μs
t_s	Output settling time	To 0.5 LSB, R_L = 10 kΩ,	C_L = 100 pF, See Note 10		12.5		μs
	Glitch energy	DIN = All 0s to all 1s			5		nV•s

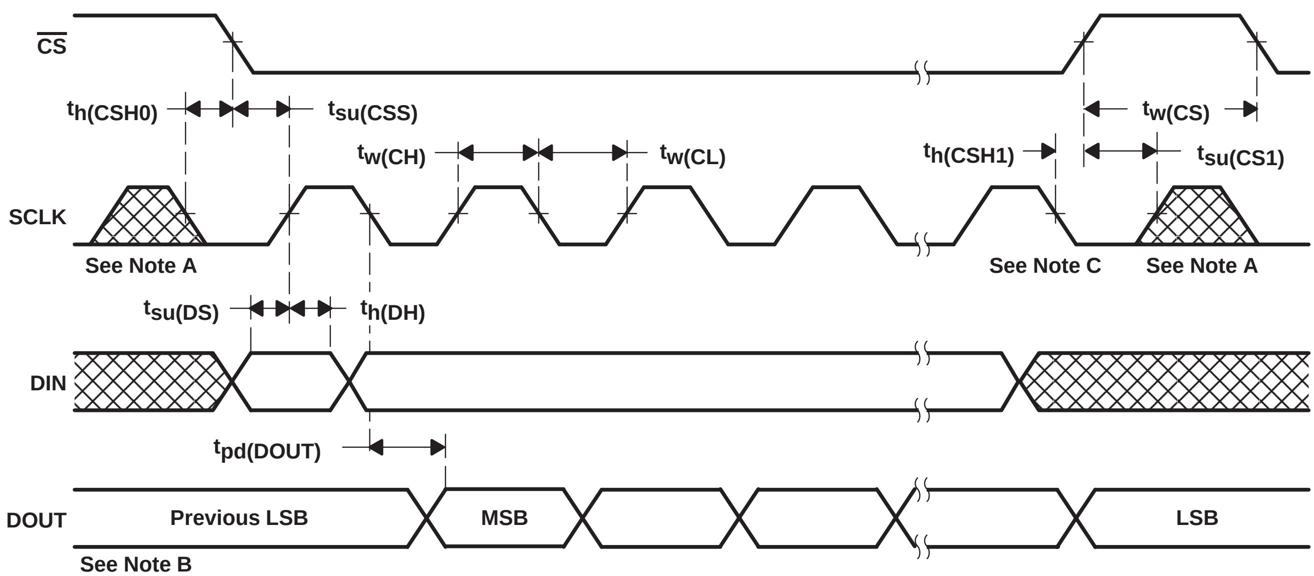
NOTE 10: Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

reference input (REFIN)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference feedthrough	REFIN = 1 V_{pp} at 1 kHz + 2.048 Vdc (see Note 11)			–80		dB
Reference input bandwidth (f–3dB)	REFIN = 0.2 V_{pp} + 2.048 Vdc	REFIN = 0.2 V_{pp} + 2.048 Vdc		30		kHz

NOTE 11: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = 2.048 Vdc + 1 V_{pp} at 1 kHz.

PARAMETER MEASUREMENT INFORMATION



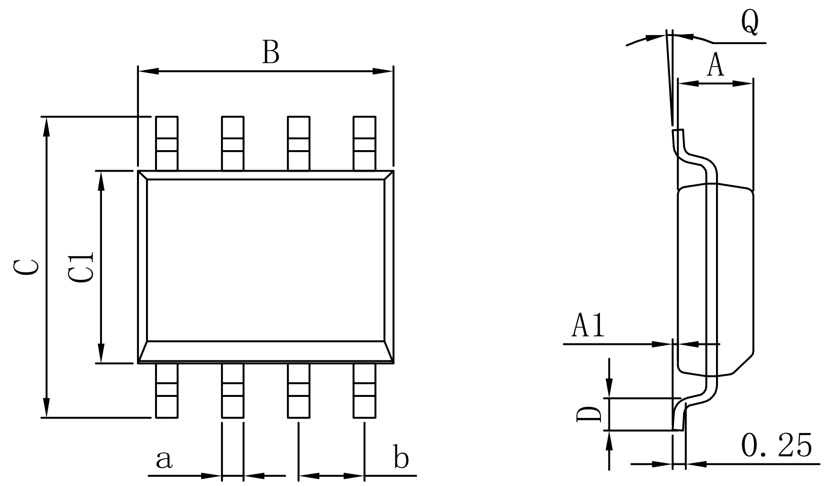
NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.

B. Data input from preceeding conversion cycle.

C. Sixteenth SCLK falling edge

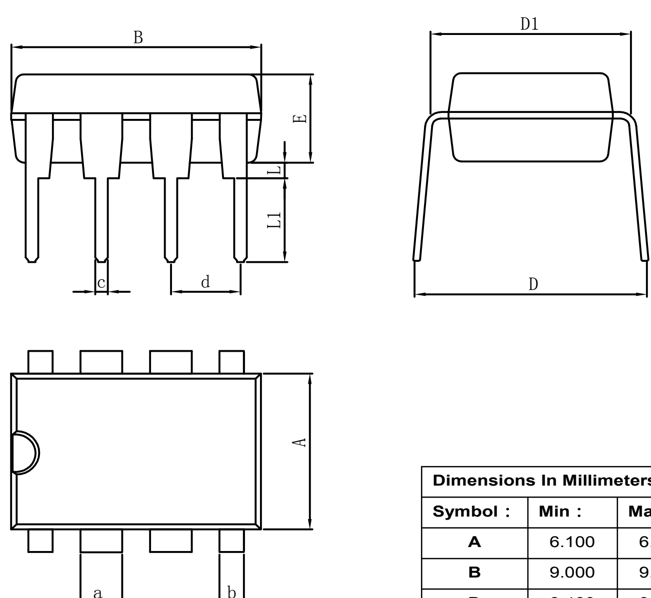
PACKAGE

SOP8



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	1.225	1.570	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	4.800	5.100	**a**	0.420 TYP	
C	5.800	6.250	**b**	1.270 TYP	
C1	3.800	4.000			

DIP8



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	6.100	6.680	**L1**	3.000	3.600
B	9.000	9.500	**a**	1.524 TYP	
D	8.400	9.000	**b**	0.889 TYP	
D1	7.420	7.820	**c**	0.457 TYP	
E	3.100	3.550	**d**	2.540 TYP	
L	0.500	0.700			

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