

HI-524

4-Channel Wideband and Video Multiplexer

FN3148  
Rev 3.00  
April 2002

The HI-524 is a 4-Channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

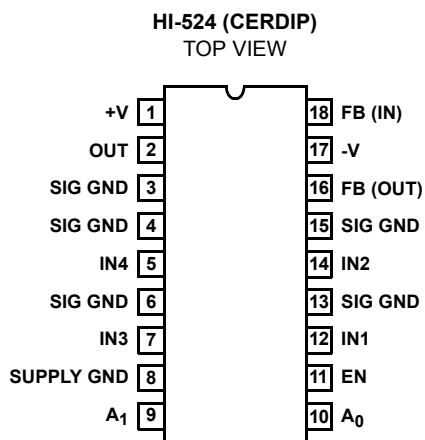
The HI-524 is designed to operate into a wideband buffer amplifier such as the Intersil HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel ON resistance, to minimize the amplifier  $V_{OS}$  and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE      | PKG. NO. |
|-------------|------------------|--------------|----------|
| HI1-0524-5  | 0 to 75          | 18 Ld CERDIP | F18.3    |

Pinout



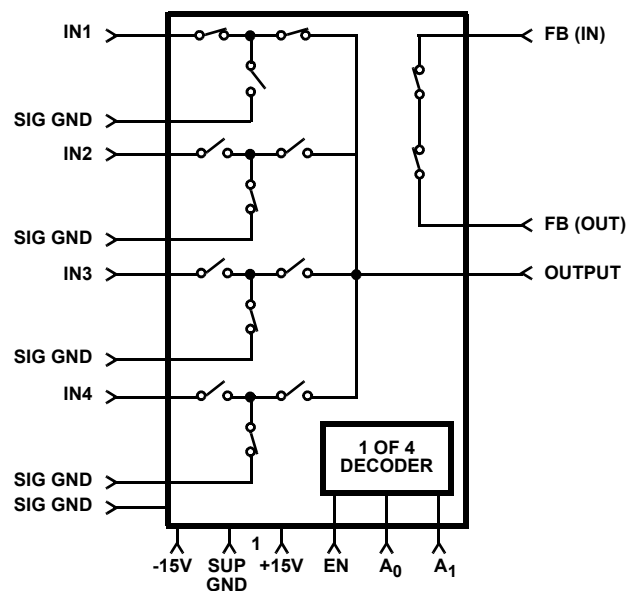
Features

- Crosstalk (10MHz) ..... < -60dB
- Fast Access Time ..... 150ns
- Fast Settling Time ..... 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Functional Diagram



TRUTH TABLE

| A <sub>1</sub> | A <sub>0</sub> | EN | ON CHANNEL |
|----------------|----------------|----|------------|
| X              | X              | L  | None       |
| L              | L              | H  | 1 (Note)   |
| L              | H              | H  | 2          |
| H              | L              | H  | 3          |
| H              | H              | H  | 4          |

NOTE: Channel 1 is shown selected in the Functional Diagram.

**Absolute Maximum Ratings**

|  |                      |
|--|----------------------|
| V+ to V-                                   | 33V                  |
| Digital Input Voltage ( $V_{EN}$ , $V_A$ ) | -6V to +6V           |
| Analog Signal ( $V_{IN}$ , $V_{OUT}$ )     | (V-) -2V to (V+) +2V |
| Either Supply to Ground                    | 16.5V                |

**Operating Conditions**

|                   |             |
|-------------------|-------------|
| Temperature Range | 0°C to 75°C |
|-------------------|-------------|

**Thermal Information**

|   |                      |                      |
|---|----------------------|----------------------|
| Thermal Resistance (Typical, Note 1)      | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
| CERDIP Package                            | 75                   | 20                   |
| Maximum Junction Temperature              |                      |                      |
| Ceramic Package                           | 175°C                |                      |
| Maximum Storage Temperature               | -65°C to 150°C       |                      |
| Maximum Lead Temperature (Soldering, 10s) | 300°C                |                      |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications** Supplies = +15V, -15V;  $V_{AH}$  (Logic Level High) = 2.4V,  $V_{AL}$  (Logic Level Low) = 0.5V;  $V_{EN}$  = 2.4V, Unless Otherwise Specified

| PARAMETER                                | TEST CONDITIONS   | TEMP (°C) | -5  |      |     | UNITS      |
|--|-------------------|-----------|-----|------|-----|------------|
|  |                   |           | MIN | TYP  | MAX |            |
| <b>DYNAMIC CHARACTERISTICS</b>           |                   |           |     |      |     |            |
| Access Time, $t_A$                       | Note 5            | 25        | -   | 150  | 300 | ns         |
| Break-Before-Make Delay, $t_{OPEN}$      | Note 5            | 25        | -   | 20   | -   | ns         |
| Enable Delay (ON), $t_{ON}$ (EN)         | $R_L = 500\Omega$ | 25        | -   | 180  | -   | ns         |
| Enable Delay (OFF), $t_{OFF}$ (EN)       | $R_L = 500\Omega$ | 25        | -   | 180  | -   | ns         |
| Settling Time (Note 5)                   | To 0.1%           | 25        | -   | 200  | -   | ns         |
|  | To 0.01%          | 25        | -   | 600  | -   | ns         |
| Crosstalk                                | Note 6            | 25        | -   | -65  | -   | dB         |
| Channel Input Capacitance, $C_{S(OFF)}$  |                   | 25        | -   | 4    | -   | pF         |
| Channel Output Capacitance, $C_{D(OFF)}$ |                   | 25        | -   | 10   | -   | pF         |
| Digital Input Capacitance, $C_A$         |                   | 25        | -   | 5    | -   | pF         |
| <b>DIGITAL INPUT SPECIFICATIONS</b>      |                   |           |     |      |     |            |
| Input Low Threshold (TTL), $V_{AL}$      |                   | Full      | -   | -    | 0.8 | V          |
| Input High Threshold (TTL), $V_{AH}$     |                   | Full      | 2.4 | -    | -   | V          |
| Input Leakage Current (High), $I_{AH}$   |                   | Full      | -   | 0.05 | 1   | $\mu$ A    |
| Input Leakage Current (Low), $I_{AL}$    |                   | Full      | -   | -    | 25  | $\mu$ A    |
| <b>ANALOG CHANNEL SPECIFICATIONS</b>     |                   |           |     |      |     |            |
| Analog Signal Range, $V_{IN}$            |                   | Full      | -10 | -    | +10 | V          |
| On Resistance, $r_{ON}$                  | Note 2            | 25        | -   | 700  | -   | $\Omega$   |
|  |                   | Full      | -   | -    | 1.5 | k $\Omega$ |
| Off Input Leakage Current, $I_{S(OFF)}$  | Note 3            | 25        | -   | 0.2  | -   | nA         |
|  |                   | Full      | -   | -    | 50  | nA         |
| Off Output Leakage Current, $I_{D(OFF)}$ | Note 3            | 25        | -   | 0.2  | -   | nA         |
|  |                   | Full      | -   | -    | 50  | nA         |
| On Channel Leakage Current, $I_{D(ON)}$  | Note 3            | 25        | -   | 0.7  | -   | nA         |
|  |                   | Full      | -   | -    | 50  | nA         |
| -3dB Bandwidth                           | Note 4            | 25        | -   | 8    | -   | MHz        |

**Electrical Specifications** Supplies = +15V, -15V;  $V_{AH}$  (Logic Level High) = 2.4V,  $V_{AL}$  (Logic Level Low) = 0.5V;  $V_{EN}$  = 2.4V, Unless Otherwise Specified **(Continued)**

| PARAMETER                           | TEST CONDITIONS | TEMP (°C) | -5  |     |     | UNITS |
|-------------------------------------|-----------------|-----------|-----|-----|-----|-------|
|                                     |                 |           | MIN | TYP | MAX |       |
| <b>POWER SUPPLY CHARACTERISTICS</b> |                 |           |     |     |     |       |
| Power Dissipation, $P_D$            |                 | Full      | -   | -   | 750 | mW    |
| Current, $I_+$                      | Note 7          | Full      | -   | -   | 25  | mA    |
| Current, $I_-$                      | Note 7          | Full      | -   | -   | 25  | mA    |

NOTES:

- $V_{IN} = 0V$ ;  $I_{OUT} = 100\mu A$  (See Test Circuit section).
- $V_O = \pm 10V$ ;  $V_{IN} = \pm 10V$ . (See Test Circuit section).
- MUX output is buffered with HA-5033 amplifier.
- 6V Step,  $\pm 3V$  to  $\mp 3V$ , See Test Circuit section.
- $V_{IN} = 10MHz$ ,  $3V_{P-P}$  on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with  $75\Omega$ .
- Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

**Test Circuits and Waveforms**  $T_A = 25^\circ C$ ,  $V_{SUPPLY} = \pm 15V$ ,  $V_{AH} = 2.4V$ ,  $V_{AL} = 0.8V$ , Unless Otherwise Specified

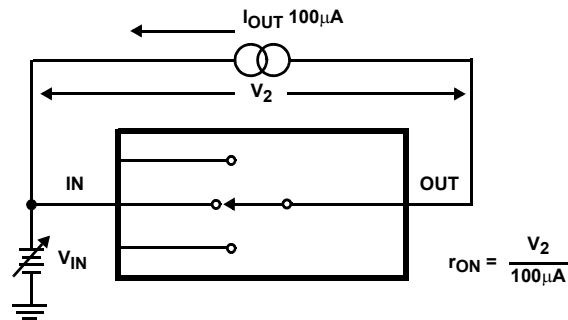


FIGURE 1A. TEST CIRCUIT

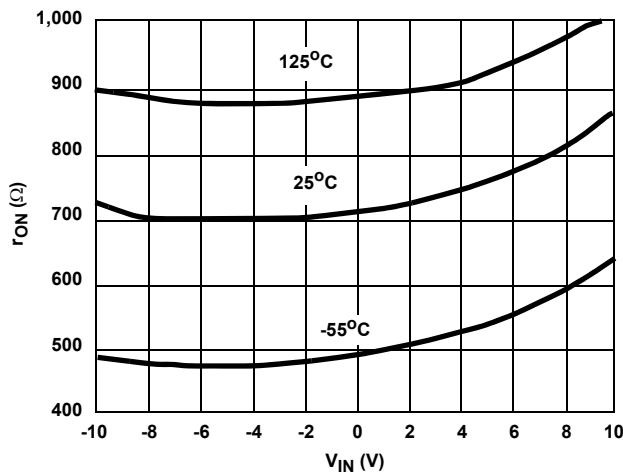


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

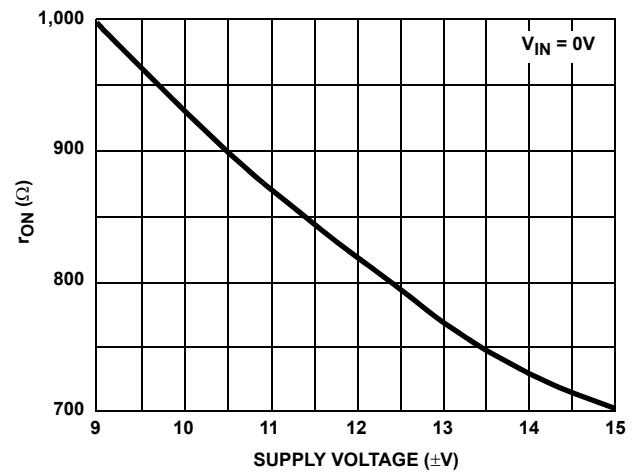


FIGURE 1C. ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

**Test Circuits and Waveforms**  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = 2.4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$ , Unless Otherwise Specified (Continued)

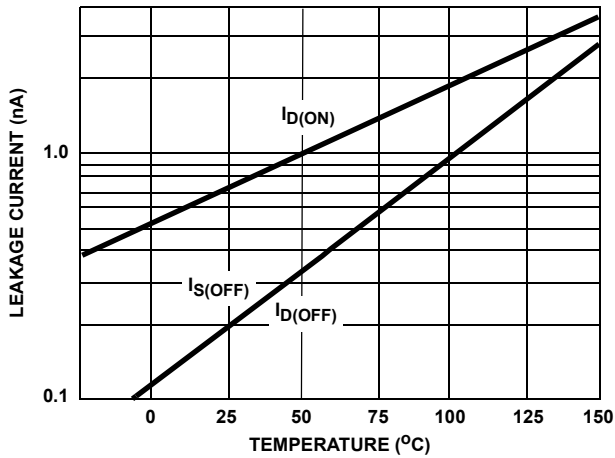


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

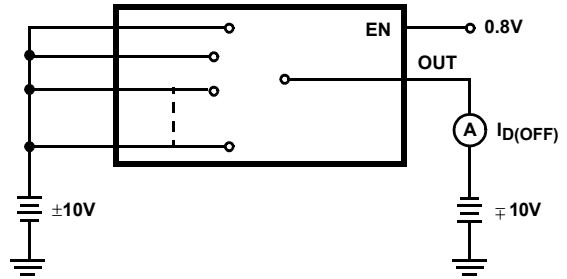


FIGURE 2B.  $I_{D(OFF)}$  TEST CIRCUIT (NOTE 8)

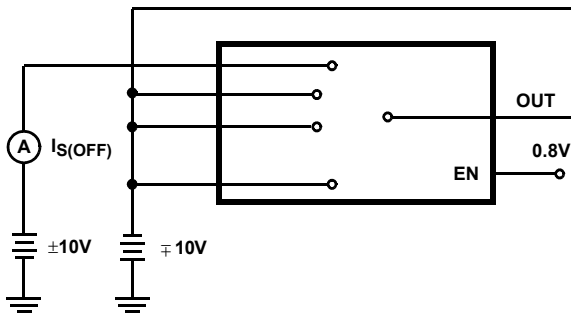


FIGURE 2C.  $I_{S(OFF)}$  TEST CIRCUIT (NOTE 8)

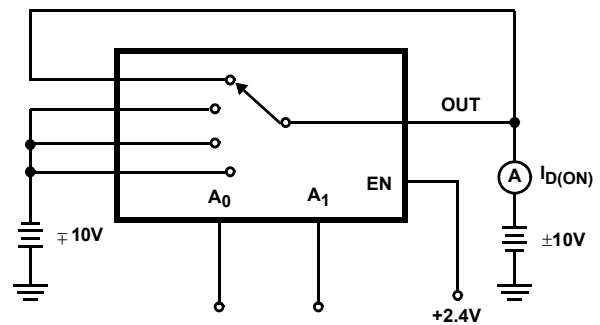


FIGURE 2D.  $I_{D(ON)}$  TEST CIRCUIT (NOTE 8)

FIGURE 2. LEAKAGE CURRENTS

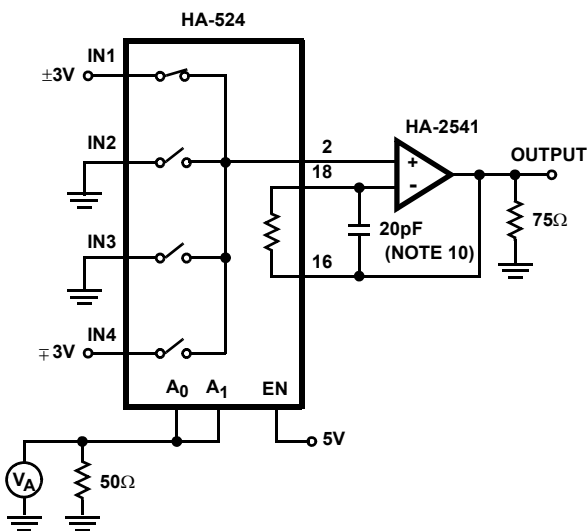


FIGURE 3A. TEST CIRCUIT

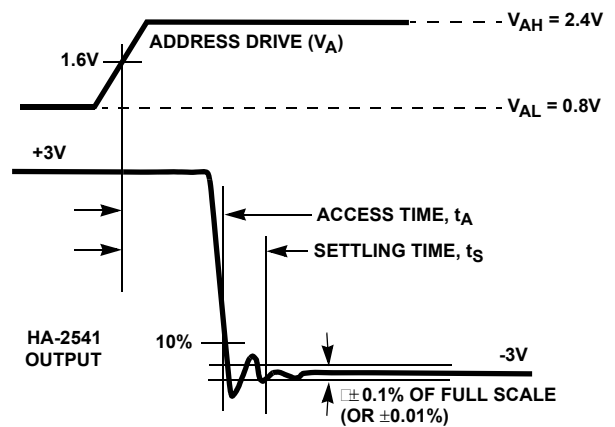


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. SETTLING TIME, ACCESS TIME, BREAK-BEFORE-MAKE DELAY (NOTE 9)

NOTES:

8. Two measurements per channel:  $\pm 10\text{V}$  and  $\mp 10\text{V}$ . (Two measurements per device for  $I_{D(OFF)} \pm 10\text{V}$  and  $\mp 10\text{V}$ .)
9. The Break-Before-Make test requires inputs 1 and 4 at the same voltage.
10. Capacitor value may be selected to optimize AC performance.

**Test Circuits and Waveforms**  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = 2.4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$ , Unless Otherwise Specified (Continued)

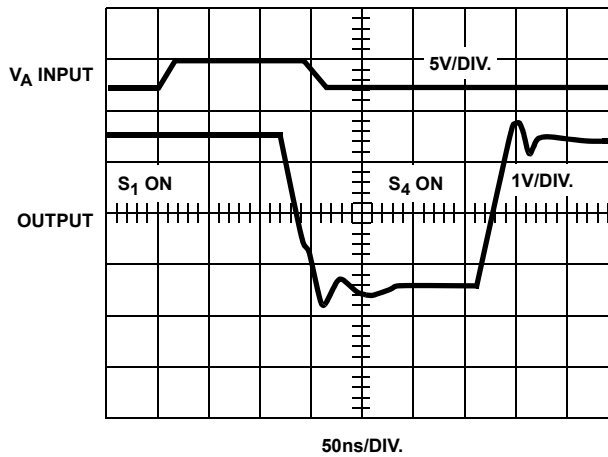
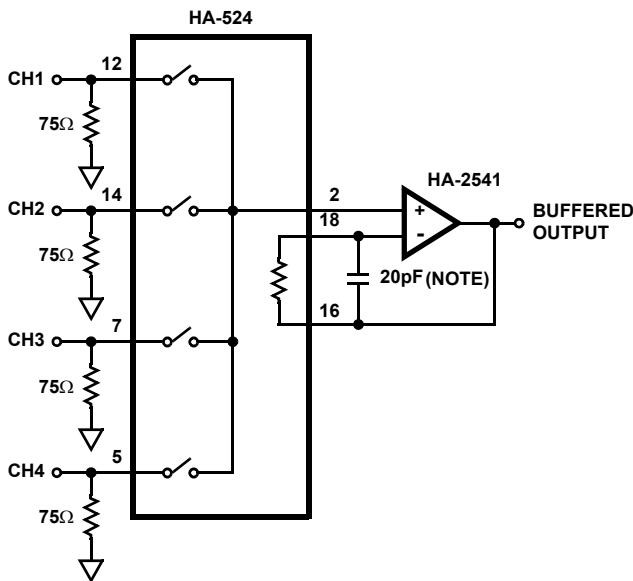


FIGURE 4. ACCESS TIME WAVEFORMS

**Application Information**

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel “ON” resistance:



NOTE: Capacitor value may be selected to optimize AC performance.

FIGURE 5.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus  $\pm 100\text{mA}$  output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to  $\pm 0.1\%$ ) and  $\pm 10\text{V}$  output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel “ON” resistance, to minimize offset voltage due to the buffer’s bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for  $V_{\text{EN}} = \text{Low}$ . This allows two or more HI-524s to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 pins labeled ‘SIG GND’ (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors ( $0.1\mu\text{F}$  to  $1\mu\text{F}$ ) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately  $160\Omega$  for an input of  $-3\text{V}$ .) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

## Die Characteristics

### DIE DIMENSIONS:

2250μm x 3720μm x 485μm

### METALLIZATION:

Type: CuAl  
 Thickness: 16kÅ ±2kÅ

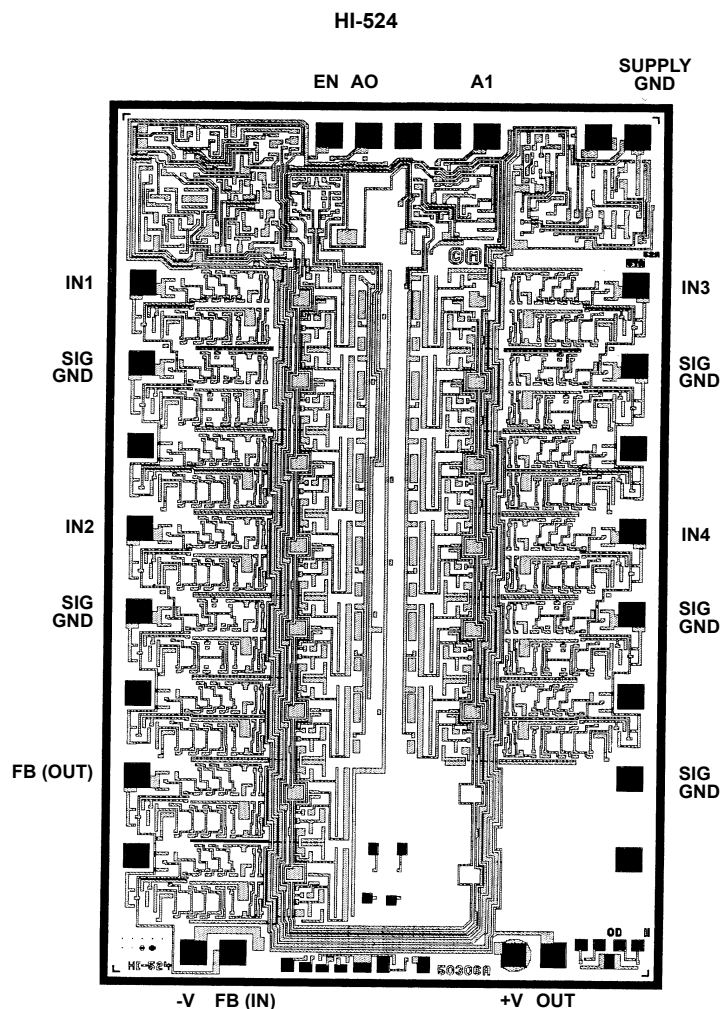
### PASSIVATION:

Type: Nitride Over Silox  
 Nitride Thickness: 3.5kÅ ±1kÅ  
 Silox Thickness: 12kÅ ±2kÅ

### WORST CASE CURRENT DENSITY:

1.58 x 10<sup>5</sup> A/cm<sup>2</sup>

## Metallization Mask Layout



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