HOLT INTEGRATED CIRCUITS INC.

HI-8437

32-Channel High Impedance Low Threshold Sensor with SPI Interface

January 2016

GENERAL DESCRIPTION

The HI-8437 is a 32-channel high impedance discrete-to-digital sensor fabricated with Silicon-on-Insulator (SOI) technology designed to interface with a Serial Peripheral Interface (SPI).

The four banks of 8 sense inputs can be programmed to detect one of two threshold ranges, VTHR1, VTHR2.

All sense inputs have a 400KΩ resistor to ground and are internally lightning protected to DO160G, Section 22, Cat AZ, BZ and ZZ without external components.

The sensing circuit window comparator thresholds are set by programming the center threshold and hysteresis registers to values from 0.4V to 5.2V. The digital values of the sensed inputs can be read either one bank at a time or all 4 banks with one command.

Interface to the digital subsystem is simple CMOS logic inputs and outputs. The logic pins are compatible with 3.3V logic allowing direct connection to a wide range of microcontrollers or FPGAs.

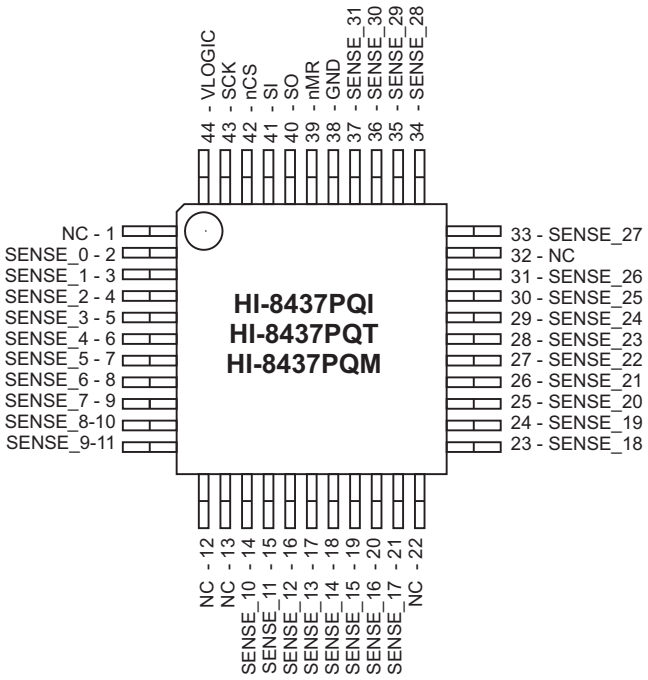
FEATURES

- Robust CMOS Silicon-on-Insulator (SOI) technology
- 32-channel Programmable Sense Operation, two programmable threshold ranges, 4 X 8 Input Sensors
- Programmable HI/LO Threshold and Hysteresis in 0.1V steps, from 0.4V to 5.2V.
- Single Low Voltage Supply Operation
- Logic Operation from 3.0V to 3.6V
- 20 MHz Serial Peripheral Interface (SPI)
- Lightning Protected Sense Inputs
- Internal Self-Test

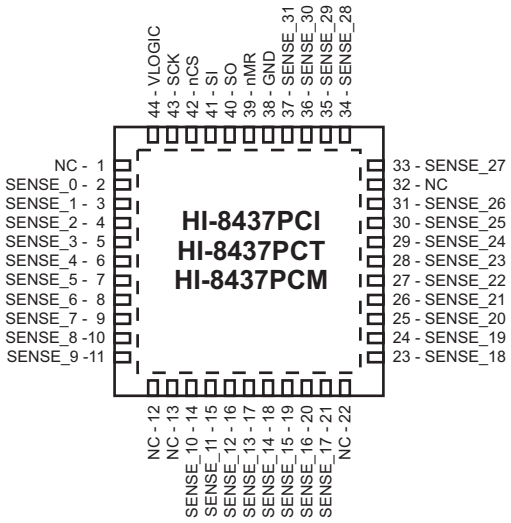
APPLICATION

- Avionics Discrete to Digital Sensing
- Low thresholds applications.

PIN CONFIGURATIONS



44 Pin Plastic Quad Flat Pack (PQFP)
10mm x 10mm



44 Pin Plastic QFN
7mm x 7mm

BLOCK DIAGRAM

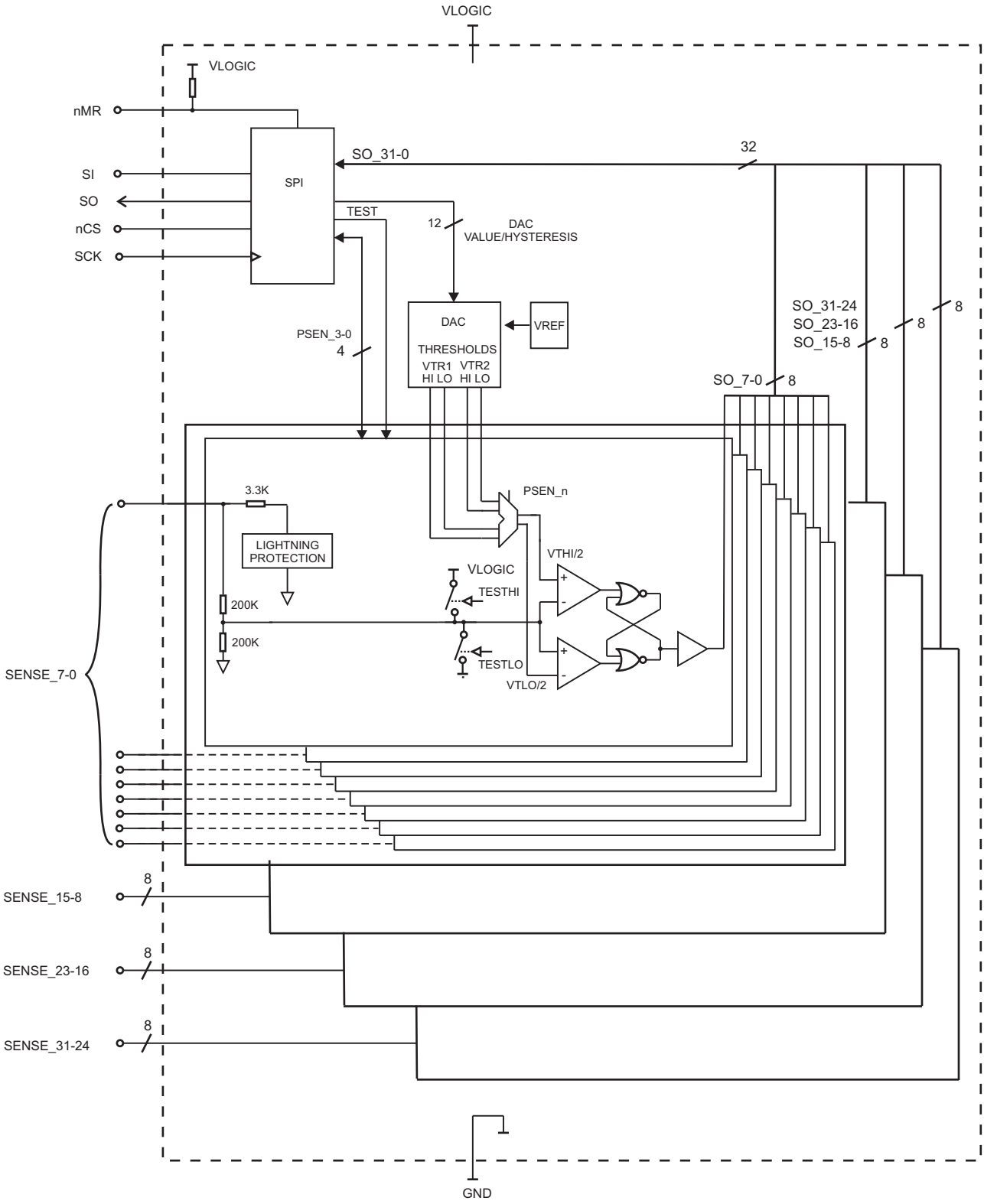


Figure 2.

PIN DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION
VLOGIC	Supply	3.3V Power Supply for both sensors and logic.
SENSE<31:0>	Discrete Input	4 banks of 8 discrete inputs programmable through the SPI to either Threshold Range 1, VTR1 or Threshold Range 2, VTR2. The type of input is programmed by bank, PSEN<3:0> bits. “0” makes the bank VTR1 sensors, “1” makes the bank VTR2 sensors. The status of the inputs SENSE<31:0> are stored in SO<31:0> See SPI section for programming and reading sensors.
GND	Supply	0V Ground for Sensor and Logic.
SCK	Digital Input	SPI Clock.
nCS	Digital Input	SPI Chip Select, Active Low, internal 30KΩ pull-up.
SI	Digital Input	SPI serial data input, internal 30KΩ pull-down.
SO	Digital Output	SPI serial data output.
nMR	Digital Input	Master Reset, Active Low, internal 30KΩ pull-up.

Table 1.

SPI COMMANDS

OP Code	R/W	# Data Bytes	DESCRIPTION
0x02	W	1	Write Control Register
0x04	W	1	Write Program Sense Banks Register, PSEN<3:0>, to program SENSE Inputs
0x3A	W	2	Write VTR1 Threshold Center Value and Hysteresis
0x3C	W	2	Write VTR2 Threshold Center Value and Hysteresis
0x1E	W	1	Write Test Mode Data Register
0x82	R	1	Read Control Register
0x84	R	1	Read Program Sense Banks Register, to read programmed bank type
0xBA	R	2	Read VTR1 Threshold Center Value and Hysteresis
0xBC	R	2	Read VTR2 Threshold Center Value and Hysteresis
0x9E	R	1	Read Test Mode Data Register
0x90	R	1	Read Bank 0, SOUT Register, SO<7:0>, status of SENSE<7:0> Inputs
0x92	R	1	Read Bank 1, SOUT Register, SO<15:8>, status of SENSE<15:8> Inputs
0x94	R	1	Read Bank 2, SOUT Register, SO<23:16>, status of SENSE<23:16> Inputs
0x96	R	1	Read Bank 3, SOUT Register, SO<31:24>, status of SENSE<31:24> Inputs
0xF8	R	4	Read All Banks, SOUT Register, SO<31:0>, status of SENSE<31:0> Inputs

Table 2.

SERIAL PERIPHERAL INTERFACE (SPI)

SPI BASICS

The HI-8437 uses a SPI (Serial Peripheral Interface) for host access to internal registers which program the chip and store sensor status. Host serial communication is enabled through the active low, Chip Select (nCS) pin, and is accessed via a four-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host, the Serial Clock (SCK) and the nCS. All read / write cycles are completely self-timed.

The SPI protocol specifies master and slave operation; the HI-8437 operates as a SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". Without describing details of the SPI modes, the HI-8437 operates in Mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 0, CPOL = 0). The host SPI logic must be set for Mode 0 for proper communications with the HI-8437.

As seen in Figure 3, SPI Mode 0 holds SCK in the low state when idle. The SPI protocol transfers serial data in 8-bit bytes. Once nCS is asserted, the rising edge of SCK shifts the input data into the master and slave devices, starting with each byte's most-significant bit. A rising edge on nCS completes the serial transfer and re-initializes the HI-8437 SPI for the next transfer. If nCS goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

In the general case, both master and slave simultaneously send and receive serial data (full duplex), per Figure 3 below. However the HI-8437 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-8437 is sending data on SO during read operations, activity on its SI input is ignored. The host likewise ignores its SI input activity while transmitting to the HI-8437.

HI-8437 SPI INSTRUCTIONS

The SPI Instructions used to read, write and configure the HI-8437 consist of an opcode and data bytes. Each SPI instruction begins with an 8-bit opcode with the format shown below. The most significant bit (MSB) specifies whether the instruction is a write, "0", or a read, "1", transfer.

When nCS goes low, the first 8 rising edges of the SCK shift the op code into the decoder register, MSB first. The SPI can be clocked up to 20 MHz.

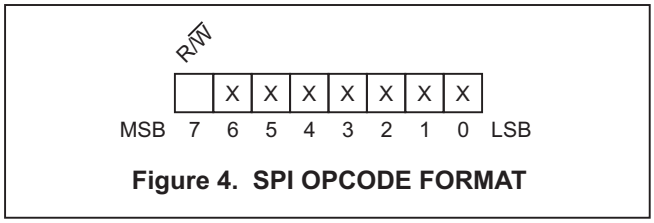


Figure 4. SPI OPCODE FORMAT

For write instructions, the next 8 rising SCK edges shift a data byte into the buffer register. The specific instruction register is loaded on the 8th rising SCK edge. This sequence is repeated until the required number of data bytes for the instruction are written.

For read instructions, the most significant bit of the requested data word appears at the SO pin at the next falling SCK edge after the last op code bit is clocked into the decoder. As in write instructions, the number of data bytes varies with the read instruction. SO data changes on the falling SCK edges.

Figure 5 to Figure 7 show read and write timing for single-byte, dual-byte and four byte register operations. The instruction op code is immediately followed by data bytes comprising the 8-bit data bytes read or written. For a register read or write, nCS is negated after all data bytes are transferred.

Table 2 summarizes the HI-8437 SPI instruction set.

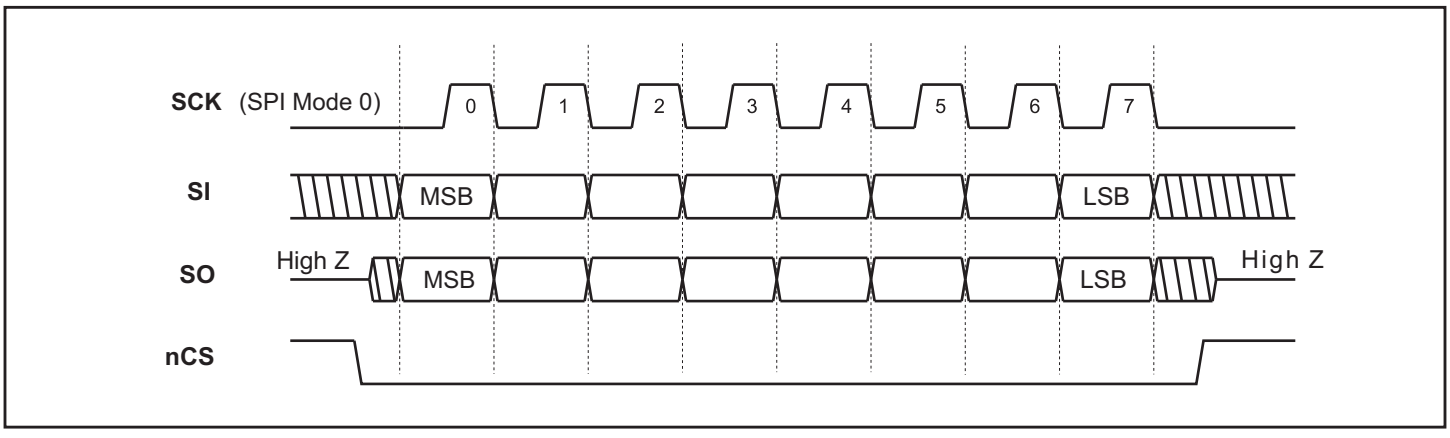


FIGURE 3. Generalized Single-Byte Transfer Using SPI Protocol Mode 0

Note: SPI Instruction op-codes not shown in Table 2 are "reserved" and must not be used. Further, these op-codes will not provide meaningful data in response to a read instruction.

Two instruction bytes cannot be "chained"; nCS must be negated after each instruction, and then reasserted for the following Read or Write instruction.

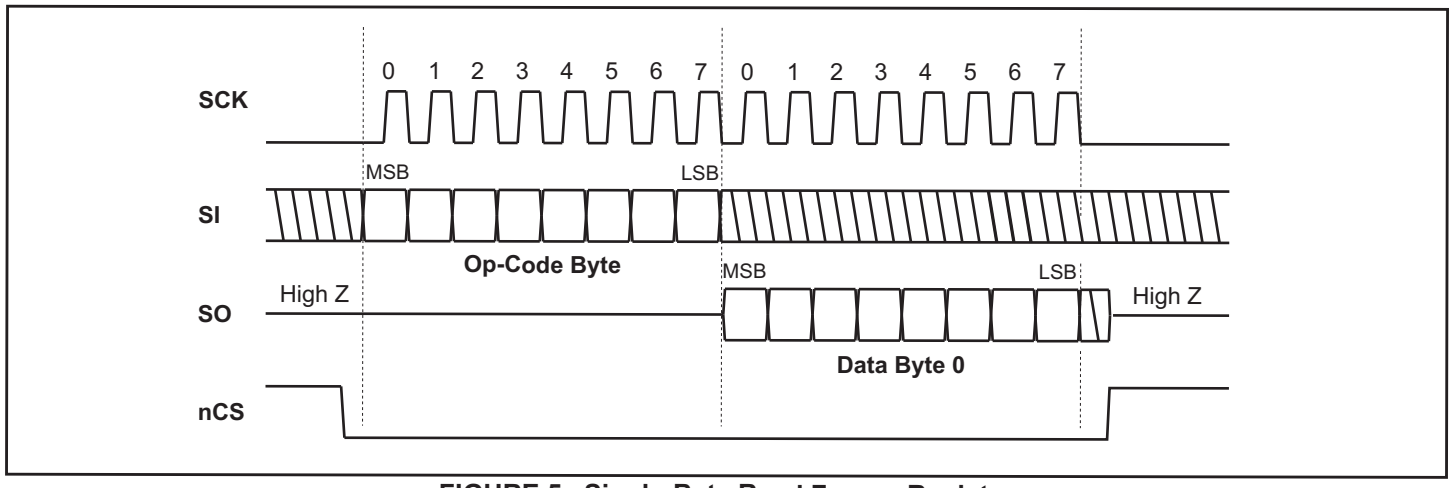


FIGURE 5. Single-Byte Read From a Register

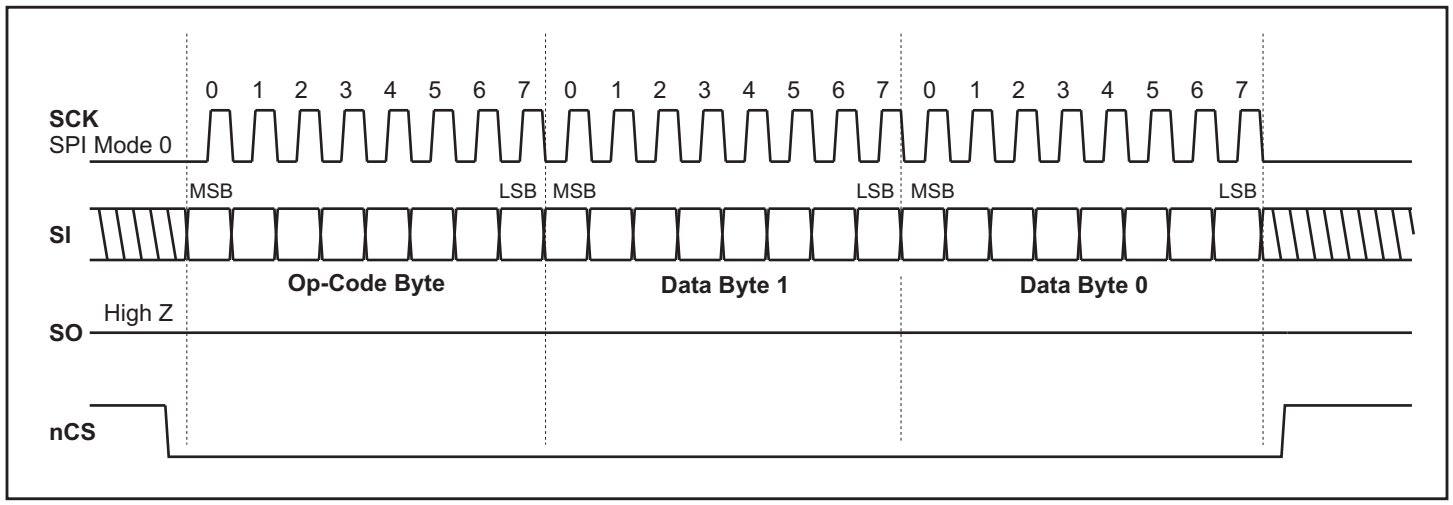


FIGURE 6. 2-Byte SPI Write Example

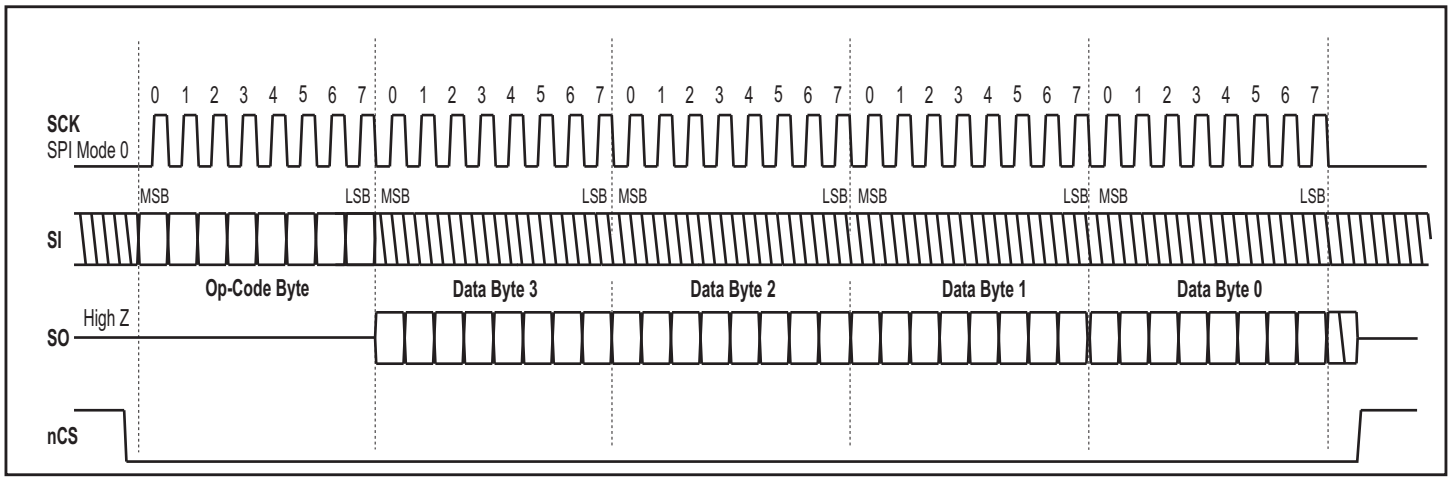


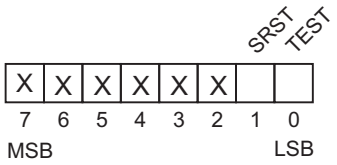
FIGURE 7. 4-Byte SPI Read Example

REGISTER DESCRIPTIONS

CONTROL REGISTER : CTRL

Read: SPI Op-code 0x82
Write: SPI Op-code 0x02

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

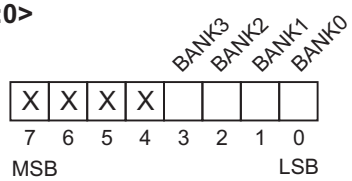
Bit	Name	R/W	Default	Description
7-2	-	R/W	0	Not Used.
1	SRST	R/W	0	Software Reset - Setting this bit to "1" holds all other registers and the TEST bit to their reset values. SRST bit must be written back to "0" to release this reset .
0	TEST	R/W	0	Setting this bit to "1" puts the HI-8437 in the self test mode. Input to sensors are internally set according to the value of the TEST MODE DATA register

TABLE 3.

PROGRAM SENSE BANKS REGISTER: PSEN<3:0>

Read: SPI Op-code 0x84
Write: SPI Op-code 0x04

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

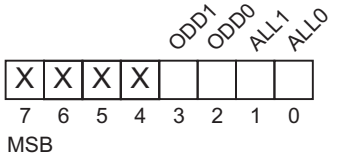
Bit	Name	R/W	Default	Description
7-4	-	R/W	0	Not Used.
3-0	BANK3-0	R/W	0	Program Sensor type for SENSE Inputs.
				Bank 0 programs inputs SENSE<7:0>
				Bank 1 programs inputs SENSE<15:8>
				Bank 2 programs inputs SENSE<23:16>
				Bank 3 programs inputs SENSE<31:24>
				Setting a bit to "0" programs the 8 inputs in the bank to be VTR1 sensors.
				Setting a bit to "1" programs the 8 inputs in the bank to be VTR2 sensors.

TABLE 4.

TEST MODE DATA REGISTER : TMDATA

Read: SPI Op-code 0x9E
Write: SPI Op-code 0x1E

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

Bit	Name	R/W	Default	Description
7-4	-	R/W	0	Not Used.
3-0	TMDATA3-0	R/W	0	These 4 bits program the internal inputs to the sense comparators when in the test mode.
				ODD1 = 1 — Odd inputs are set high
				ODD0 = 1 — Odd inputs are set low
				ALL1 = 1 — All inputs are set high
				ALL0 = 1 — All inputs are set low

Note: Only one mode can be selected. If more than one bit is high the inputs will all be set low.

TABLE 5.

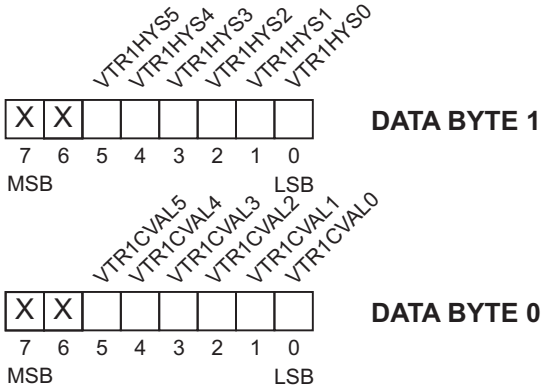
REGISTER DESCRIPTIONS (cont.)

VTR1 THRESHOLD CENTER VALUE AND HYSTERESIS REGISTER: VTR1CENHYS

Read: SPI Op-code 0xBA
Write: SPI Op-code 0x3A

Reset Value 00

[opcode, DB1 , DB0]



Bit	Name	R/W	Default	Description
DATA WORD 1				
7-6	-	R/W	0	Not Used.
5-0	VTR1HYS5-0	R/W	0	VTR1 Hysteresis. For all inputs programmed to be VTR1 sensors the hysteresis is set by these 6 bits. **Hysteresis = 0.2V x VTR1HYS**.
DATA WORD 0				
7-6	-	R/W	0	Not Used.
5- 0	VTR1CVAL5-0	R/W	0	VTR1 Threshold Center Value. For all inputs programmed to be VTR1 sensors the center threshold is set by these 6 bits. **Center Threshold = 0.1V x VTR1CVAL**.

VTHI = Threshold center value + ½ Hysteresis, Max limit = 5.2V, Min limit = 0.6V

VTLO = Threshold center value - ½ Hysteresis, Max limit = 5.0V, Min limit = 0.4V

Example: VTR1 sensors with VTHI = 3.0V and VTLO = 1.0V:

a) Program VTR1HYS — Hysteresis = VTHI - VTLO = 0.2V x VTR1HYS

VTR1HYS = (3V - 1V)/(0.2V) = 10 LSB

b) Program VTR1CVAL — Center Value = (VTHI + VTLO) / 2 = 0.1V x VTR1CVAL

VTR1CVAL = (3V + 1V) / (2 x 0.1) = 20 LSB

c) Write 0x3A 0x0A 0x14 to SPI

0x3A writes to the VTR1 Threshold and Hysteresis Register.

0x0A = 10 LSB x 0.2V/LSB = 2V Hysteresis

0x14 = 20 LSB x 0.1V/LSB = 2V Center Threshold

VTHI = 2V + ½ (2V) = 3V

VTLO = 2V - ½ (2V) = 1V

Note: The maximum value for VTHI = 5.2V and the minimum value for VTLO = 0.4V. Also VTHI - VTLO >= 0.2V.

TABLE 6.

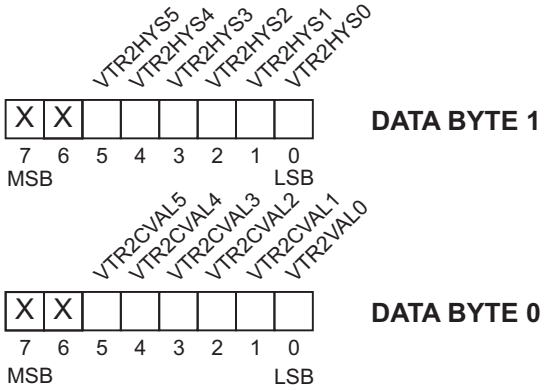
REGISTER DESCRIPTIONS (cont.)

VTR2 THRESHOLD CENTER VALUE AND HYSTERESIS REGISTER: VTR2CENHYS

Read: SPI Op-code 0xBC
Write: SPI Op-code 0x3C

Reset Value 00

[Opcode, DB1, DB0]



Bit	Name	R/W	Default	Description
DATA WORD 1				
7-6	-	R/W	0	Not Used.
5-0	VTR2HYS5-0	R/W	0	VTR2 Hysteresis. For all inputs programmed to be VTR2 sensors the hysteresis is set by these 6 bits. **Hysteresis = 0.2V x VTR2HYS**.
DATA WORD 0				
7-6	-	R/W	0	Not Used.
5- 0	VTR2CVAL5-0	R/W	0	VTR2 Threshold Center Value. For all inputs programmed to be VTR2 sensors the center threshold is set by these 6 bits. **Center Threshold = 0.1V x VTR2CVAL**.

VTHI = Threshold center value + ½ Hysteresis, Max limit = 5.2V, Min limit = 0.6V

VTLO = Threshold center value - ½ Hysteresis, Max limit = 5.0V, Min limit = 0.4V

Example: VTR2 sensor with VTHI = 5V and VTLO = 2V:

a) Program VTR2HYS — Hysteresis = VTHI - VTLO = 0.2V x VTR2HYS

VTR2HYS = (5V - 2V)/(0.2V) = 15 LSB

b) Program VTR2CVAL — Center Value = (VTHI + VTLO) / 2 = 0.1V x VTR2CVAL

VTR2CVAL = (5V + 2V) / (2 x 0.1) = 35 LSB

c) write 0x3C 0x0F 0x23 to SPI

0x3C writes to the VTR2 Threshold and Hysteresis Registers.

0x0F = 15 LSB x 0.2V/LSB = 3V Hysteresis

0x23 = 35 LSB x 0.1V/LSB = 3.5V Center Value

VTHI = 3.5 + ½ (3) = 5V

VTLO = 3.5 - ½ (3) = 2V

Note: The maximum value for VTHI = 5.2V and the minimum value for VTLO = 0.4V. Also VTHI - VTLO >= 0.2V.

TABLE 7.

REGISTER DESCRIPTIONS (cont.)

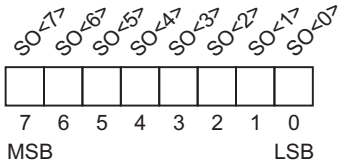
SENSOR OUTPUT STATUS REGISTER: SO<31:0>
THIS 32 BIT REGISTER IS ACCESSED BY THE FOLLOWING 5 SPI COMMANDS

For sense inputs: SO<n> = "1" if the SENSE<n> pin is open or < VTLO
SO<n> = "0" if the SENSE<n> pin is >= VTHI

SENSOR STATUS BANK 0 REGISTER: SO<7:0>

Read: SPI Op-code 0x90
Write: NA, read only

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

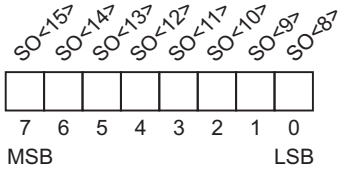
Bit	Name	R/W	Default	Description
7-0	SO<7:0>	R	0	Sensor output status, SO<7:0> reports the state of SENSE<7:0>.

TABLE 8.

SENSOR STATUS BANK 1 REGISTER: SO<15:8>

Read: SPI Op-code 0x92
Write: NA, read only

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

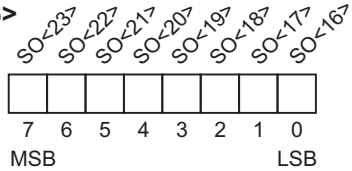
Bit	Name	R/W	Default	Description
7-0	SO<15:8>	R	0	Sensor output status, SO<15:8> reports the state of SENSE<15:8>.

TABLE 9.

SENSOR STATUS BANK 2 REGISTER: SO<23:16>

Read: SPI Op-code 0x94
Write: NA, read only

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

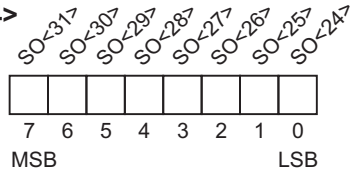
Bit	Name	R/W	Default	Description
7-0	SO<23:16>	R	0	Sensor output status, SO<23:16> reports the state of SENSE<23:16>.

TABLE 10.

SENSOR STATUS BANK 3 REGISTER: SO<31:24>

Read: SPI Op-code 0x96
Write: NA, read only

Reset Value 00
[Opcode, DB0]



DATA BYTE 0

Bit	Name	R/W	Default	Description
7-0	SO<31:24>	R	0	Sensor output status, SO<31:24> reports the state of SENSE<31:24>.

TABLE 11.

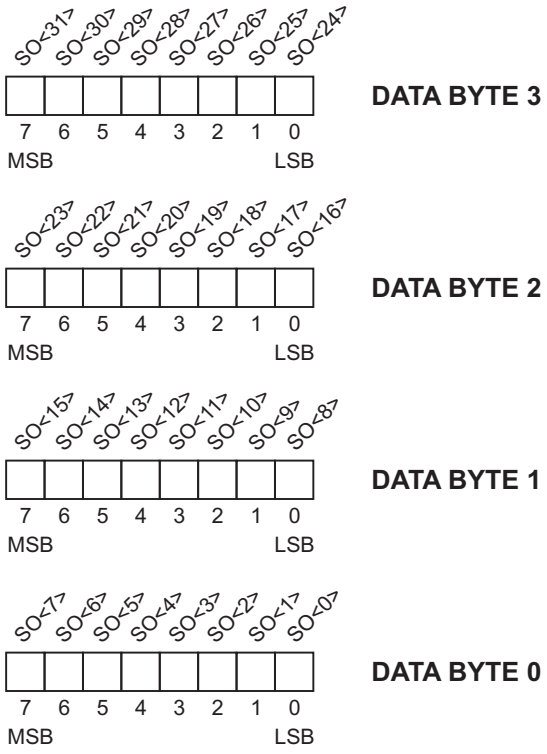
REGISTER DESCRIPTIONS (cont.)

SENSOR STATUS ALL BANKS REGISTER: SO<31:0>

Read: SPI Op-code 0xF8
Write: NA, read only

Reset Value 00

[Opcode, DB3, DB2, DB1, DB0]

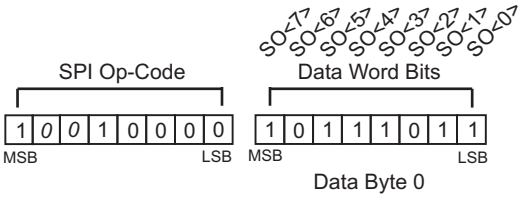


Bit	Name	R/W	Default	Description
31-0	SO<31:0>	R	0	Sensor output status, SO<31:0> reports the state of SENSE<31:0>.

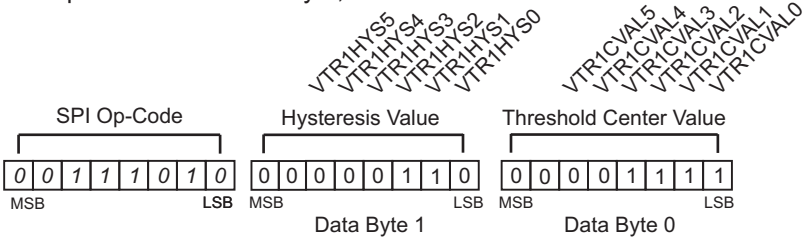
TABLE 12.

SPI Format Examples

Example 1. Single Data Byte, Read Sense Data in SENSE BANK 0 (Op-Code 0x90).



Example 2. Double Data Byte, Write VTR1 Threshold Center Value and Hysteresis (Op-Code 0x3A) .



Example 3. 4 Data Byte, Read all sense values, SENSE ALL BANKS (Op-Code 0xF8).

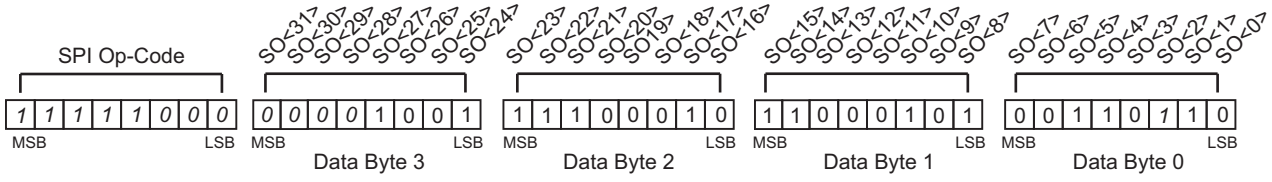


TABLE 13.

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8437 is comprised of 32 sensors arranged in 4 banks of 8 inputs, easily accessible via a four wire SPI communication bus. Each bank of sensors can be programmed with one of two threshold ranges, VTR1 or VTR2. The state of each sensor can be read out through the SPI.

The VTR1 high/low thresholds can be programmed independently of the VTR2 high/low thresholds. Table 14 summarizes basic function selection and Table 16 gives more details on possible threshold values.

An internal test mode is available which sets the input to each sensor comparator to the test value as programmed by the Test Mode Data Register.

NOTE: Certain safety-critical flight applications require periodic sensor testing or register re-programming during flight. If programmable registers are periodically re-written, the sensor inputs **must** be in a high or low state prior to and during each re-programming cycle. See also section on Test Mode.

INITIALIZATION AND RESET

The HI-8437 generates a full reset upon application of power. This power-on-reset (POR) sets all registers to their default values.

The part can also be initialized to the full reset state by applying a 100ns active low pulse to the external nMR pin.

A software reset is also possible via the SPI by writing a “1” to CNTRL<1>. This reset is the same as the full reset except the part is held in the reset mode until the CNTRL<1> bit is written back to a “0”.

CONFIGURATION

The user configures the HI-8437 for specific applications by:
1) Programming the sensor threshold range for each of the 4 banks.
2) Convert the required VTHI and VTLO into center and hysteresis values as shown in example below.

FUNCTION TABLE

Table 14. Function Table

SENSE_n	PSEN_n	SO_n
> VT1HI	L (VTR1)	L
Open or < VT1LO	L (VTR1)	H
> VT2HI	H (VTR2)	L
Open or < VT2LO	H (VTR2)	H

H = VLOGIC, L = GND
VTHI = Threshold Center Value + ½ Hsyteresis
VTLO = Threshold Center Value - ½ Hysteresis

PROGRAMMING THRESHOLDS

The HI-8437’s on-chip DAC takes the 6-bit programmed center and hysteresis values from the Threshold Center Value and Hysteresis Registers (VTR1CENHYS and VTR2CENHYS) and converts them to VTHI and VTLO values. Maximum and minimum values may be found in Table 16. The gain of the DAC is 0.1V per LSB.

VTHI = center value + ½ hysteresis
VTLO = center value - ½ hysteresis

To program the thresholds:
a) Select VTHI and VTLO for each threshold range.
b) VTRnHYS = (VTHI - VTLO) / (0.2V/LSB).
c) VTRnCVAL = (VTHI + VTLO)/2 / (0.1V/LSB)
d) Program the registers.

FUNCTIONAL DESCRIPTION (cont.)

TEST MODE

Writing a high in CTRL<0> puts the HI-8437 into the test mode. Referring to Figure 2, when in the test mode each of the internal inputs to the sense comparators are set to either a high or low. Since the input sense pin is isolated by a 200KΩ resistor, this test mode will not disturb the actual status of the input pin.

By programming the Test Mode Data Register, one of four input data patterns can be selected. See Table 5 on page 6 for options. The comparator results are read through the SPI just as in normal operation.

Before entering Test Mode the sensors must be programmed with valid threshold values.

NOTE: Certain flight applications require periodic sensor testing during flight. To guarantee consistent sensor outputs when alternating between test mode and normal operation mode, the sensor inputs **must** be in a high or low state upon exiting test mode.

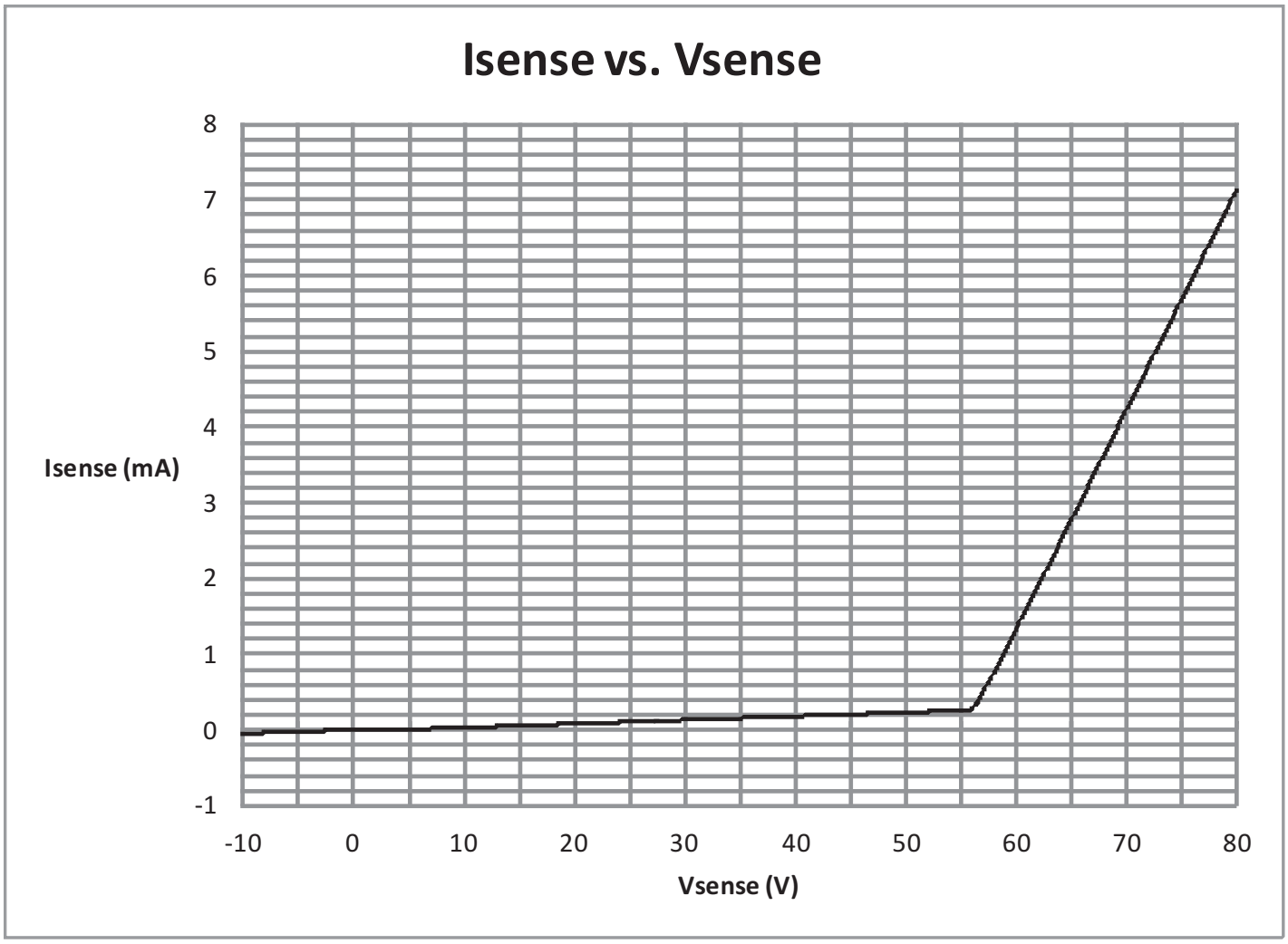


Figure 8. Input Current Vs. Input Voltage

FUNCTIONAL DESCRIPTION (cont.)

96 Channel Sensor Application using HI-8437

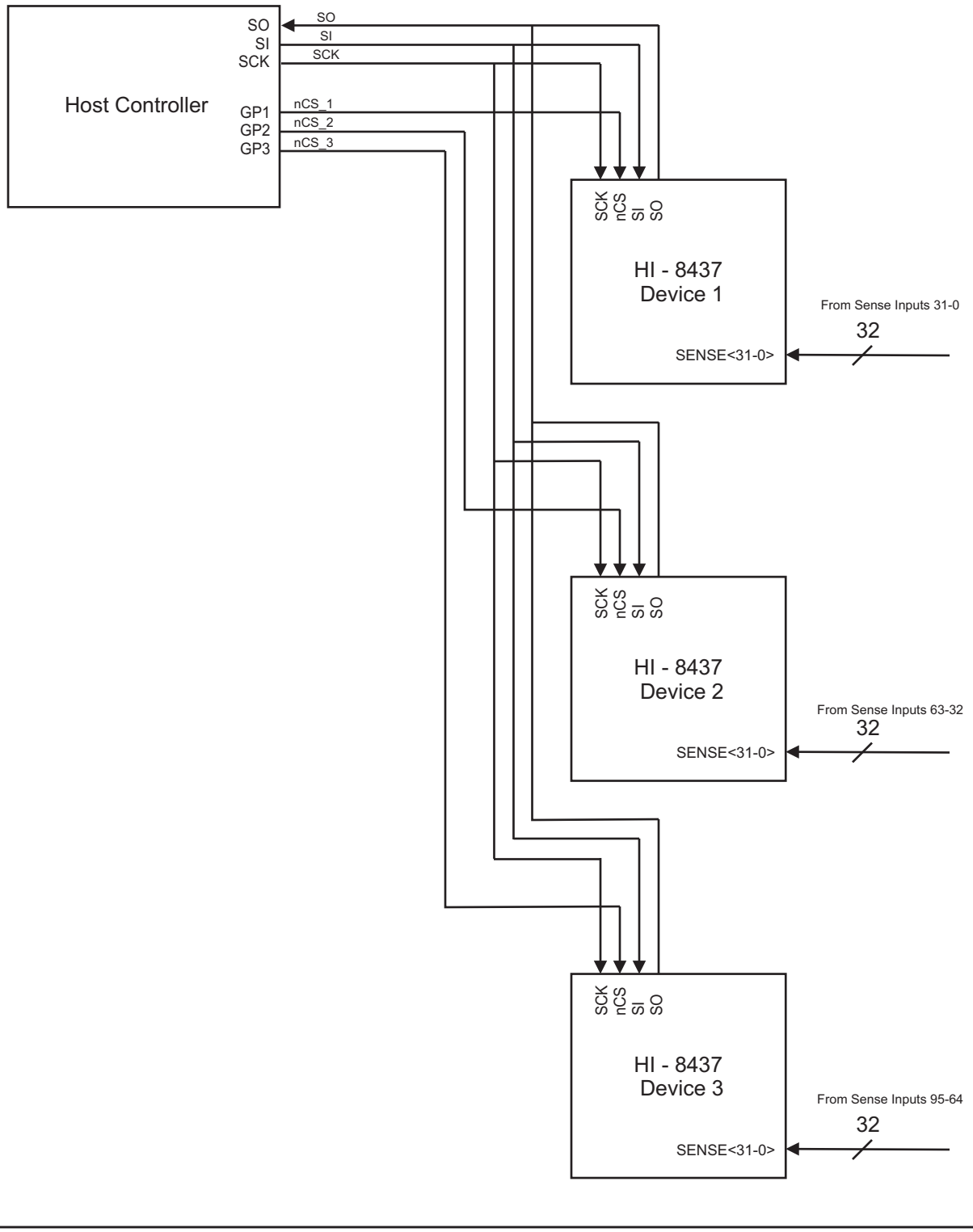


Figure 9. Multiple Chip Connection

FUNCTIONAL DESCRIPTION (cont.)

LIGHTNING PROTECTION

All SENSE_n inputs are protected to RTCA/DO-160G, Section 22, Categories AZ and BZ, Waveforms 3, 4, 5A, with no external components. In addition, all inputs are also protected to ZZ, Waveforms 3 and 5B, to provide more robustness in composite airframe applications. Table 15 and Figure 10 give values and waveforms. See Application Note AN-305 for recommendations on lightning protection of Holt's family of Discrete-to-Digital devices.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
2	250/10	125/25	125/125	125/125
Z	500/20	300/60	300/300	300/300
3	600/24	300/60	300/300	300/300

Table 15. Waveform Peak Amplitudes

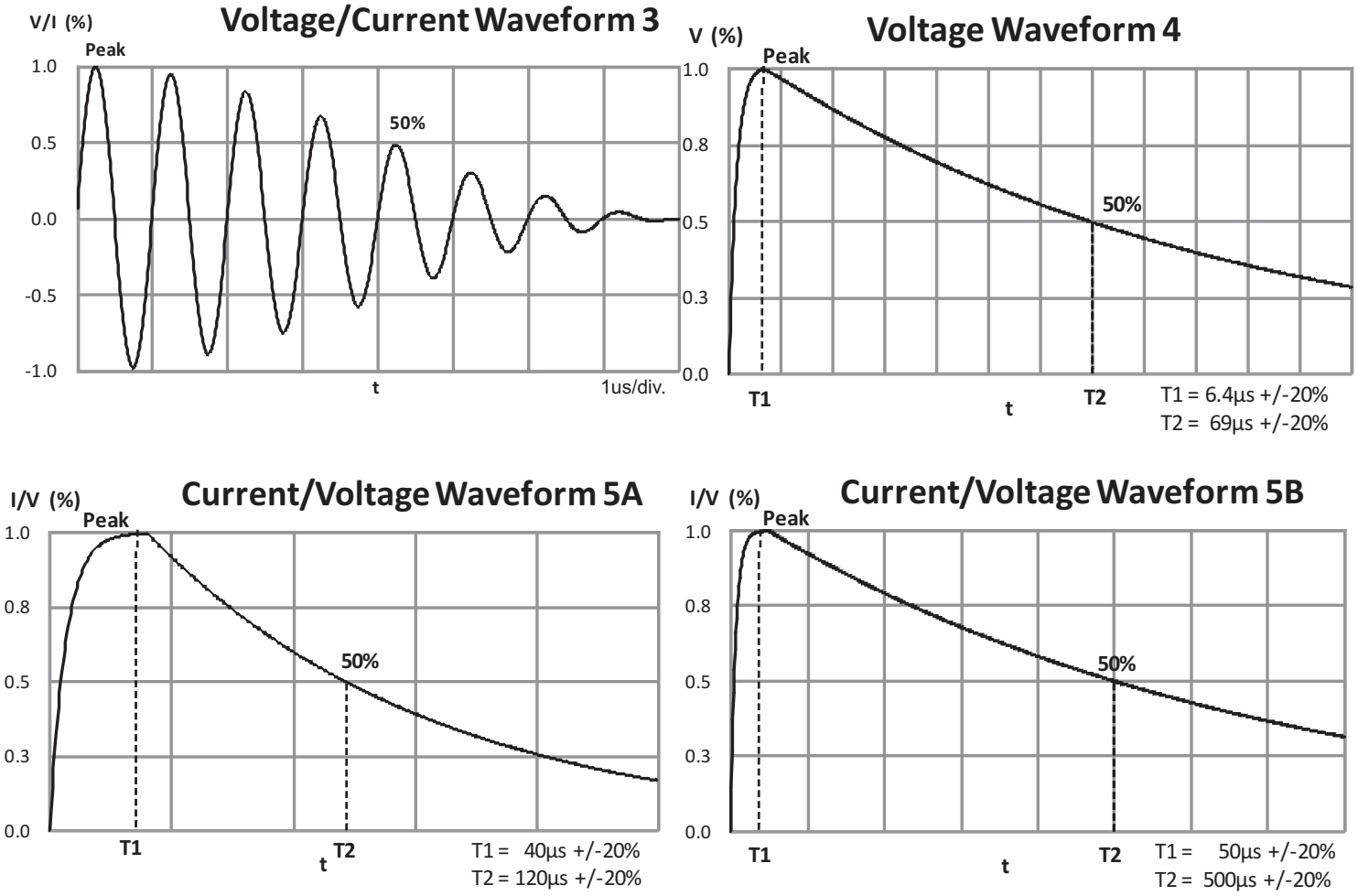


Figure 10. Lightning Waveforms

FUNCTIONAL DESCRIPTION (cont.)

Table 16. Configuration examples and allowed threshold values -55C to 125C.

VLOGIC	PSENn	Operation	Programmed VTHI	Programmed VTLO	Guaranteed High Threshold*	Guaranteed Low Threshold*
3.0V to 3.6V	L	VTR1	1.4V	0.4V	VTHI + 0.3V	VTLO - 0.2V
3.0V to 3.6V	H	VTR2	5.2V	0.4V	VTHI + 1.0V	VTLO - 0.2V

NOTE: VTHI = Center Value + 0.5 x Hysteresis, VTLO = Center Value - 0.5 x Hysteresis
*: See Figure 11 for guaranteed tolerance for programmed VTHI and VTLO

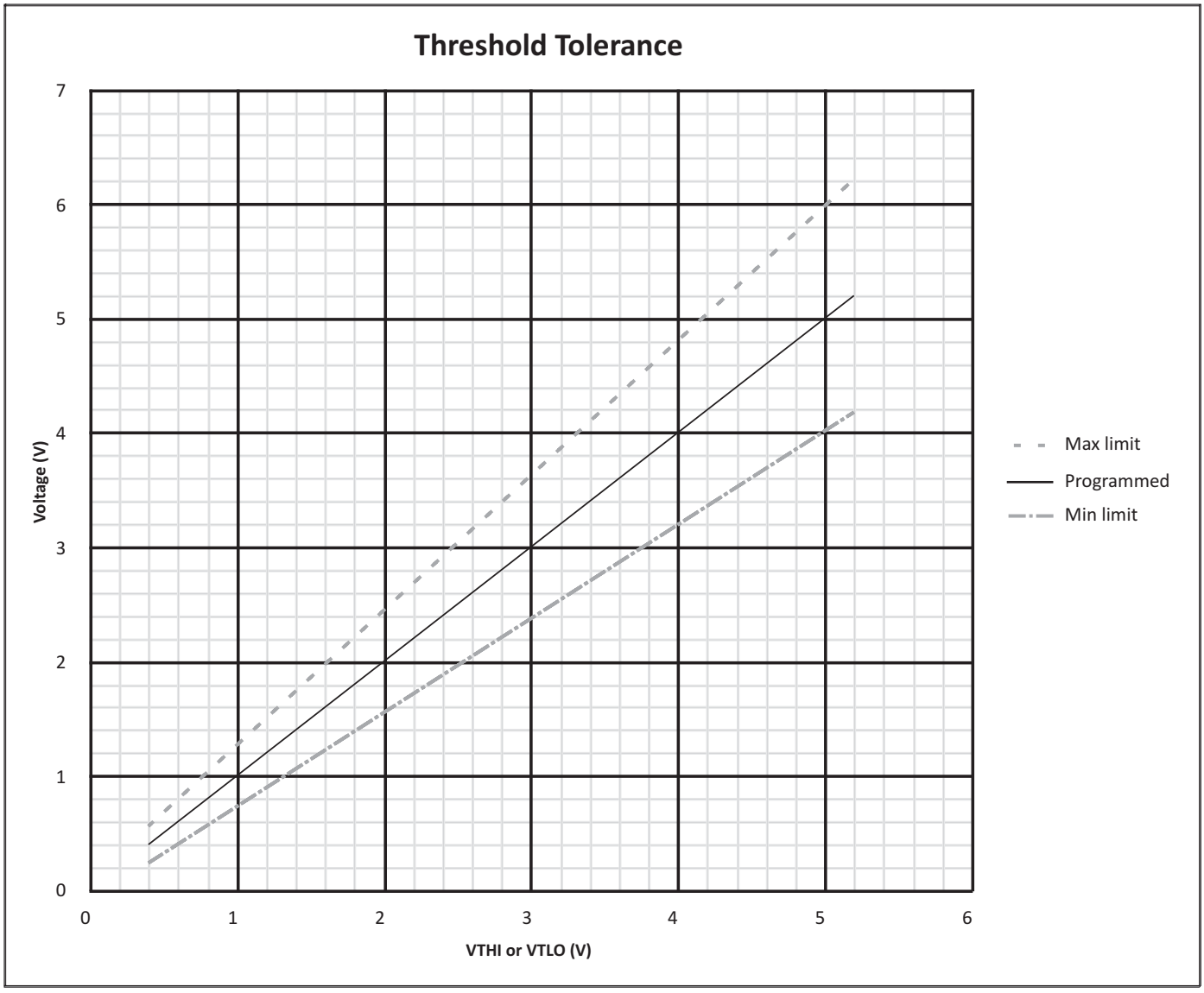


Figure 11: Threshold tolerance over Programmed value

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground	
Supply Voltage (VLOGIC)	-0.3V to +7V
Logic Input Voltage Range	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range	
(DC)	-80V to +80V
(AC, 60 - 400Hz)	115Vrms
Continuous Power Dissipation (TA=+70°C)	
QFN (derate 21.3mW/°C above +70°C)	1.7W
QFP (derate 10.0mW/°C above +70°C)	1.5W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to -150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VLOGIC	3.0V to 3.6V
Digital Inputs	0 to VLOGIC
Sense_n	-4.0V to 36V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

VDD = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
DISCRETE INPUTS						
Input Resistance to ground	R_{IN}			400		KΩ
Threshold DAC Gain	V_{TDG}	1 DAC bit = 0.1V. Guaranteed monotonic		0.1		V/bit
Max Threshold High (Open State Input Voltage)	V_{THIMAX}	VTHI = Center Value + ½ Hysteresis Input voltage to give Low output VTHI - VTLO ≥ 0.2V			Refer to Figure 11	V
Min Threshold Low (Ground State Input Voltage)	V_{TLOMIN}	VTLO = Center Value - ½ Hysteresis Input voltage to give High output VTHI - VTLO ≥ 0.2V	Refer to Figure 11			V
LOGIC INPUTS						
Input Voltage	V_{IH}	Input Voltage HI	80%			VLOGIC
	V_{IL}	Input Votage LO			20%	VLOGIC
Input Current, SI	I_{SINK}	V_{IN} = VLOGIC, 30KΩ pull down			125	µA
	I_{SOURCE}	V_{IN} = GND			0.1	µA
Input Current, nMR, nCS	I_{SINK}	V_{IN} = VLOGIC	0.1			µA
	I_{SOURCE}	V_{IN} = GND , 30KΩ pull up	125			µA
LOGIC OUTPUTS						
Output Voltage	V_{OH}	I_{OH} = -100µA	90%			VLOGIC
	V_{OL}	I_{OL} = 100µA			10%	VLOGIC
Output Current	I_{OL}	V_{OUT}= 0.4V	1.6			mA
	I_{OH}	V_{OUT} = VLOGIC - 0.4V			-1.0	mA
Output Capacitance	C_O			15		pF
SUPPLY CURRENT						
VLOGIC Current	I_{DD1}	All Sense Pins Open			15	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V, TA = Operating Temperature Range

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
SPI INTERFACE TIMINGS					
SCK clock period	t_{CYC}	50			ns
nCS active after last SCK rising edge	t_{CHH}	5			ns
nCS setup time to first SCK rising edge	t_{CES}	5			ns
nCS hold time after last SCK falling edge	t_{CEH}	5			ns
nCS inactive between SPI instructions	t_{CPH}	55			ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10			ns
SCK rise time	t_{SCKR}			10	ns
SCK fall time	t_{SCKF}			10	ns
SCK pulse width high	t_{SCKH}	20			ns
SCK pulse width low	t_{SCKL}	20			ns
SO valid after SCK falling edge	t_{DV}			20	ns
SO high-impedance after $\overline{CS}$ inactive	t_{CHZ}			20	
nMR pulse width	t_{MR}	100			ns
SENSOR TIMINGS					
Delay, change at sense input to valid status in SO_n				1	µs
Delay, change of Threshold to valid status in SO_n				1	µs

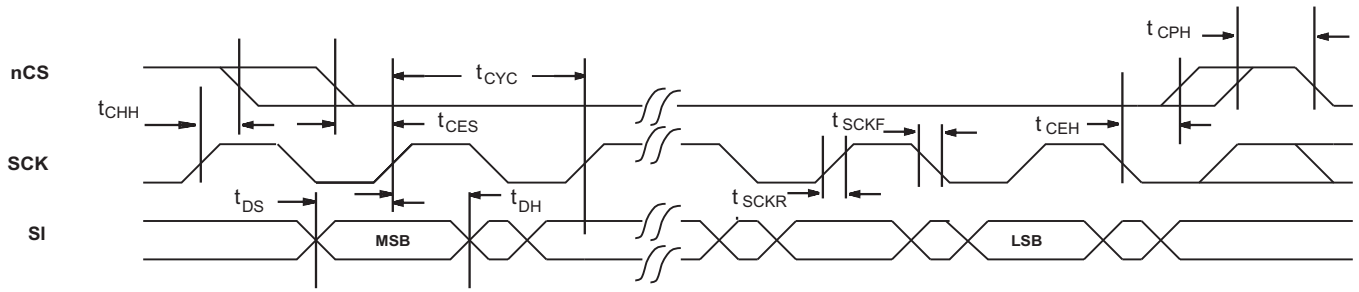


FIGURE 12. SPI Serial Input Timing

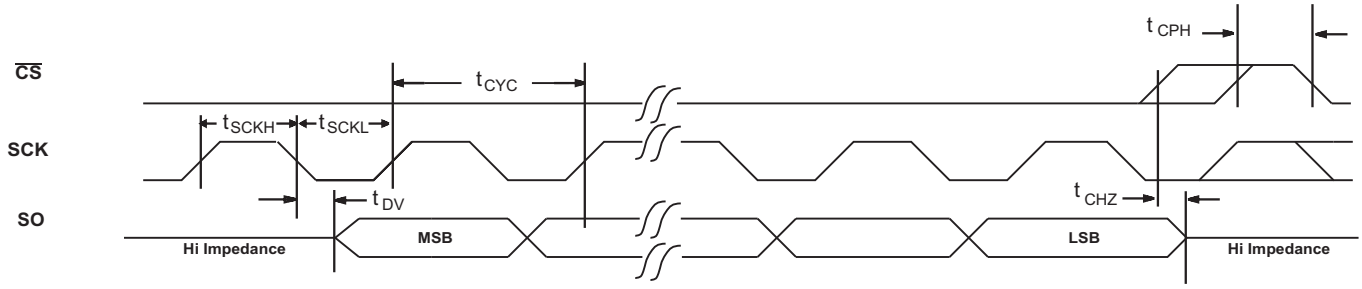


FIGURE 13. SPI Serial Output Timing

ORDERING INFORMATION

HI - 8437xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8437PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PMQS)
8437PC	44 PIN PLASTIC CHIP-SCALE, QFN (44PCS)

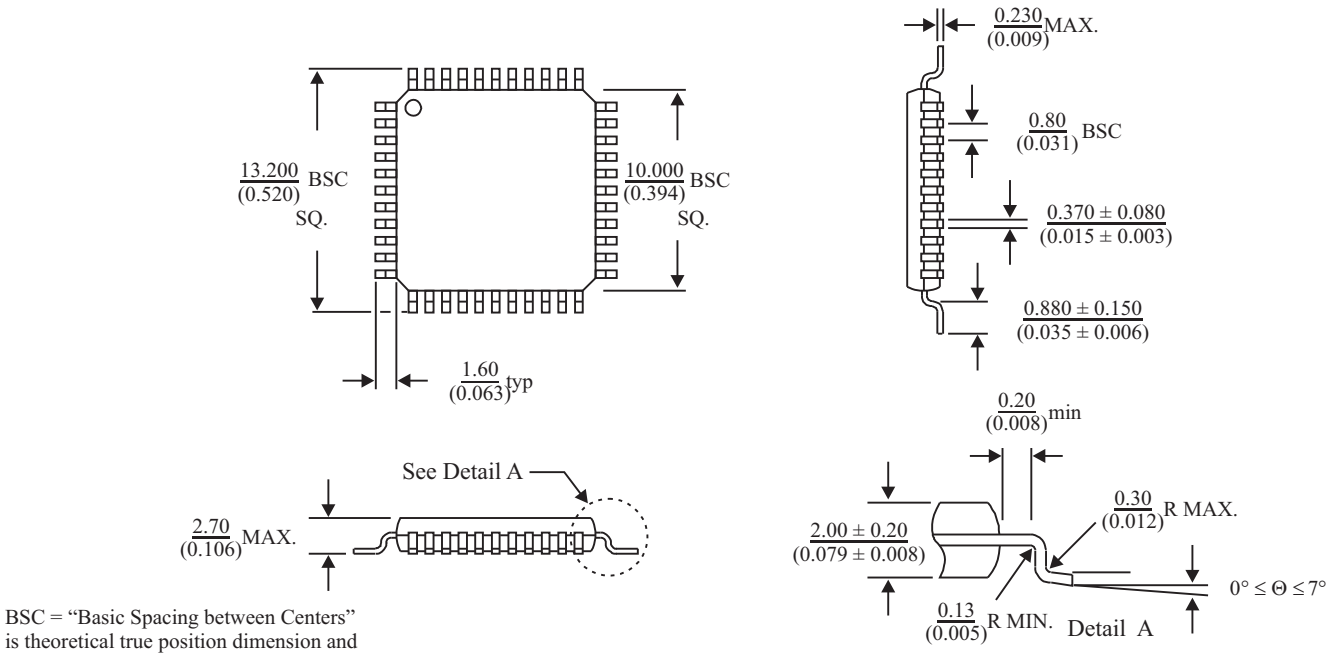
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8437	New	11/22/13	Initial Release.
	A	01/29/16	Update SPI Output timing diagram. Update AC Characteristics for t_{CHZ}. Clarify operation when switching between test mode and normal operation mode or re-writing programmable registers.

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS

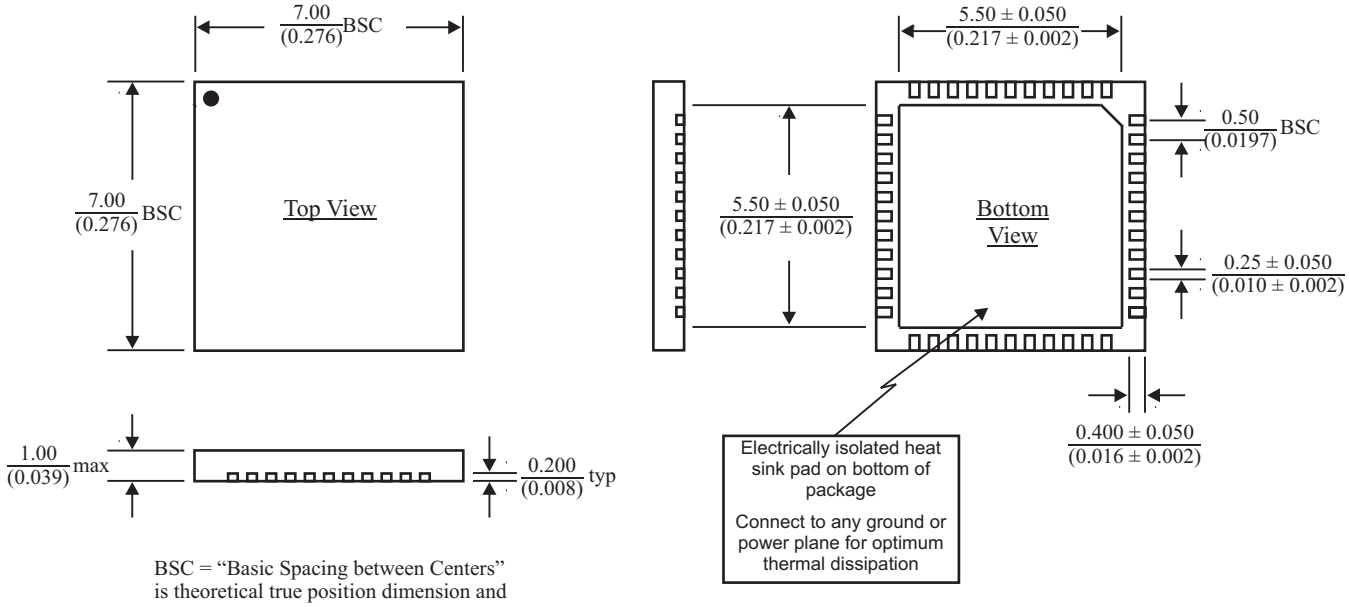


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)