September 1998 File Number 3579.4

8-Bit, 250 MSPS, Flash A/D Converter

The HI1166 is an 8-bit, ultra high speed, flash Analog-to-Digital converter IC capable of digitizing analog signals at a maximum rate of 250 MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

Applications

- Spectrum Analyzers
- Radar Systems
- Direct RF Down-Conversion
- Video Digitizing
- Communication Systems
- Digital Oscilloscopes

Ordering Information

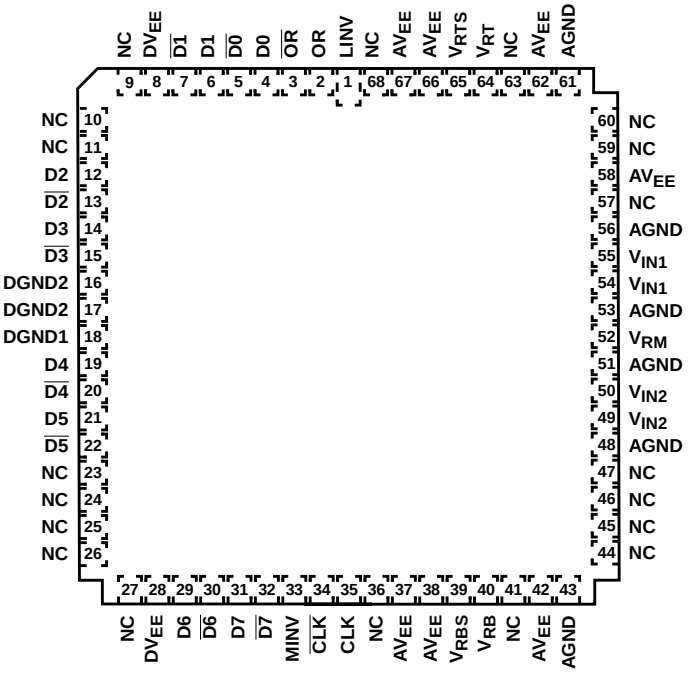
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1166AIL	-20 to 100	68 Ld CLCC	J68.A
HI1166-EV	25	Evaluation Board	

Features

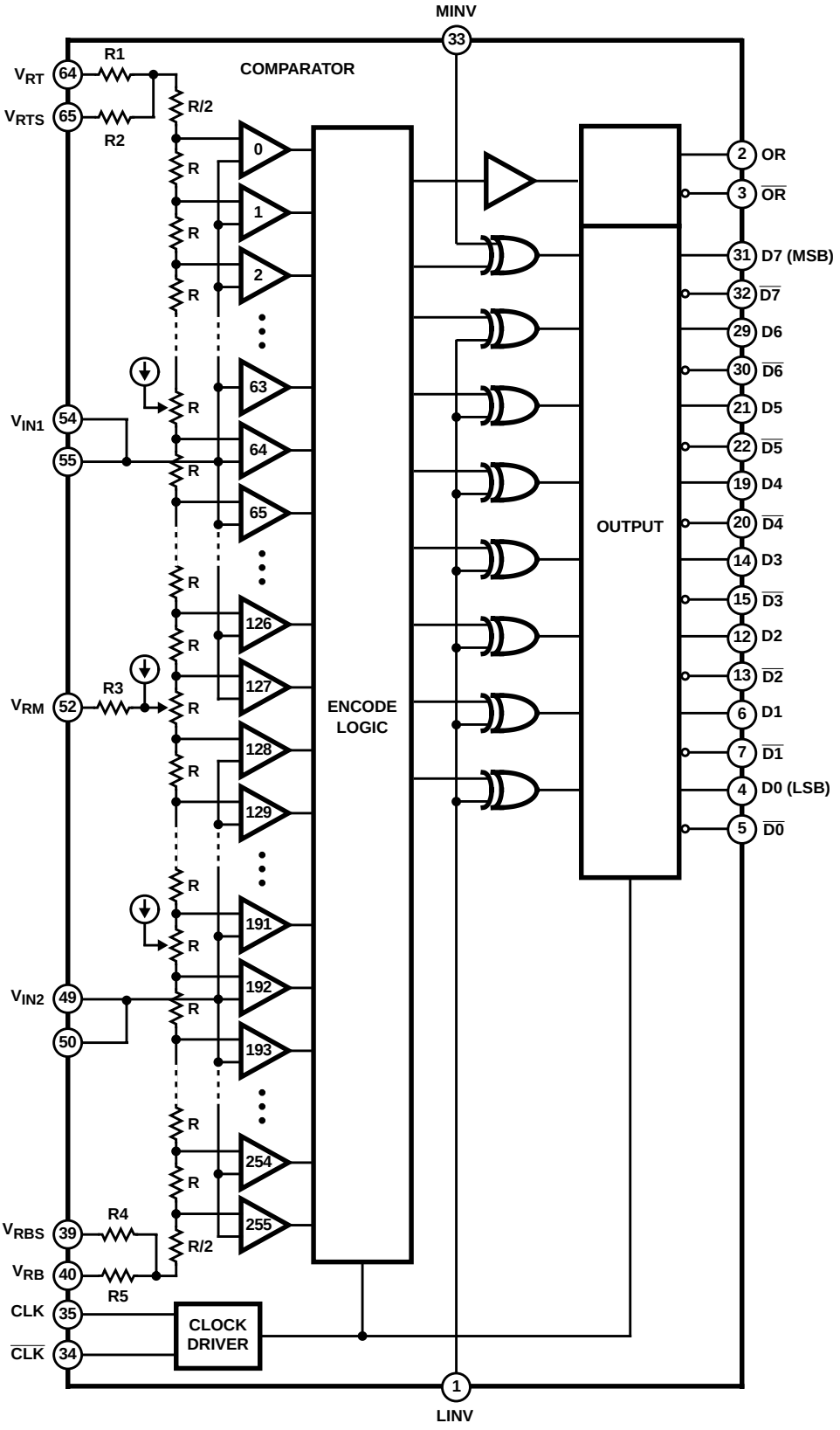
- Differential Linearity Error . . . . . ±0.5 LSB or Less
- Integral Linearity Error . . . . . ±0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate (Min) . . . . . 250 MSPS
- Low Input Capacitance 18pF (Typ)
- Wide Analog Input Bandwidth (Min for Full Scale Input) 250MHz
- Single Power Supply . . . . . -5.2V
- Low Power Consumption . . . . . 1.4W (Typ)
- Low Error Rate
- Capable of Driving 50Ω Loads
- Evaluation Board Available
- Direct Replacement for Sony CXA1166K

Pinout

HI1166
(CLCC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V to +0.5V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} . . . . . -2.7V to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
MINV, LINV, CLK, $\overline{CLK}$ . . . . . -4V to +0.5V
$|CLK - \overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) . . . . . -30mA to 0mA
Temperature Range, T_A (Note 5) . . . . . -20^oC to 100^oC
T_C . . . . . -20^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}{}^oC/W$	$\theta_{JC}{}^oC/W$
CLCC Package	38	10

Maximum Power Dissipation 2.1W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range (T_{STG}) . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

Operating Conditions (Note 1)

Supply Voltage	MIN	TYP	MAX
AV_{EE}, DV_{EE}	-5.5V	-5.2	-4.95V
AV_{EE} - DV_{EE}	-0.05V	0	0.05V
AGND - DGND	-0.05V	0	0.05V

Reference Input Voltage	MIN	TYP	MAX
V_{RT}	-0.1V	-2	0.1V
V_{RB}	-2.2V	-2	-1.8V

Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, INL	f_C = 250 MSPS	-	±0.3	±0.5	LSB
Differential Linearity Error, DNL	f_C = 250 MSPS	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1kHz, Full Scale, f_C = 250MHz	44	46	-	dB
	Input = 60kHz, Full Scale, f_C = 250MHz	-	37	-	dB
Error Rate	Input = 50MHz, Full Scale, Error > 16 LSB, f_C = 250MHz	-	-	10^{-9}	TPS (Note 3)
	Input = 62.499MHz, Full Scale, Error > 16 LSB, f_C = 250MHz	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG	NTSC 40 IRE Mod. Ramp, f_C = 250 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Overrange Recovery Time		-	1.0	-	ns
Maximum Conversion Rate, f_C		250	-	-	MSPS
Aperture Jitter, t_{AJ}		-	9	-	ps
Sampling Delay, t_{DS}		0.4	1.4	2.4	ns
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	V_{IN} - 1V + 0.07V_{RMS}	-	18	-	pF
Analog Input Resistance, R_{IN}		50	120	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	-	450	µA
Full Scale Input Bandwidth	V_{IN} = 2V_{P-P}	200	250	-	MHz
REFERENCE INPUTS					
Reference Resistance, R_{REF}		83	125	182	Ω

Electrical Specifications $T_A = 25^oC$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Residual Resistance	R1	Note 2	0.1	0.6	2.0	Ω
	R2		300	500	700	Ω
	R3		0.5	2.0	5.0	Ω
	R4		300	500	700	Ω
	R5		0.1	0.6	2.0	Ω
DIGITAL INPUTS						
Logic H Level, V_{IH}			-1.13	-	-	V
Logic L Level, V_{IL}			-	-	-1.5	V
Logic H Current, I_{IH}		Input Connected to GND	0	-	70	µA
Logic L Current, I_{IL}		Input Connected to -2V	-50	-	50	µA
Input Capacitance			-	4	-	pF
DIGITAL OUTPUTS						
Logic H Level, V_{OH}		$R_L = 50Ω$	-1.0	-	-	V
Logic L Level, V_{OL}		$R_L = 50Ω$	-	-	-1.6	V
TIMING CHARACTERISTICS						
H Pulse Width of Clock, t_{PW1}			1.8	-	-	ns
L Pulse Width of Clock, t_{PW0}			1.8	-	-	ns
Output Rise Time, t_r		$R_L = 50Ω$	-	0.6	1.5	ns
Output Fall Time, t_f		$R_L = 50Ω$	-	0.6	1.5	ns
Output Delay, t_{OD}		$R_L = 50Ω$	1.8	2.5	3.2	ns
POWER SUPPLY CHARACTERISTICS						
Supply Current, I_{EE}			-360	-270	-	mA
Power Consumption, P_D		Note 4	-	1.4	1.9	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $PD = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
5. T_A is specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

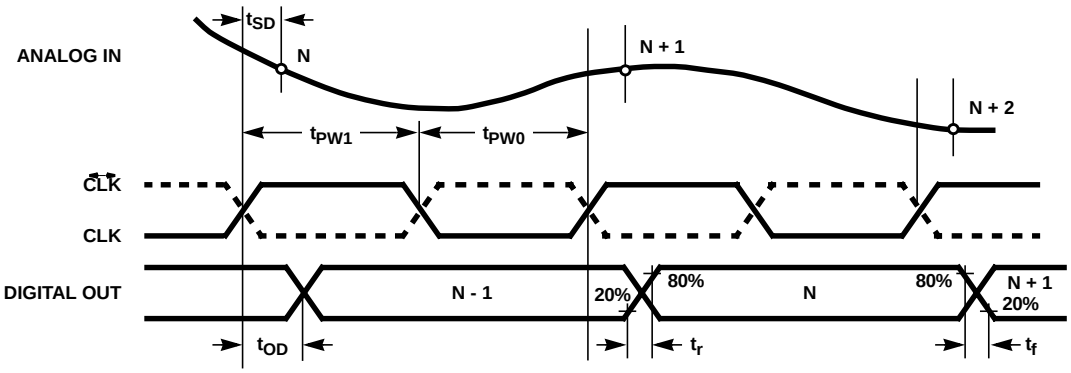


FIGURE 1.

Typical Performance Curves

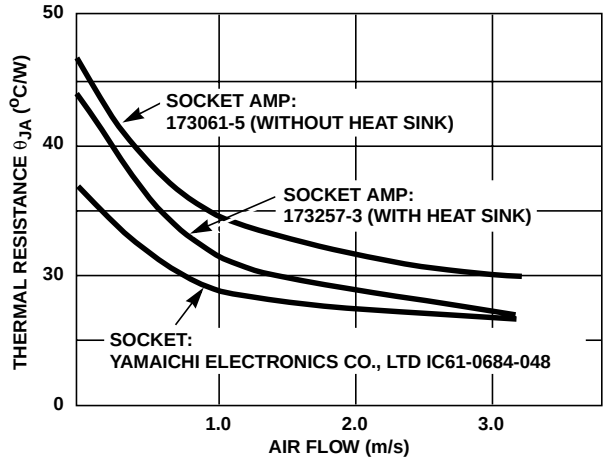


FIGURE 2. THERMAL RESISTANCE OF THE CONVERTER MOUNTED ON A BOARD

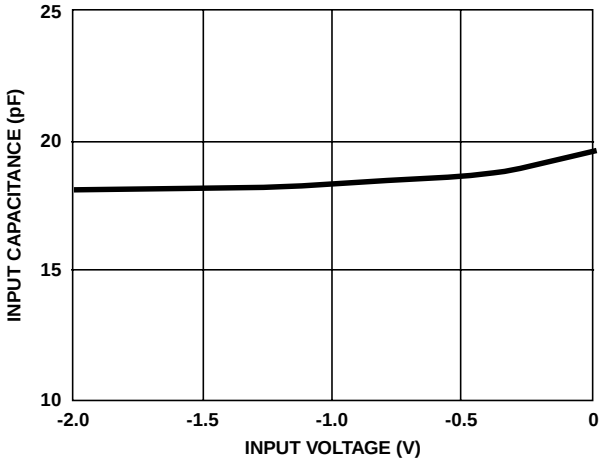


FIGURE 3. V_{IN} PIN CAPACITANCE vs VOLTAGE CHARACTERISTICS

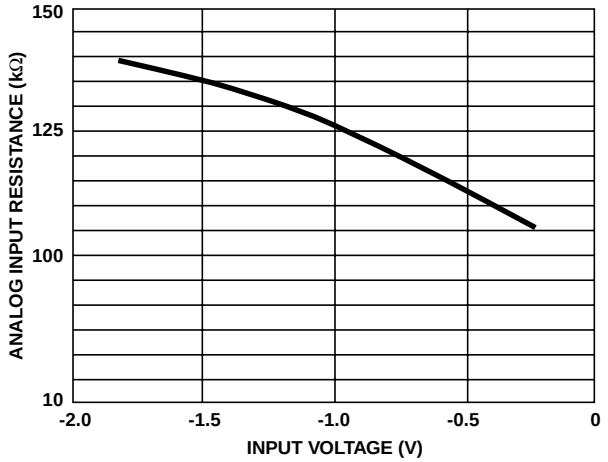


FIGURE 4. V_{IN} PIN INPUT RESISTANCE vs VOLTAGE CHARACTERISTICS

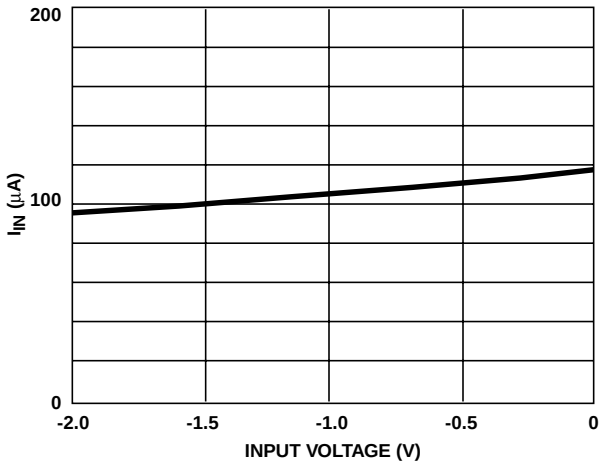


FIGURE 5. V_{IN} PIN INPUT CURRENT vs VOLTAGE CHARACTERISTICS

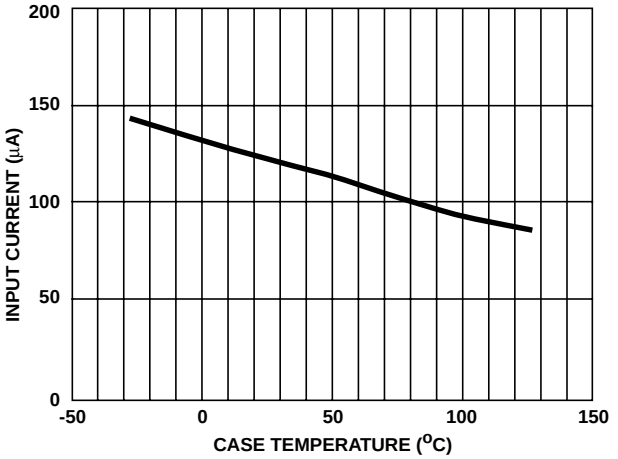


FIGURE 6. V_{IN} PIN INPUT CURRENT vs TEMPERATURE CHARACTERISTICS

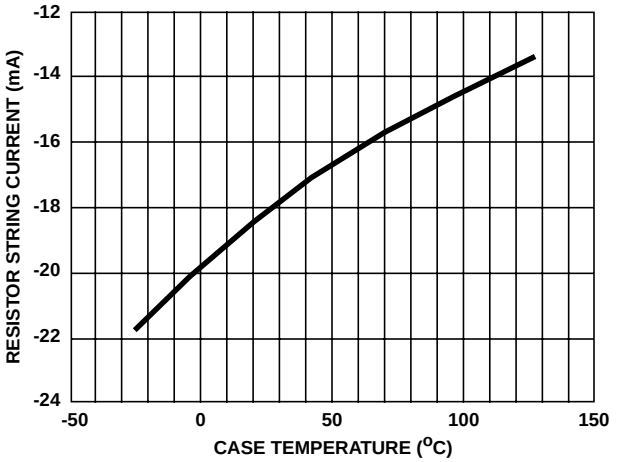


FIGURE 7. RESISTOR STRING CURRENT vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

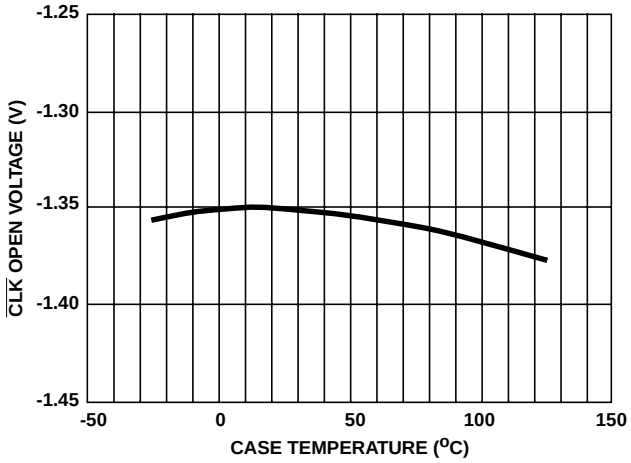


FIGURE 8. $\overline{CLK}$ OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

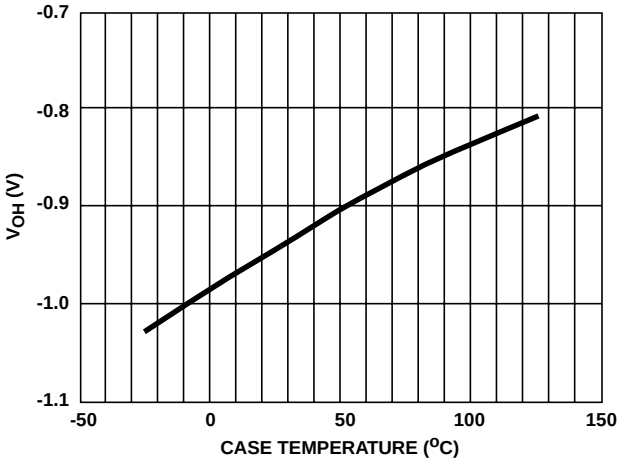


FIGURE 9. V_{OH} vs TEMPERATURE CHARACTERISTICS

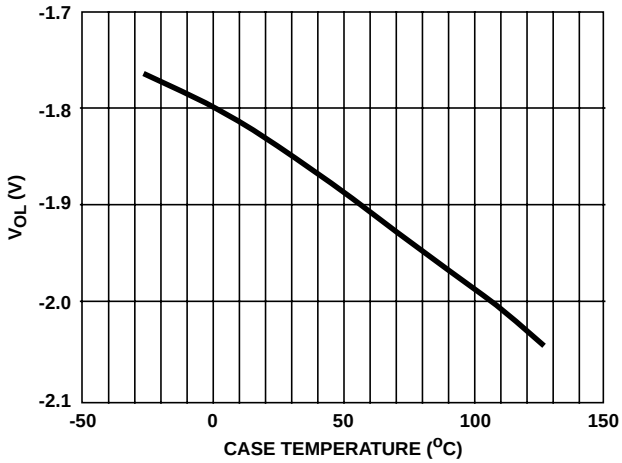


FIGURE 10. V_{OL} vs TEMPERATURE CHARACTERISTICS

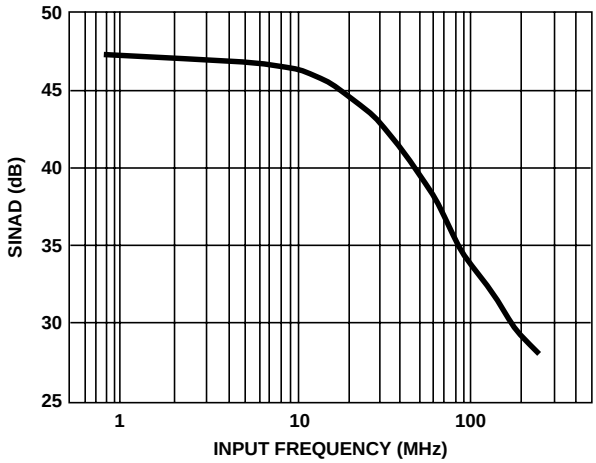


FIGURE 11. SINAD vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

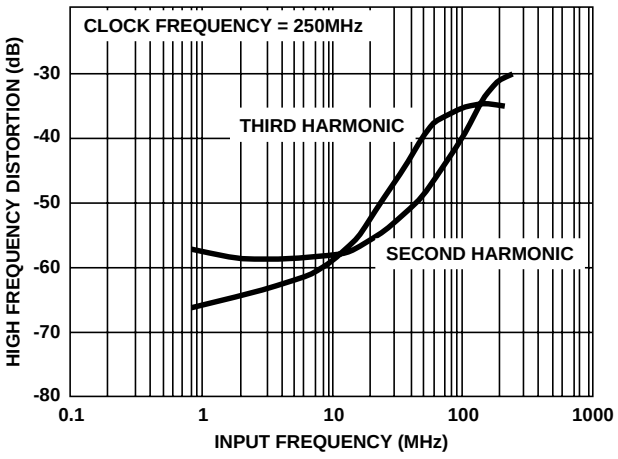


FIGURE 12. HARMONIC DISTORTION vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

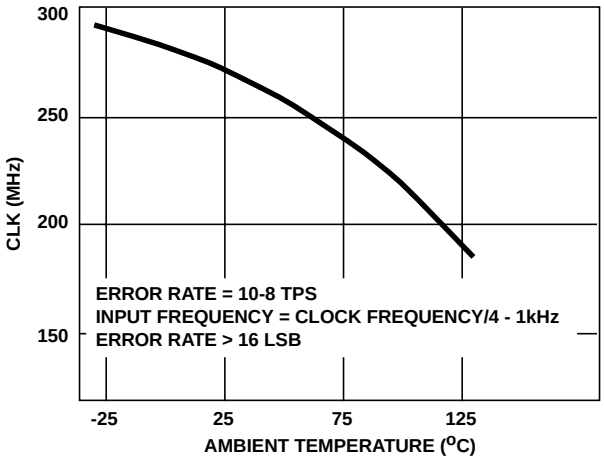


FIGURE 13. MAXIMUM CONVERSION RATE vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

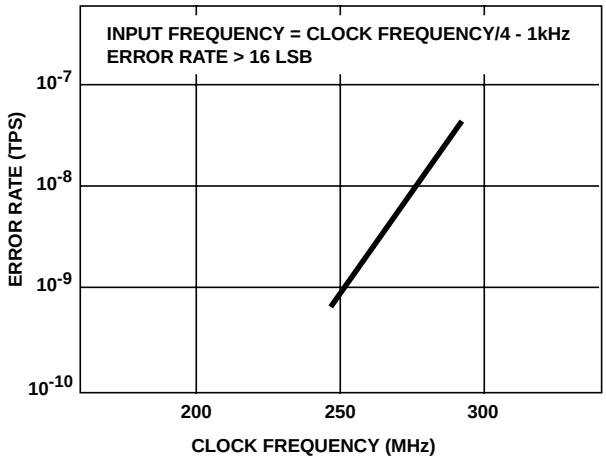


FIGURE 14. ERROR RATE vs CONVERSION RATE

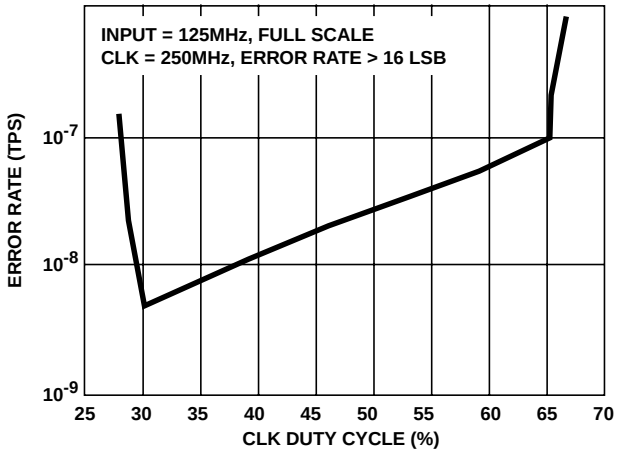


FIGURE 15. ERROR RATE vs CLOCK DUTY CYCLE

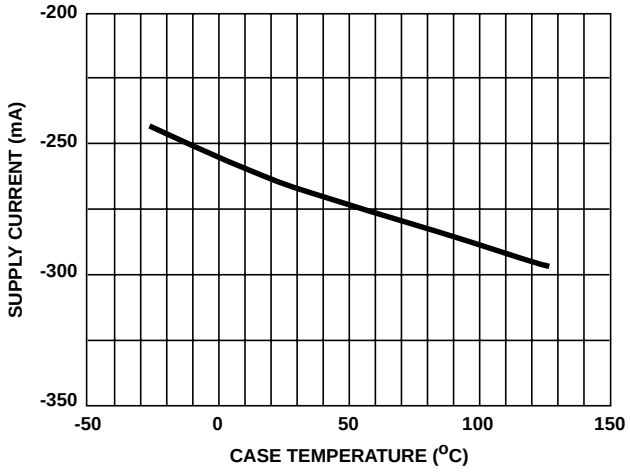
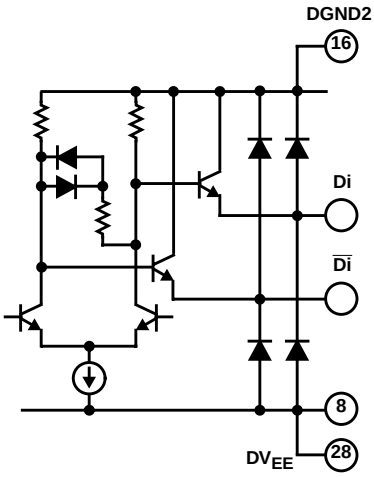
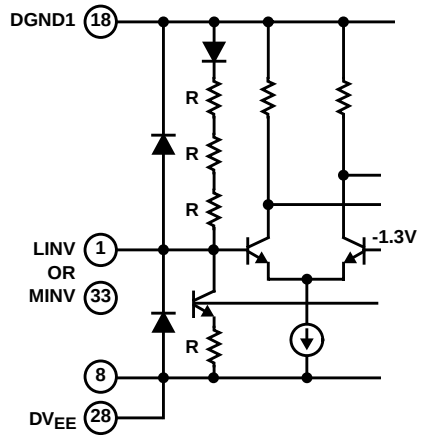
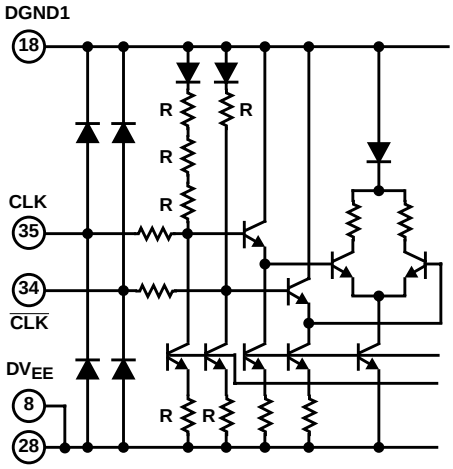
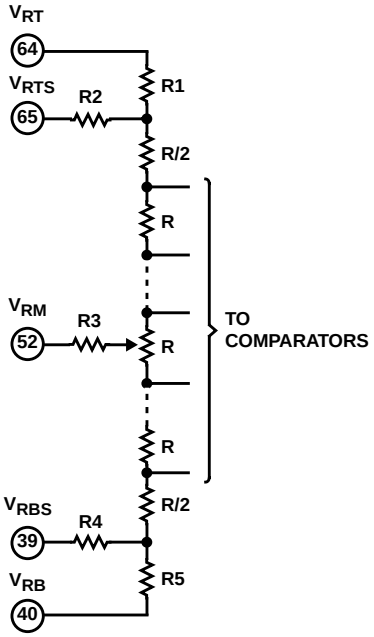


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

Pin Descriptions

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
4, 5	D0, $\overline{D0}$	O	ECL		LSB and complementary LSB output.
6, 7	D1, $\overline{D1}$				D1 to D6: Data Output. $\overline{D1}$ to $\overline{D6}$: Complementary Data Output.
12, 13	D2, $\overline{D2}$				
14, 15	D3, $\overline{D3}$				
19, 20	D4, $\overline{D4}$				
21, 22	D5, $\overline{D5}$				
29, 30	D6, $\overline{D6}$				
31, 32	D7, $\overline{D7}$				MSB Complementary MSB Data Output.
2, 3	OR, $\overline{OR}$				Overrange and Complementary Overrange Output.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	LINV	I	ECL		Polarity selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
33	MINV	I	ECL		Polarity selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
35	CLK	I	ECL		CLK Input.
34	$\overline{CLK}$	I	ECL		Complementary CLK Input. Pulled down to -1.3V when left open.
64	V_{RT}	I	0V		Analog Reference Voltage (Top) (0V Typ).
65	V_{RTS}	O	0V		Reference Voltage Sense (Top).
52	V_{RM}	I	$V_{RB/2}$		Reference Voltage Mid Point. Can be used for linearity compensation.
39	V_{RBS}	O	-2V		Reference Voltage Sense (Bottom).
40	V_{RB}	I	-2V		Analog Reference Voltage (Bottom).

Pin Descriptions (Continued)

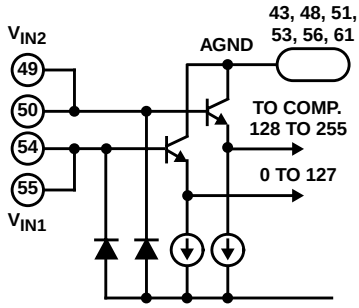
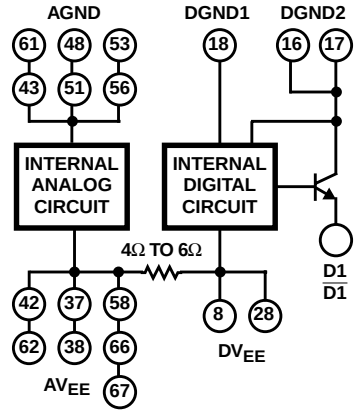
PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
49, 50 54, 55	V_{IN2} V_{IN1}	I	V_{RTS} to V_{RBS}		Analog Input. All of the pins must be wired externally.
43, 48, 51, 53, 56, 61	AGND		0V		Analog ground.
37, 38, 42, 58, 62, 66, 67	AV_{EE}		-5.2V		Analog supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
18	DGND1		0V		Digital ground.
16, 17	DGND2		0V		Digital ground for output drive.
8, 28	DV_{EE}		-5.2V		Digital supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).

TABLE 1. A/D OUTPUT CODE

V_{IN} (NOTE 6)	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000 • • • • • 00		0	100 • • • • • 00		0	011 • • • • • 11		0	111 • • • • • 11	
	0	1	000 • • • • • 00		1	100 • • • • • 00		1	011 • • • • • 11		1	111 • • • • • 11	
	1	1	000 • • • • • 01		1	100 • • • • • 01		1	011 • • • • • 10		1	111 • • • • • 10	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
-1V	127	1	011 • • • • • 11		1	111 • • • • • 11		1	000 • • • • • 00		1	100 • • • • • 00	
	128	1	100 • • • • • 00		1	000 • • • • • 00		1	111 • • • • • 11		1	011 • • • • • 11	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
	254	1	111 • • • • • 10		1	011 • • • • • 10		1	100 • • • • • 01		1	000 • • • • • 01	
	255	1	111 • • • • • 11		1	011 • • • • • 11		1	100 • • • • • 00		1	000 • • • • • 00	
-2V		1	111 • • • • • 11		1	011 • • • • • 11		1	100 • • • • • 00		1	000 • • • • • 00	

NOTE:

6. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$.

Test Circuits and Waveforms

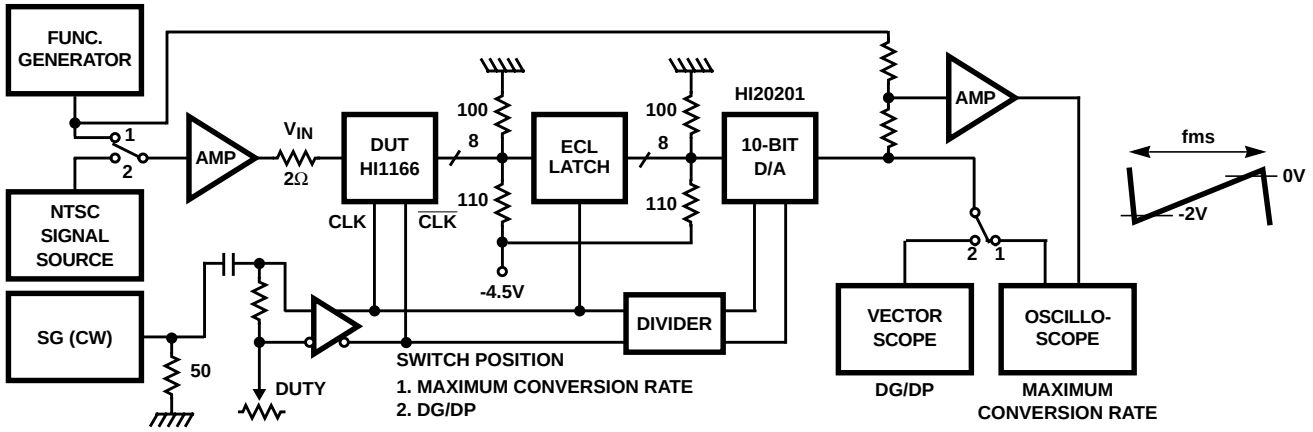


FIGURE 17. MAXIMUM CONVERSION RATE TEST CIRCUIT

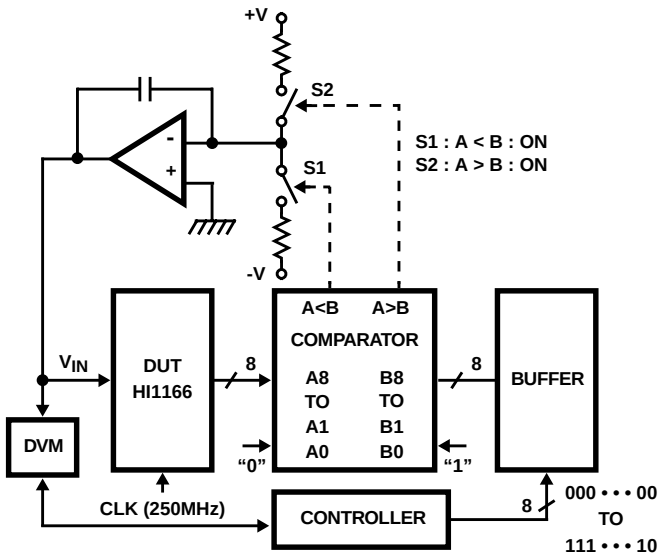


FIGURE 18. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits and Waveforms (Continued)

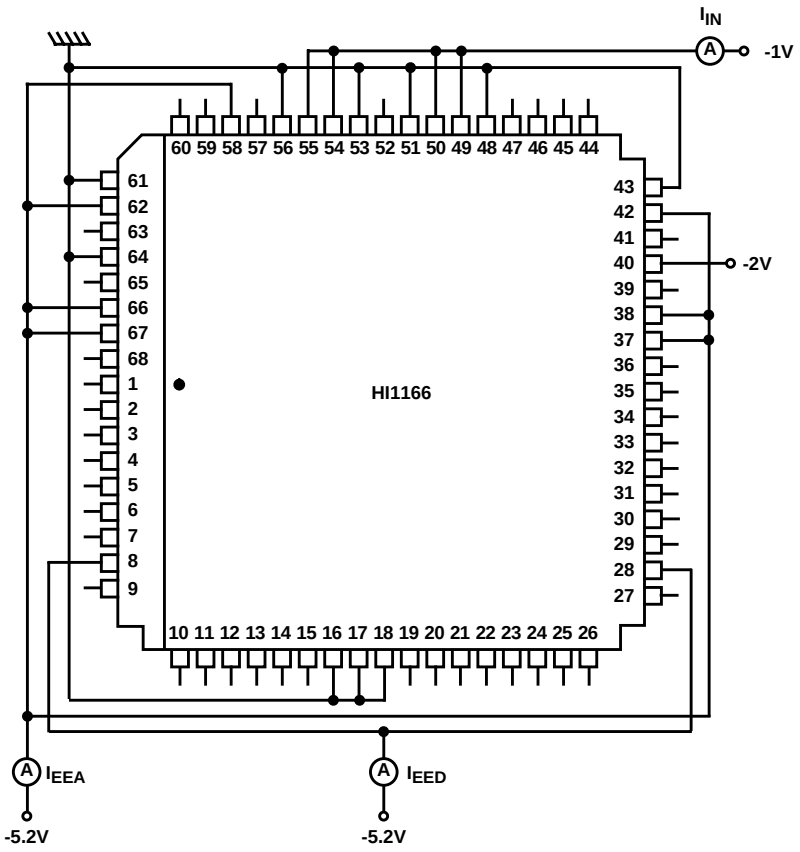


FIGURE 19. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

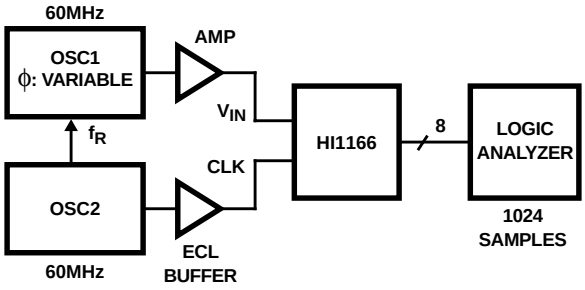
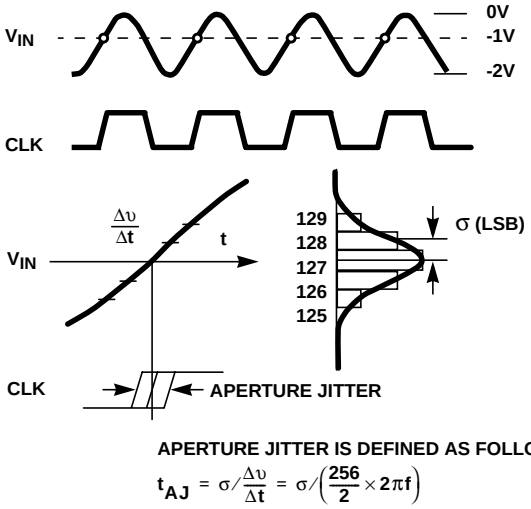


FIGURE 20A.



APERTURE JITTER IS DEFINED AS FOLLOWS:

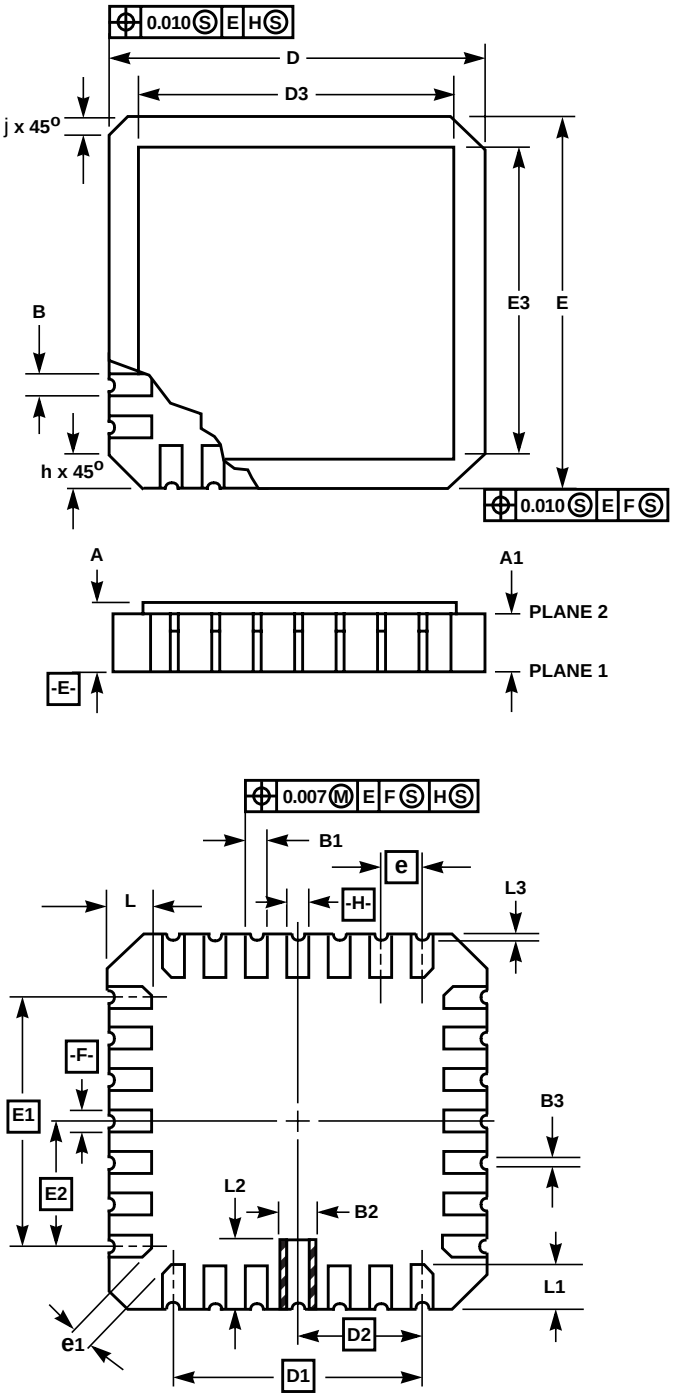
$$t_{AJ} = \sigma / \frac{\Delta\upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 20B. APERTURE JITTER TEST METHOD

FIGURE 20. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

Ceramic Leadless Chip Carrier Packages (CLCC)



J68.A

68 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.087	1.70	2.20	6, 7
A1	0.058	0.072	1.47	1.83	-
B	-	-	-	-	-
B1	0.033	0.039	0.85	0.99	2, 4
B3	0.006	0.022	0.15	0.56	-
D	0.940	0.965	23.88	24.51	-
D1	0.800 BSC		20.32 BSC		-
D2	0.400 BSC		10.16 BSC		-
D3	0.616	0.632	15.65	16.05	2
E	0.940	0.965	23.88	24.51	-
E1	0.800 BSC		20.32 BSC		-
E2	0.400 BSC		10.16 BSC		-
E3	0.616	0.632	15.65	16.05	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
j	0.040 Ref		1.00 Ref		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	17		17		3
NE	17		17		3
N	68		68		3

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NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.