HI1179

August 1997

8-Bit, 35 MSPS, Video A/D Converter

Features

- **Resolution 8-Bit . . . . . ±0.5 LSB (DNL)**
- **ENOB at f_{IN} = 1MHz . . . . . 7.6 Bits**
- **Maximum Sampling Frequency . . . . . 35 MSPS**
- **Low Power Consumption 80mW (at 35 MSPS Typ) (Reference Current Excluded)**
- **Built-In Input Clamp Function (DC Restore)**
- **No Sample/Hold Required**
- **Internal Voltage Reference**
- **Input CMOS Compatible**
- **Three-State TTL Compatible Output**
- **Single Power Supply . . . . . +5V**
- **Low Input Capacitance (Typ) 8pF**
- **Reference Impedance (Typ) 330Ω**
- **Direct Replacement for Sony CXD1179**

Applications

- **Desktop Video**
- **Multimedia**
- **Video Digitizing**
- **Image Scanners**
- **Low Cost High Speed Data Acquisition Systems**

Description

The HI1179 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 35 MSPS, allowing up to 8x over sampling of NTSC and PAL signals.

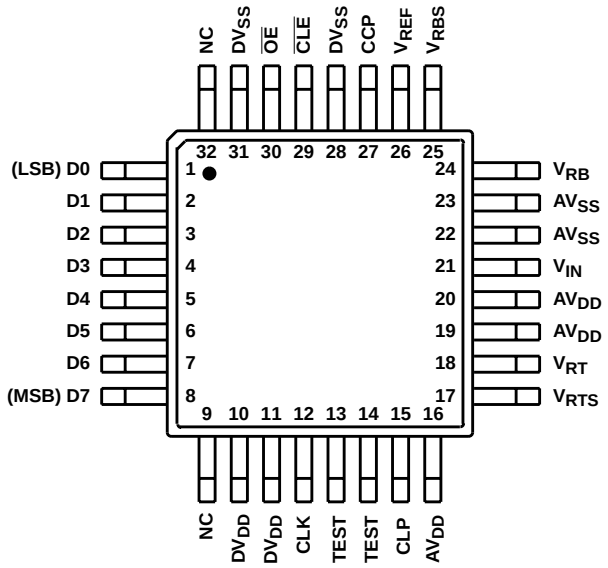
The HI1179 is available in the Industrial temperature range and is supplied in 32 lead Plastic Metric Quad Flatpack (MQFP) package. For lower sampling rates, refer to the HI1176 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI1179JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S
HI1179-EV	25	Evaluation Board	

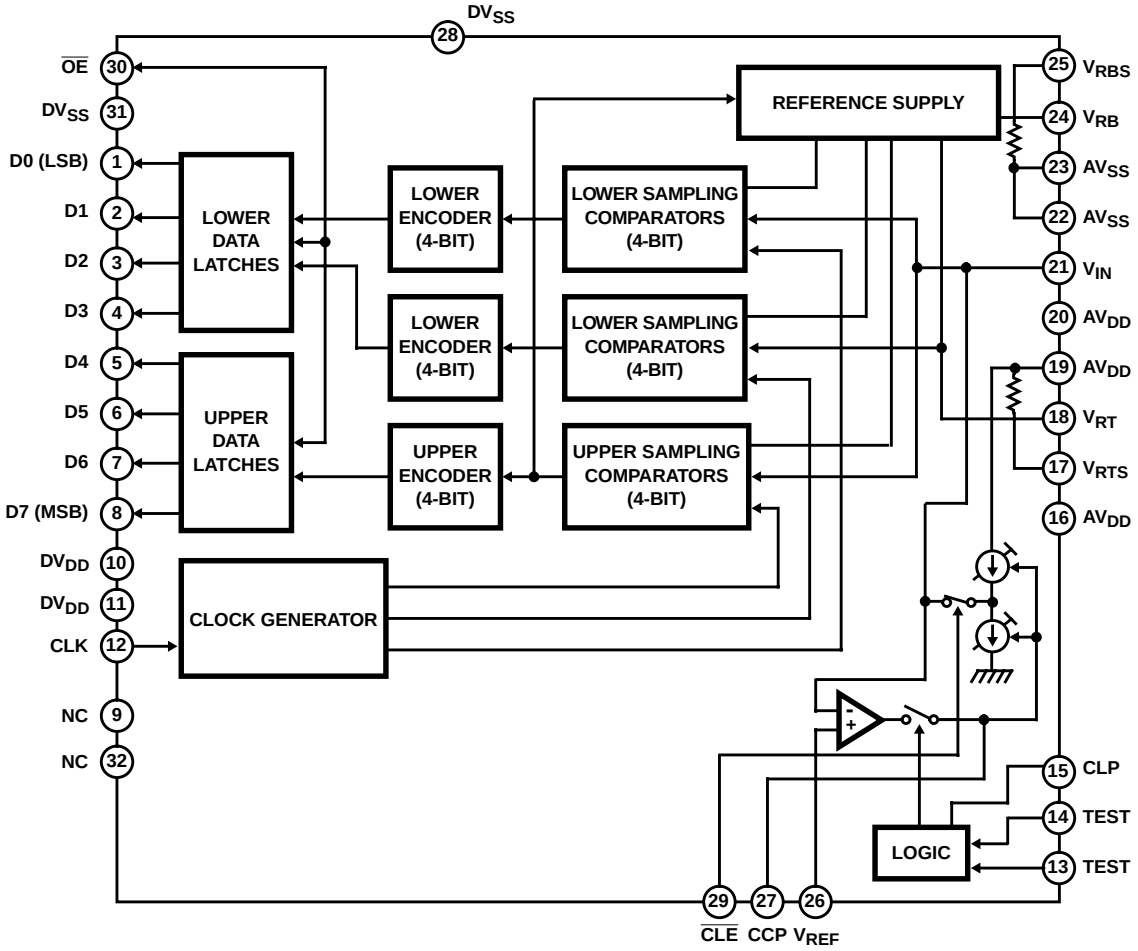
Pinout

HI1179 (MQFP)
TOP VIEW

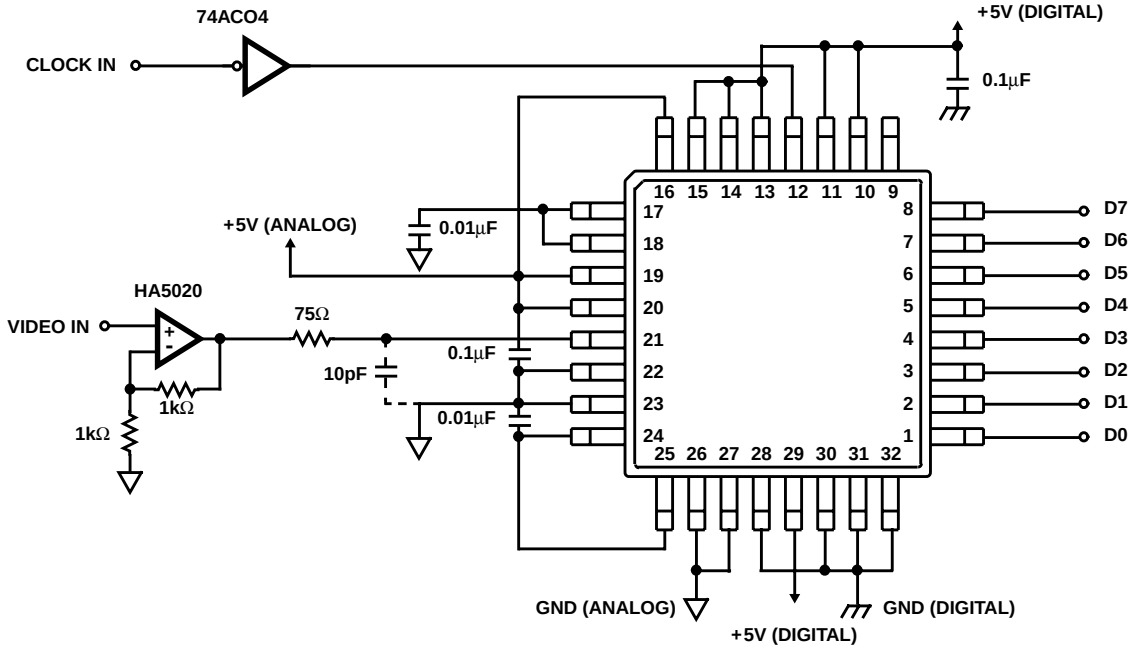


File Number **3666.3**

Functional Block Diagram



Typical Application Schematic



NON-CLAMP APPLICATION (INTERNAL REFERENCE USED)

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} . . . . . V_{DD} to V_{SS}
Digital Input Voltage . . . . . V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} to V_{SS}

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ^{o}C/W
MQFP Package 122
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range, T_{STG} . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

Recommended Operating Conditions (Note 2)

Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
|DGND-AGND| . . . . . .0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.7V and Below
Temperature Range, T_A . . . . . -40^{o}C to 85^{o}C
Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT} (1.8V_{P-P} to AV_{DD})
Clock Pulse Width
t_{PW1} . . . . . .14ns (Min)
t_{PW0} . . . . . .14ns (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25^{o}C (Note 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Maximum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	35	40	-	MSPS
Minimum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	-	-	0.5	MSPS
Integral Non-Linearity, INL	f_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-1.0	±0.5	+1.3	LSB
Differential Non-Linearity, DNL	f_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-0.5	±0.3	+0.5	LSB
DYNAMIC CHARACTERISTICS					
ENOB	f_{IN} = 1MHz	-	7.6	-	Bits
	f_{IN} = 5MHz	-	7.3	-	Bits
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Offset Voltage E_{OT}		-60	-40	-20	mV
E_{OB}		+55	+75	+95	mV
Sampling Delay, t_{SD}		-	2	-	ns
ANALOG INPUTS					
Analog Input Bandwidth, BW	-1dB	-	25	-	MHz
	-3dB	-	60	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + 0.07V_{RMS}	-	8	-	pF
REFERENCE INPUT					
Reference Pin Current, I_{REF}		4.5	6.1	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}		230	330	440	Ω

Electrical Specifications f_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 2) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCES						
Self Bias						
V_{RB}	Short V_{RB} to V_{RBS}, Short V_{RT} to V_{RTS}		0.52	0.56	0.60	V
V_{RT} - V_{RB}			1.96	2.10	2.24	V
V_{RT} - V_{RB}	Short V_{RT} to V_{RTS}, Short V_{RB} to AV_{SS}		2.13	2.33	2.53	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			3.5	-	-	V
V_{IL}			-	-	0.5	V
Digital Input Current						
I_{IH}	V_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min	V_{OH} = V_{DD} -0.5V	-1.1	-2.5	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	6.5	-	mA
Digital Output Leakage Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max	V_{OH} = V_{DD}	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_D	Load is One TTL Gate and 10pF Load		7	13	18	ns
Output Enable/Disable Delay	t_{PZH}, t_{PZL}	R_L = 1K, C_L = 15pF, $\overline{OE}$ = 5V → 0V	5	8	14	ns
	t_{PHZ}, t_{PLZ}	R_L = 1K, C_L = 15pF, $\overline{OE}$ = 0V → 5V	4	6.5	11	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 35 MSPS, NTSC Ramp Wave Input		-	16	22	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3µs	V_{REF} = 0.5V	-20	0	+20	mV
		V_{REF} = 2.5V	-30	-10	+10	mV
Clamp Pulse Delay, t_{CPD}			-	25	-	ns

NOTE:

3. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

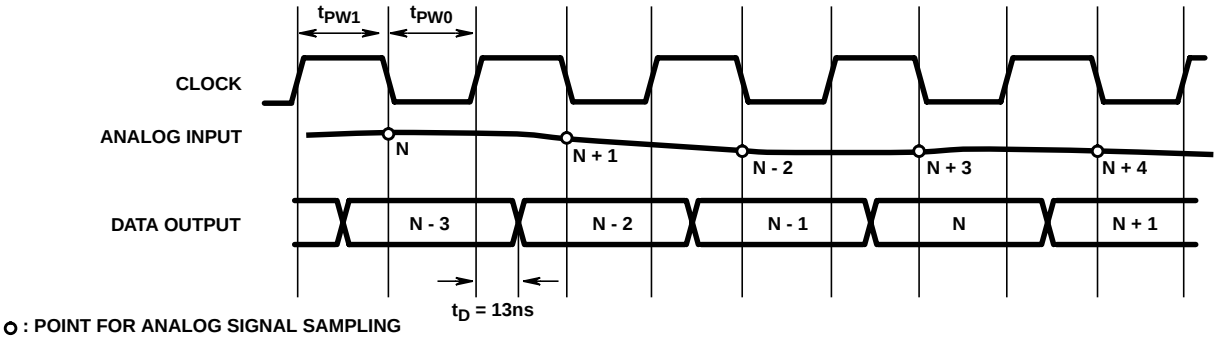


FIGURE 12.

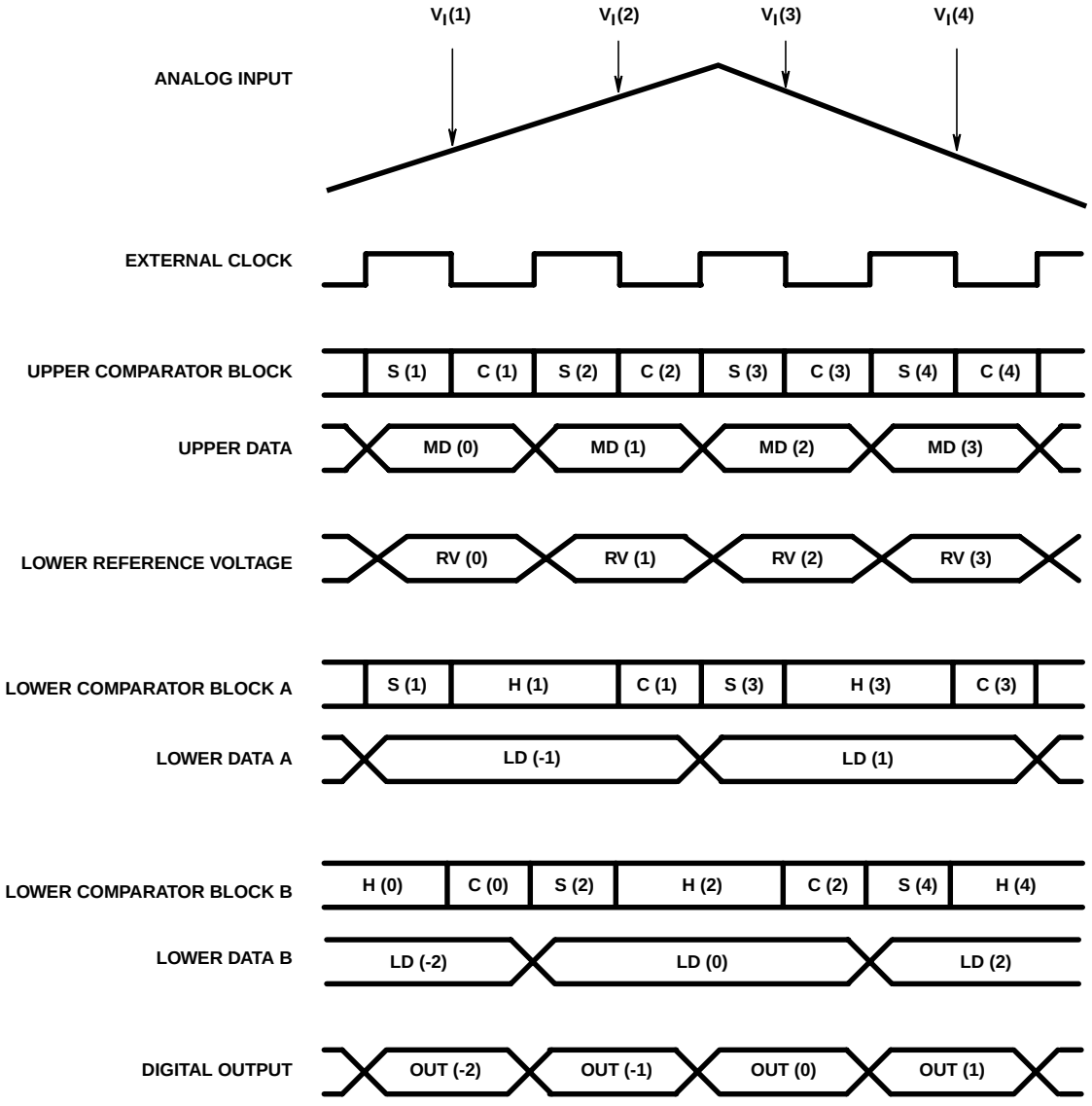


FIGURE 13.

Timing Diagrams (Continued)

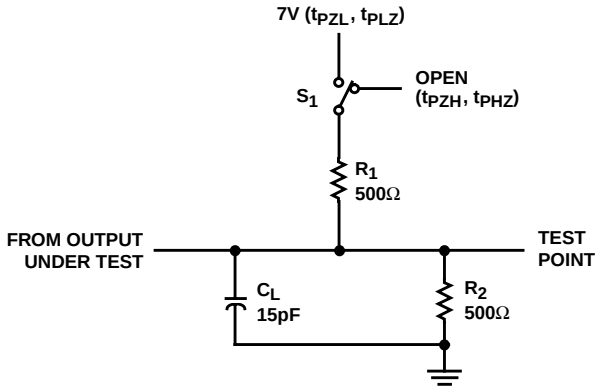


FIGURE 14A. THREE-STATE LOAD CIRCUIT

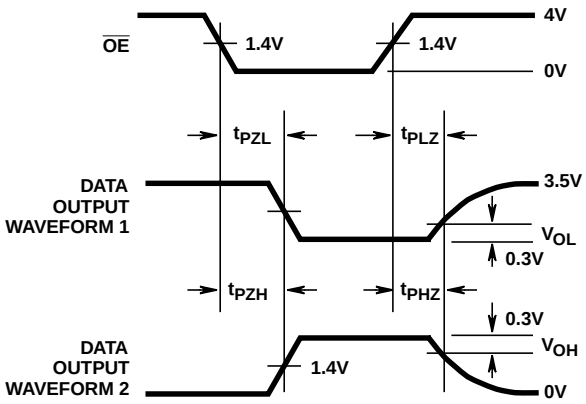


FIGURE 14B. THREE-STATE OUTPUT ENABLE/DISABLE TIMES

Typical Performance Curves f_C = 35 MSPS, T_A = 25°C, Unless Otherwise Specified

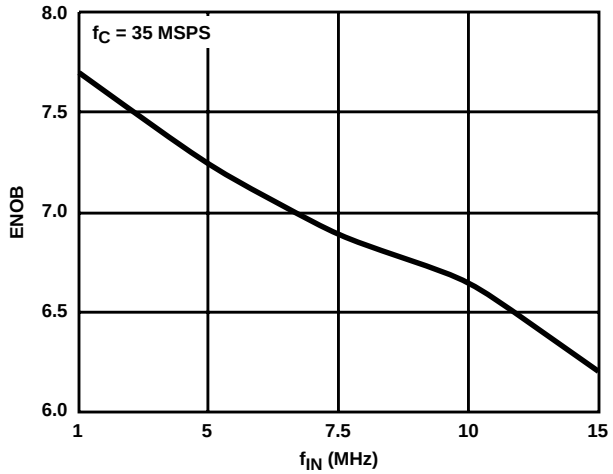


FIGURE 15. ENOB vs INPUT FREQUENCY

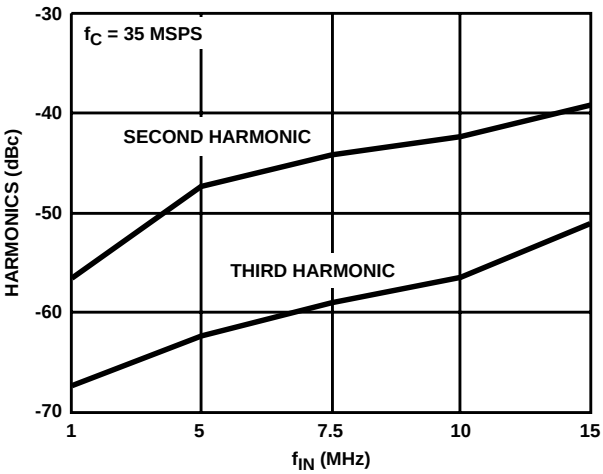


FIGURE 16. HARMONICS vs INPUT FREQUENCY

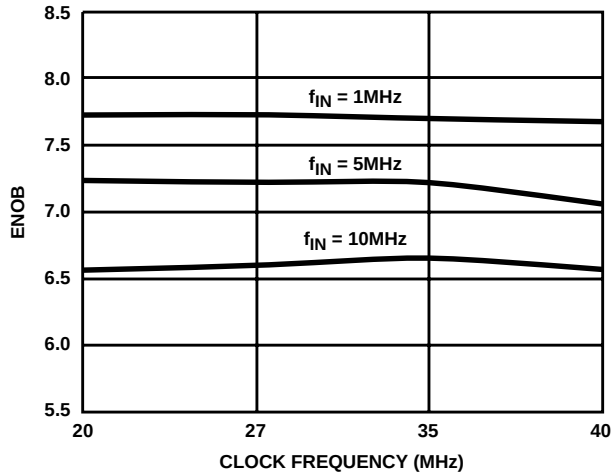


FIGURE 17. ENOB vs CLOCK FREQUENCY

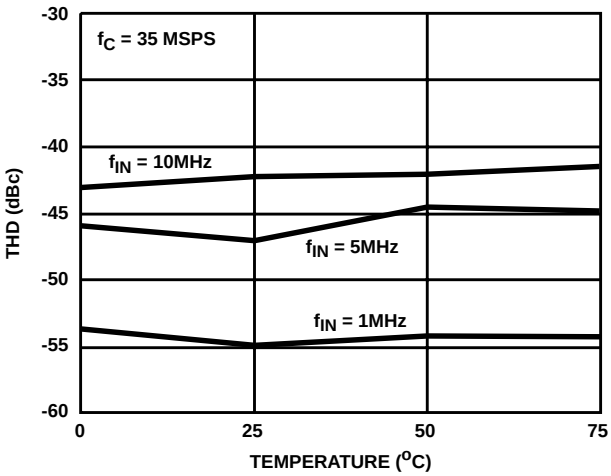


FIGURE 18. THD vs TEMPERATURE

Typical Performance Curves f_C = 35 MSPS, T_A = 25°C, Unless Otherwise Specified **(Continued)**

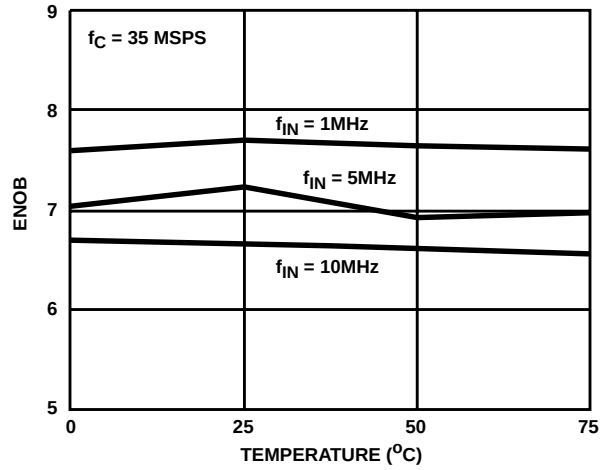


FIGURE 19. ENOB vs TEMPERATURE

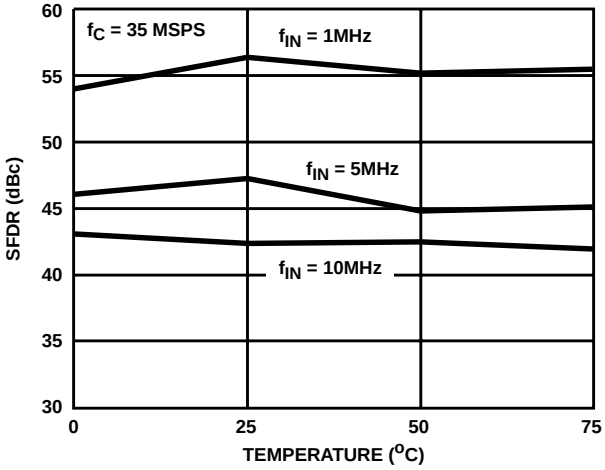


FIGURE 20. SFDR vs TEMPERATURE

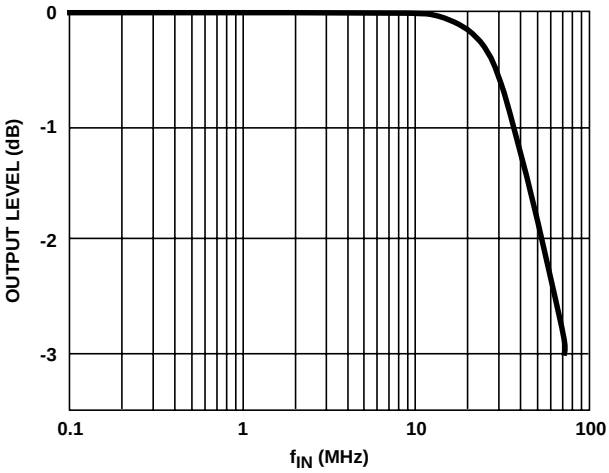


FIGURE 21. OUTPUT LEVEL vs INPUT FREQUENCY

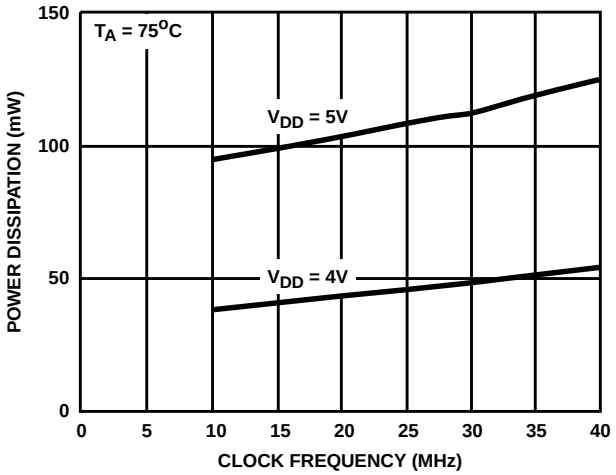
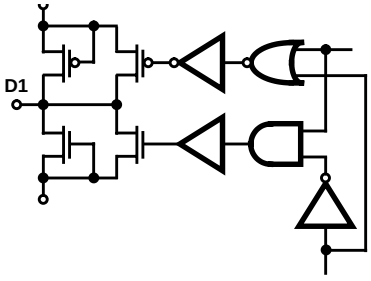
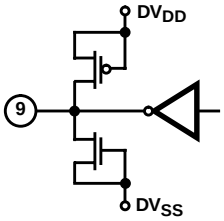
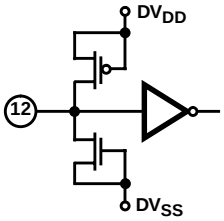
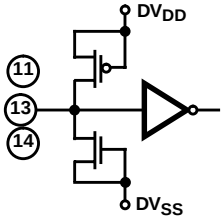
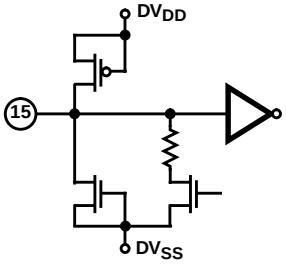
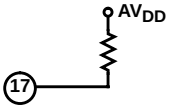
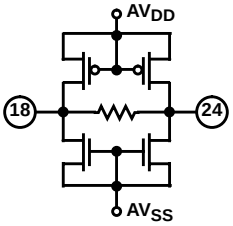


FIGURE 22. POWER DISSIPATION vs CLOCK FREQUENCY

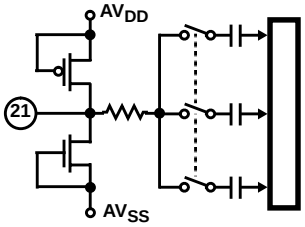
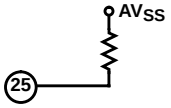
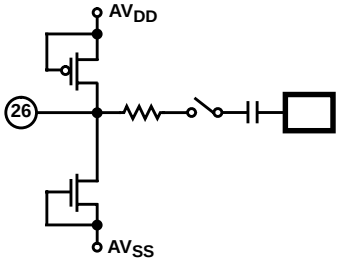
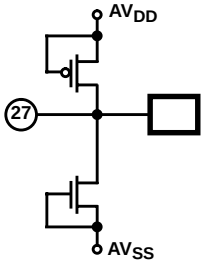
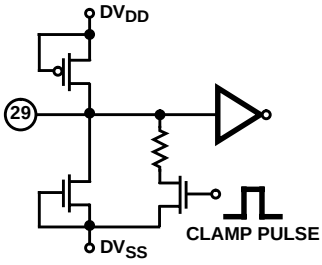
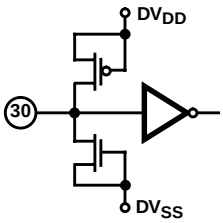
Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) output.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
9	NC		This pin must be left open. Used for test purposes only.
10	DV_{DD}		Digital +5V.
12	CLK		Clock Input.
11, 13, 14	TEST		Pin 11 must be connected to DV_{DD}. Pin 13, and Pin 14 must be connected to DV_{DD} or DV_{SS}. Used for test purposes only.
15	CLP		Clamp Pulse Input. The input signal voltage is clamped to V_{REF} while the clamp pulse is low.
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approximately +2.6V.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog Input.
22, 23	AV_{SS}		Analog Ground.
25	V_{RBS}		When shorted with V_{RB}, generates approximately +0.5V.
26	V_{REF}		Clamp Reference Voltage Input.
27	CCP		Integrates the voltage for clamp control. CCP and V_{IN} voltage changes are in phase.
28, 31	DV_{SS}		Digital ground.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	255	1	1	1	1	1	1	1	1
	•					•			
	•					•			
	•					•			
	•								
	128	1	0	0	0	0	0	0	0
	127	0	1	1	1	1	1	1	1
	•					•			
	•					•			
	•					•			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1179 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between VRT-VRB is constantly applied to the upper 4-bit comparator group. VI(1) is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples VI(1) on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 clock cycle delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

Separate analog and digital grounds to reduce noise effects, connecting them at a single point near the HI1179. Analog and digital power should also be separated for optimum performance. If a single 5V supply is used, isolate the analog and digital power with an inductor or ferrite bead to minimize the digital noise on the analog supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The analog input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with a low impedance source with sufficient bandwidth and drive capability.

Op amps such as the HA-2544, the HA5020 and the HFA1100 family should make excellent input amplifiers depending on the applications requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

The input can be AC or DC coupled. If AC coupled the input will float to about $^1/_2(V_{RT} + V_{RB})$. The other option is to use the internal clamp, which will be discussed later. When DC coupling the input be sure to disable the clamp function ($\overline{CLE}$, pin 29).

Reference Input

The HI1179 has an internal reference with the option to use an external reference if more accuracy is desired.

The analog input range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal reference can be used by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. The internal bias generator will set V_{RT} to about 2.6V and V_{RB} to about 0.6V. The analog input range of the A/D will now be from 0.6V to 2.6V. The internal reference may be subjected to power supply variations since the internal reference resistor ladder is connected directly to V_{DD} and V_{SS}. Any supply variations can be minimized by good decoupling of V_{RT} and V_{RB}.

An external reference can be used for increased accuracy, by connecting the reference voltage to V_{RT} and V_{RB}. If an external reference is used, V_{RT} should be keep below 2.8V and (V_{RT} - V_{RB}) should be less than 2.8V and greater than 1.8V. If a V_{RB} below +0.6V is used the linearity of the part may degrade. An ICL8069 reference and a dual op amp, with outputs connect to V_{RT} and V_{RB}, makes a good, low cost external reference.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor when using either internal or external references.

Clamp Operation

The HI1179 provides a clamp (DC restore) option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin before the signal is digitized. The clamp

function is enabled by tying $\overline{CLE}$ low. In this case a negative going pulse is sent to the CLP pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 15 shows the HI1179 configured for this mode of operation.The clamp pulse is latched by the ADC sampling clock through an external latch. This is not necessary to the operation of the clamp function but in video applications, if this is not done, then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency. The pulse width of the input clamp pulse will depend on the input signal. For example, a 1µs pulse width will allow the user to clamp the back porch of an NTSC input signal to the reference voltage, V_{REF}.

The clamp can be disabled by tying $\overline{CLE}$ high and then the HI1179 acts like a normal A/D converter, accepting a DC coupled input. The Typical Application Schematic illustrates the operation of HI1179 when the clamp function is not used.

Additional information on the HI1179 is available in Application Note 9407, “Using the HI1176/HI1179 Evaluation Board”.

Test Circuits

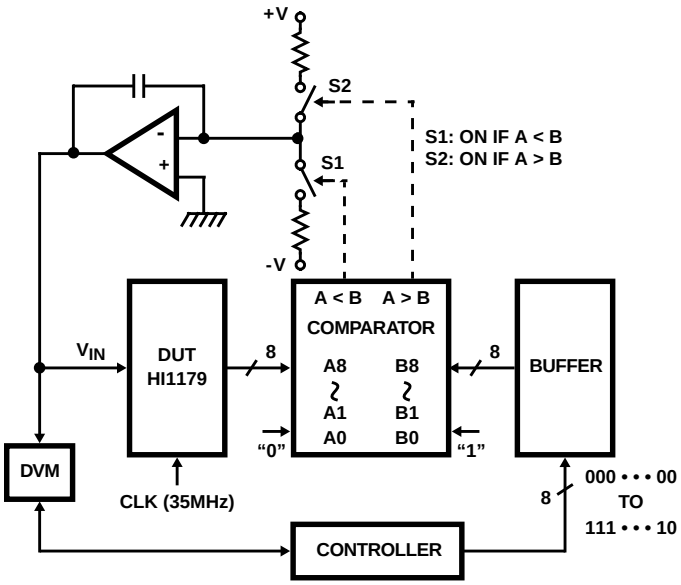


FIGURE 23. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

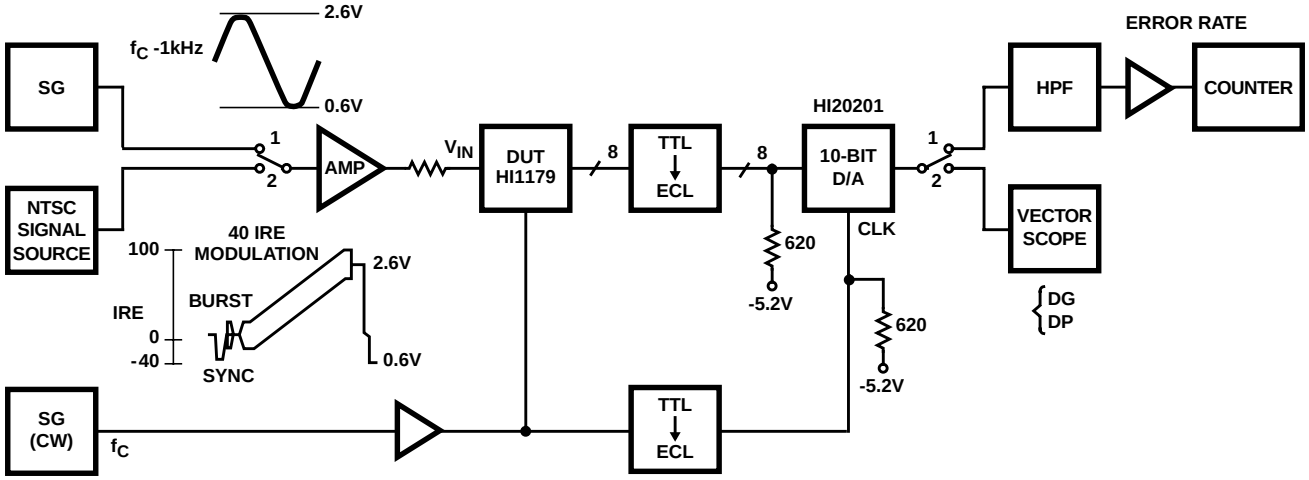


FIGURE 24. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

Test Circuits (Continued)

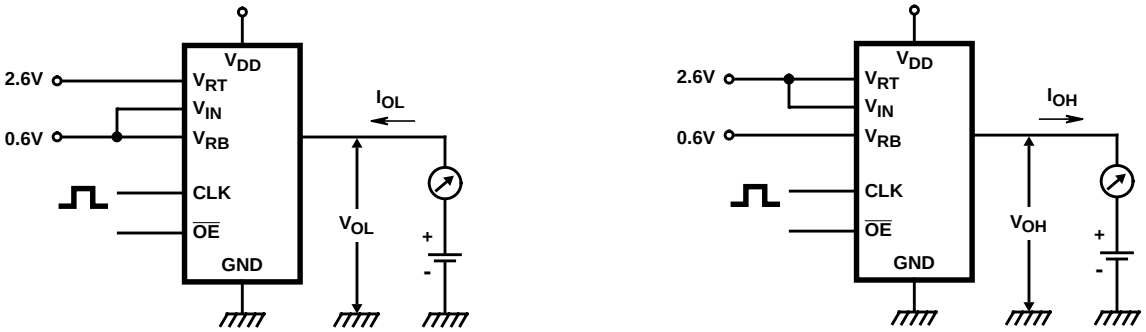


FIGURE 25A. FIGURE 25B.

FIGURE 25. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Typical Application Circuits

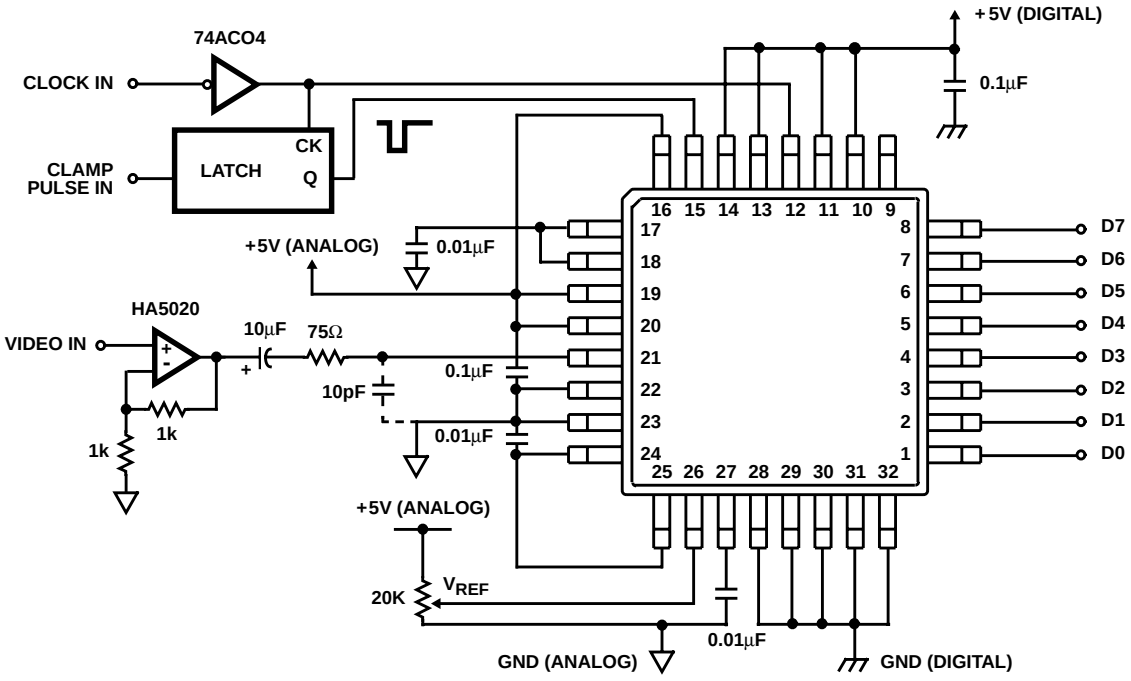
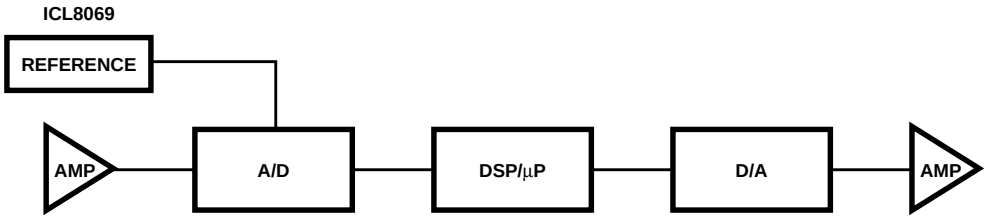


FIGURE 26. INPUT CLAMP APPLICATION (INTERNAL REFERENCE USED)

Typical Application Circuits (Continued)



HA5020 (Single)	HI1179 (8-Bit)	HSP9501	HI1171 (8-Bit)	HA5020 (Single)
HA5022 (Dual)		HSP48410	CA3338 (8-Bit)	HA2842 (Single)
HA5024 (Quad)		HSP48908		HFA1115 (Single)
HA5013 (Triple)		HSP48901		HFA1212 (Dual)
HFA1105 (Single)		HSP48212		HFA1412 (Quad)
HFA1205 (Dual)		HSP43881		
HFA1405 (Quad)		HSP43168		

HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution, 4K x 4K Frame Size
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP48212: Video Mixer
HSP43881: Digital Filter, 30MHz, 1-D and 2-D FIR Filters
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz

CMOS Logic Available in HC, HCT, AC, ACT and FCT.

FIGURE 27. 8-BIT VIDEO COMPONENTS

Static Performance Definitions

Offset, full-scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Offset Error (VOS)

The first code transition should occur at a level $^1/_2$ LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive full scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI1179. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 1024 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion

This is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Sampling Delay (t_{SD})

Sampling delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the sampling delay due to variation of internal clock path delays.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is available after 2.5 cycles of the clock. This is due to the architecture of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 2.5 cycles.

Output Data Delay (t_D)

Output Data Delay is the delay time from when the data is valid (rising clock edge) to when it shows up at the output bus. This is due to internal delays at the digital output.

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