

HI-506A, HI-507A HI-508A, HI-509A

16-Channel, 8-Channel, Differential 8-Channel and Differential 4-Channel, CMOS Analog MUXs with Active Overvoltage Protection

August 1997

Features

- Analog Overvoltage 70V_{p-p}
- No Channel Interaction During Overvoltage
- Maximum Power Supply 44V
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range $\pm 15V$
- Access Time 500ns
- Power Dissipation 7.5mW

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0506A-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0506A-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0506A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0506A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0507A-8	-55 to 125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0507A-5	0 to 75	28 Ld PDIP	E28.6
HI1-0508A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI1-0508A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0508A-5	+0 to 75	16 Ld PDIP	E16.3
HI1-0509A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0509A-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0509A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI1-0509A-8	-55 to 125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0509A-5	0 to 75	16 Ld PDIP	E16.3

Description

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70V_{p-p} levels with $\pm 15V$ supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1k Ω of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16 channel multiplexer, the HI-507A is an 8-Channel differential multiplexer, the HI-508A is a single 8 channel multiplexer and the HI-509A is a differential 4-Channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

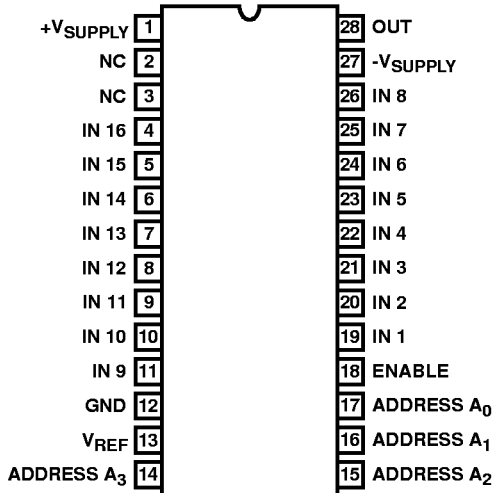
The HI-506A/507A devices are available in a 28 lead Plastic or Ceramic DIP and the HI-508A/509A devices are available in a 16 lead Plastic or Ceramic DIP package.

The HI-50XA are offered in industrial/commercial and military grades, additional Hi-Rel screening including 160 hour burn-in is specified by the "8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 or HI-549/883 data sheets.

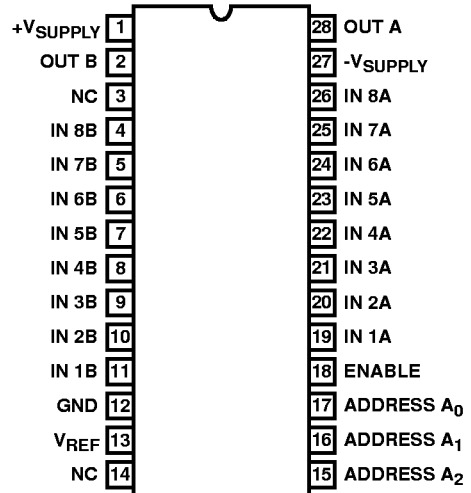
HI-506A, HI-507A, HI-508A, HI-509A

Pinouts

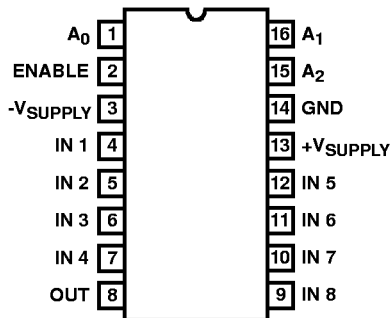
HI1-506A (CERDIP)
HI3-506A (PDIP)
TOP VIEW



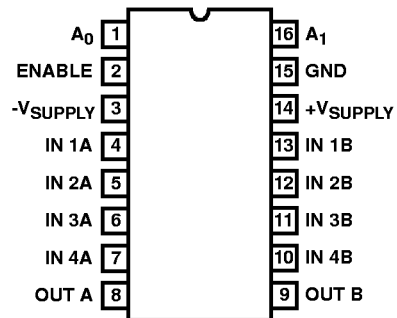
HI1-507A (CERDIP)
HI3-507A (PDIP)
TOP VIEW



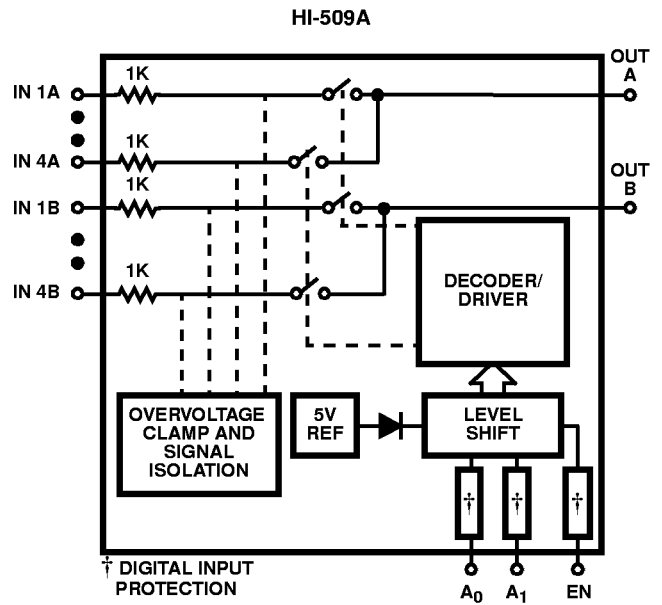
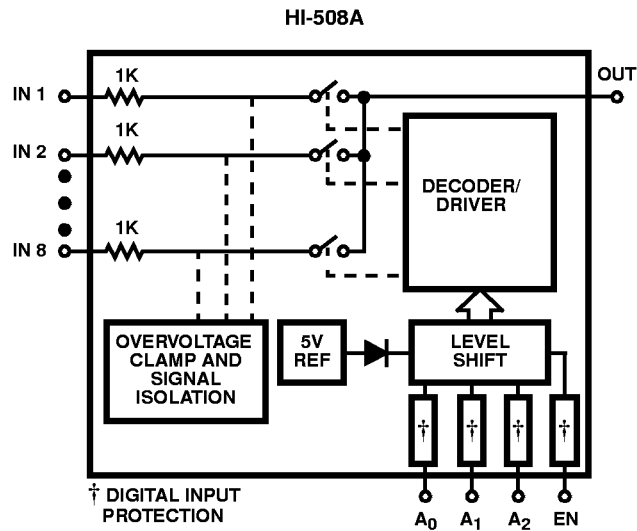
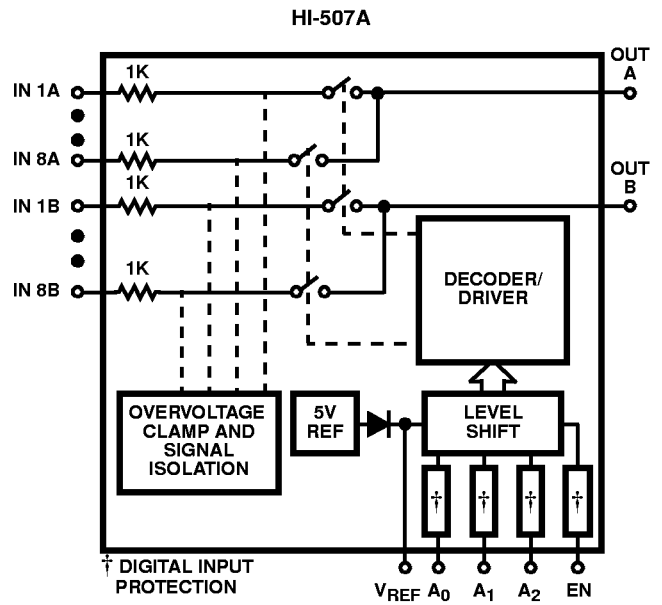
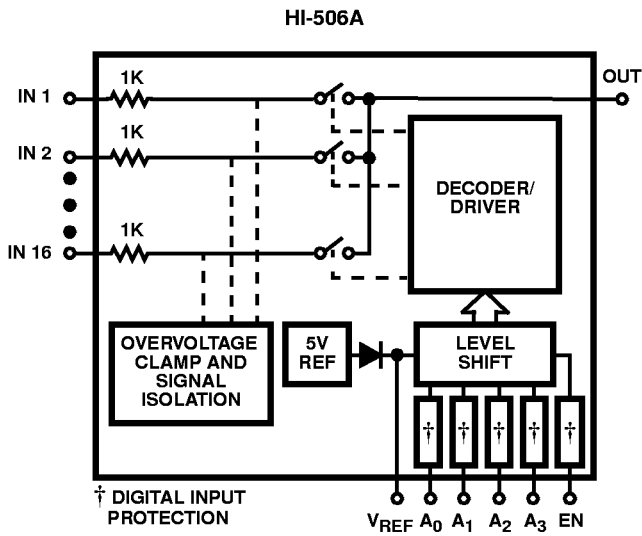
HI1-508A (CERDIP)
HI3-508A (PDIP)
TOP VIEW



HI1-509A (CERDIP)
HI3-509A (PDIP)
TOP VIEW

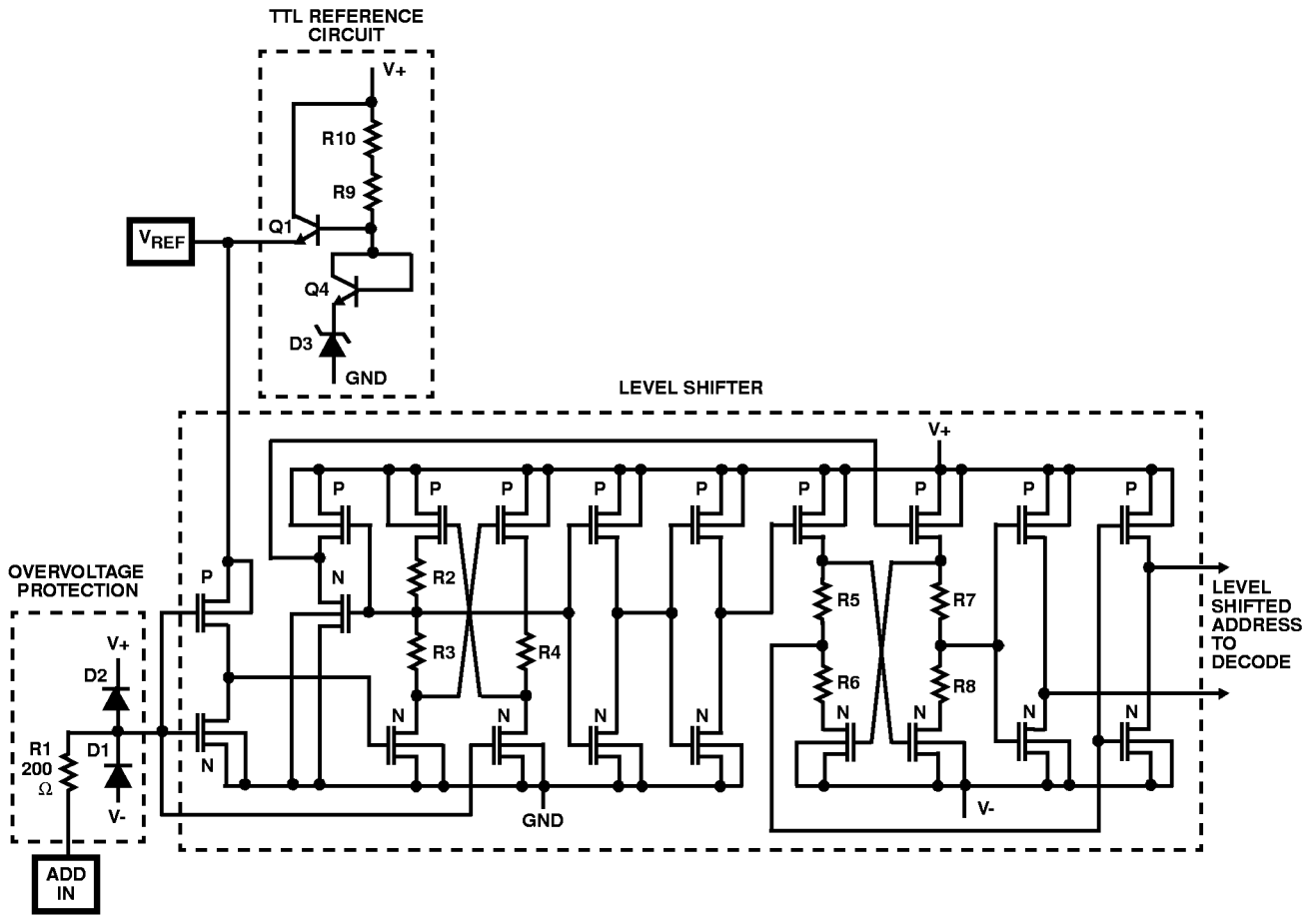


Functional Diagrams

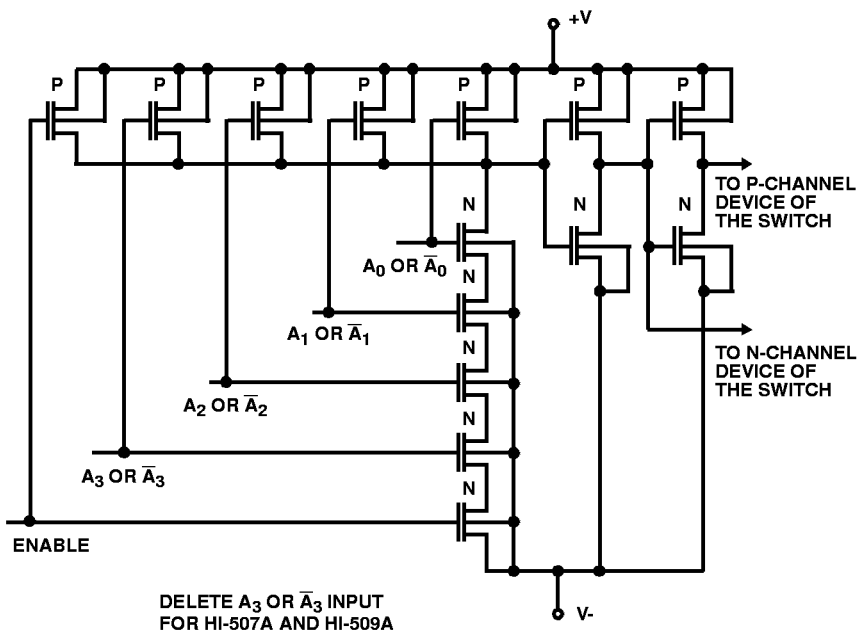


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

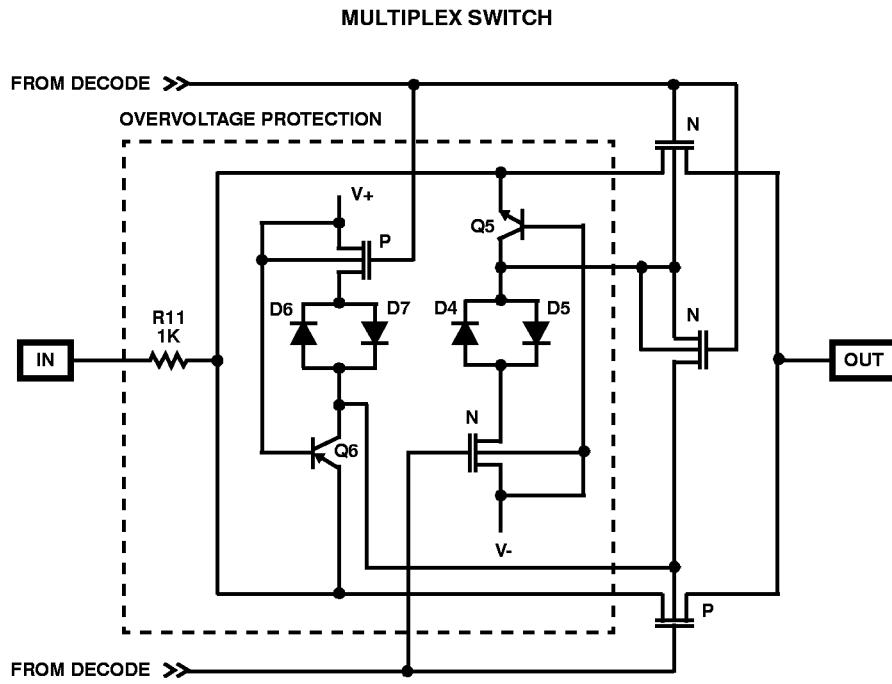


ADDRESS DECODER



DELETE A₃ OR \bar{A}_3 INPUT FOR HI-507A AND HI-509A

Schematic Diagrams (Continued)



HI-506A, HI-507A, HI-508A, HI-509A

Absolute Maximum Ratings

V _{SUPPLY(+)} to V _{SUPPLY(-)}	+44V
V _{SUPPLY(+)} to GND	+22V
V _{SUPPLY(-)} to GND	+25V
Digital Input Overvoltage	
+V _{EN} , +V _A	+V _{SUPPLY} +4V
-V _{EN} , -V _A	-V _{SUPPLY} -4V
	or 20mA, Whichever Occurs First
Analog Signal Overvoltage	
+V _S	+V _{SUPPLY} +20V
-V _S	-V _{SUPPLY} -20V
Continuous Current, S or D	20mA
Peak Current, S or D	40mA
	Pulsed at 1ms, 10% Duty Cycle (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld CERDIP Package (HI-506A, HI-507A)	55	18
16 Ld CERDIP Package (HI-508A, HI-509A)	85	32
28 Ld PDIP Package (HI-506A, HI-507A)	60	N/A
16 Ld PDIP Package (HI-508A, HI-509A)	100	N/A
Maximum Junction Temperature		
CERDIP Package		175°C
PDIP Package		150°C
Maximum Storage Temperature Range		-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)		300°C

Operating Conditions

Temperature Ranges

HI-506A/507A/508A/509A-2, -8	-55°C to 125°C
HI-506A/507A/508A/509A-5, -7	0°C to 75 °C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEMP (°C)	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Access Time, t_A (Note 2)	25	-	0.5	-	-	0.5	-	μ s
	Full	-	-	1.0	-	-	1.0	μ s
Break-Before-Make Delay, t_{OPEN} (Note 2)	25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$ (Note 2)	25	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$ (Note 2)	25	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506A and HI-507A)	25	-	1.2	-	-	1.2	-	μ s
Settling Time to 0.01%, t_S (HI-506A and HI-507A)	25	-	3.5	-	-	3.5	-	μ s
Settling Time to 0.1%, t_S (HI-508A and HI-509A)	25	-	1.2	-	-	1.2	-	μ s
Settling Time to 0.01%, t_S (HI-508A and HI-509A)	25	-	3.5	-	-	3.5	-	μ s
"Off Isolation" (Note 7)	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$	25	-	12	-	-	12	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506A)	25	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507A)	25	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508A)	25	-	25	-	-	25	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509A)	25	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A	25	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$	25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold, TTL Drive, V _{AL} (Note 2)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V _{AH} (Notes 2, 9)	Full	+4.0	-	-	+4.0	-	-	V

HI-506A, HI-507A, HI-508A, HI-509A

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEMP (°C)	HI-50XA-2, -8			HI-50XA-5, -7			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Input Leakage Current (High or Low), I _A (Notes 2, 6)	Full	-	-	1.0	-	-	1.0	μA	
MOS Drive, V _{AL} , HI-506A/HI-507A (Note 10)	25	-	-	0.8	-	-	0.8	V	
MOS Drive, V _{AH} , HI-506A/HI-507A (Note 10)	25	6.0	-	-	6.0	-	-	V	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V _S (Note 2)	Full	-15	-	+15	-15	-	+15	V	
On Resistance, r _{ON} , (Notes 2, 3)	25	-	1.2	1.5	-	1.5	1.8	kΩ	
	Full	-	1.5	1.8	-	1.8	2.0	kΩ	
Off Input Leakage Current, I _{S(OFF)} (Notes 2, 4)	25	-	0.03	-	-	0.03	-	nA	
	Full	-	-	50	-	-	50	nA	
Off Output Leakage Current, I _{D(OFF)} (Notes 2, 4)	25	-	0.1	-	-	0.1	-	nA	
	HI-506A	Full	-	-	300	-	-	300	nA
	HI-507A	Full	-	-	200	-	-	200	nA
	HI-508A	Full	-	-	200	-	-	200	nA
	HI-509A	Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, I _{D(OFF)} (Note 5)	25	-	4.0	-	-	4.0	-	nA	
	Full	-	-	2.0	-	-	-	μA	
On Channel Leakage Current, I _{D(ON)} (Notes 2, 4)	25	-	0.1	-	-	0.1	-	nA	
	HI-506A	Full	-	-	300	-	-	300	nA
	HI-507A	Full	-	-	200	-	-	200	nA
	HI-508A	Full	-	-	200	-	-	200	nA
	HI-509A	Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I _{DIFF} , (HI-507A, HI-509A Only)	Full	-	-	50	-	-	50	nA	
POWER REQUIREMENTS									
Current, I ₊ , Pin 1 (Notes 2, 8)	Full	-	1.5	2.0	-	1.5	2.0	mA	
Current, I ₊ , HI-508A/HI-509A (Notes 2, 8)	Full	-	1.5	2.4	-	1.5	2.0	mA	
Current, I ₋ , Pin 27 (Notes 2, 8)	Full	-	0.02	1.0	-	0.02	1.0	mA	
Power Dissipation, P _D	Full	-	7.5	-	-	7.5	-	mW	

NOTES:

2. 100% tested for Dash 8. Leakage currents not tested at -55°C.
3. V_{OUT} = ±10V, I_{OUT} = ±100μA.
4. 10nA is the practical lower limit for high speed measurement in the production test environment.
5. Analog Overvoltage = ±33V.
6. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
7. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz.
8. V_{EN}, V_A = 0V or 4V.
9. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V supply are recommended.
10. V_{REF} = +10V.

HI-506A, HI-507A, HI-508A, HI-509A

Typical Performance Curves and Test Circuits $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified

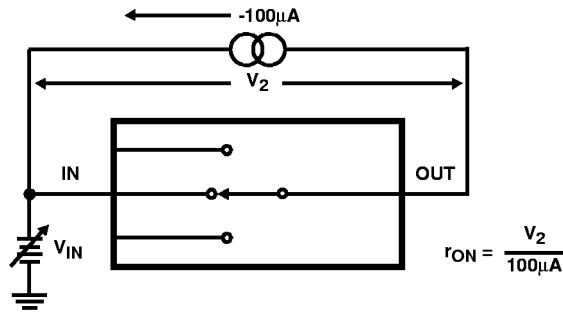


FIGURE 1A. TEST CIRCUIT

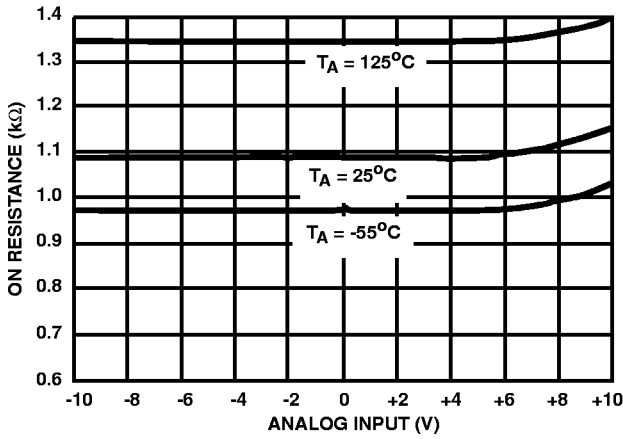


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

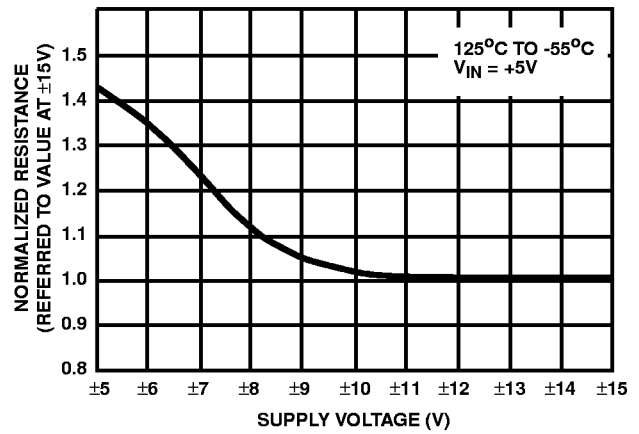


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

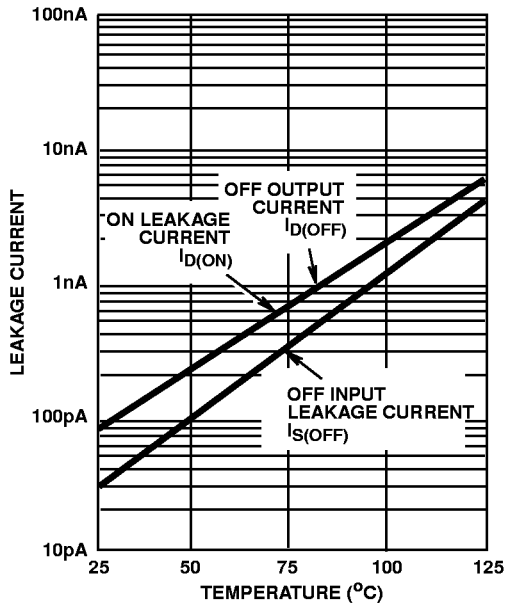


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

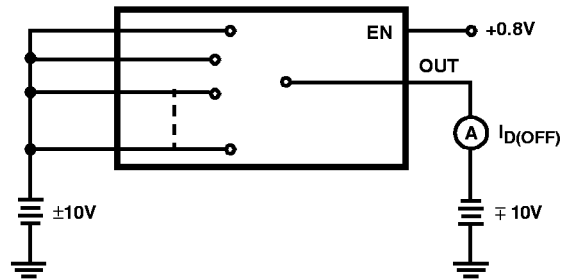


FIGURE 2B. $I_{\text{D(OFF)}}$ (NOTE 1)

Typical Performance Curves and Test Circuits

$T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$,
Unless Otherwise Specified (Continued)

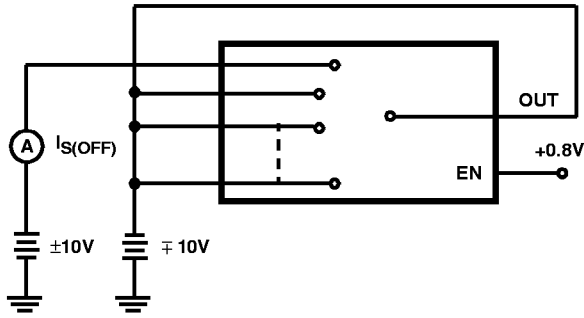


FIGURE 2C. $I_{\text{S(OFF)}}$ TEST CIRCUIT (NOTE 1)

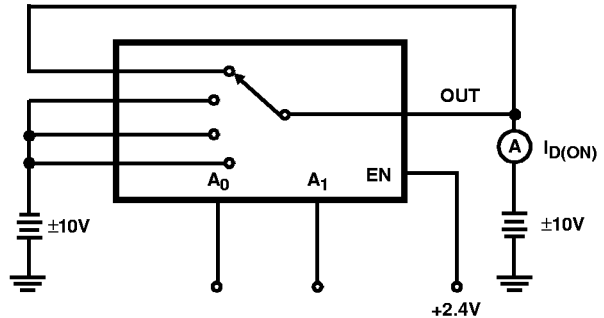


FIGURE 2D. $I_{\text{D(ON)}}$ TEST CIRCUIT (NOTE 1)

NOTE:

- Two measurements per channel: $\pm 10\text{V}$ and $\mp 10\text{V}$. (Two measurements per device for $I_{\text{D(OFF)}}$ $\pm 10\text{V}$ and $\mp 10\text{V}$.)

FIGURE 2. LEAKAGE CURRENTS

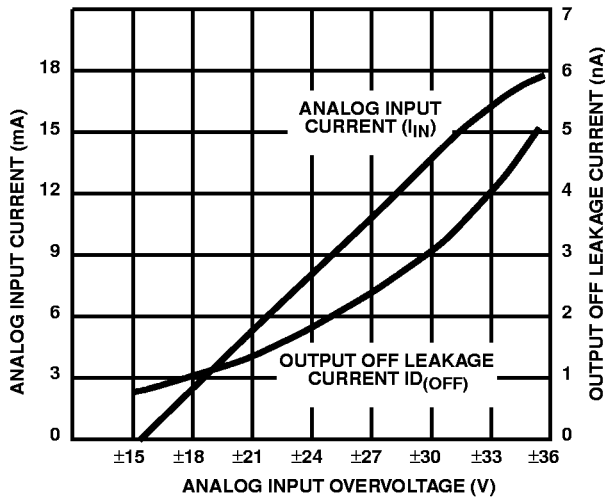


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

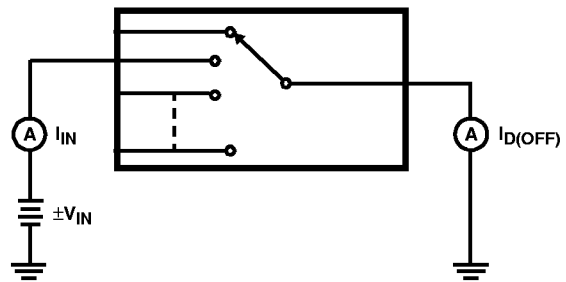


FIGURE 3B. TEST CIRCUIT

FIGURE 3. OVERVOLTAGE CHARACTERISTICS

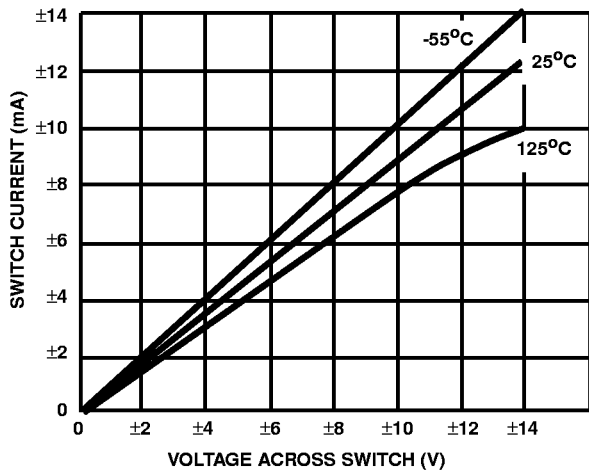


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

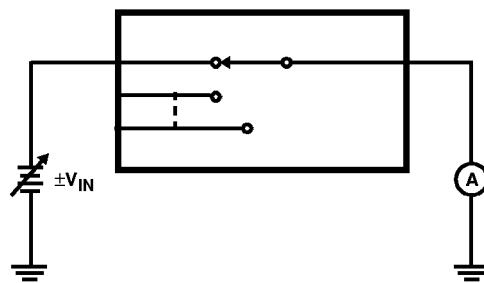


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Typical Performance Curves and Test Circuits $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified (Continued)

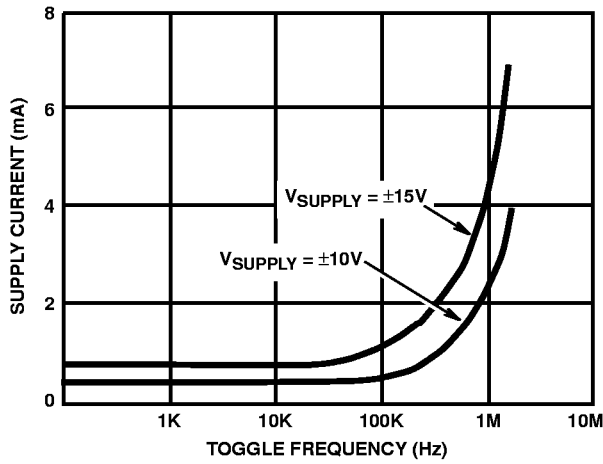


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. SUPPLY CURRENTS

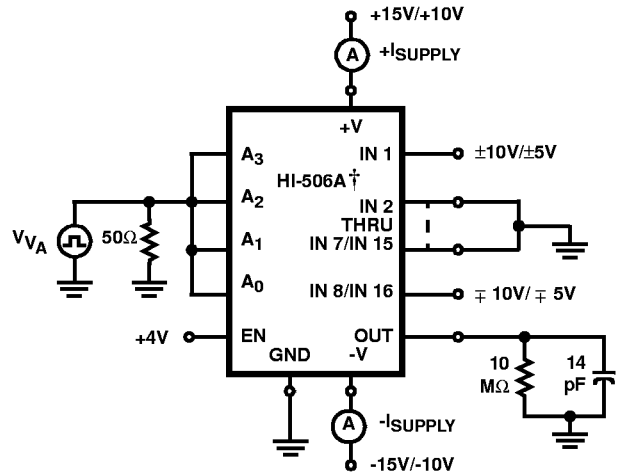


FIGURE 5B. TEST CIRCUIT

† Similar connection for HI-507A/HI-508A/HI-509A

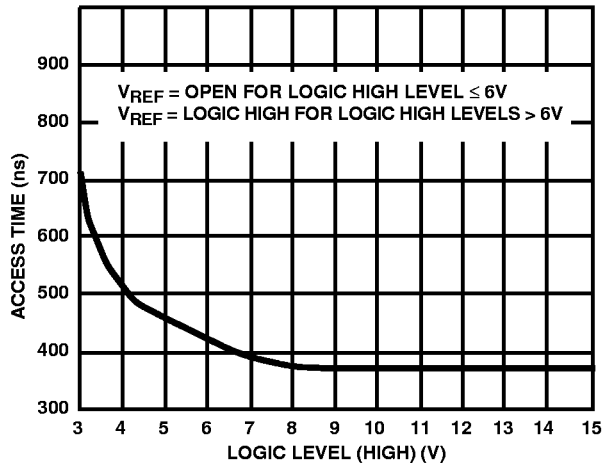


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)

FIGURE 6. ACCESS TIME

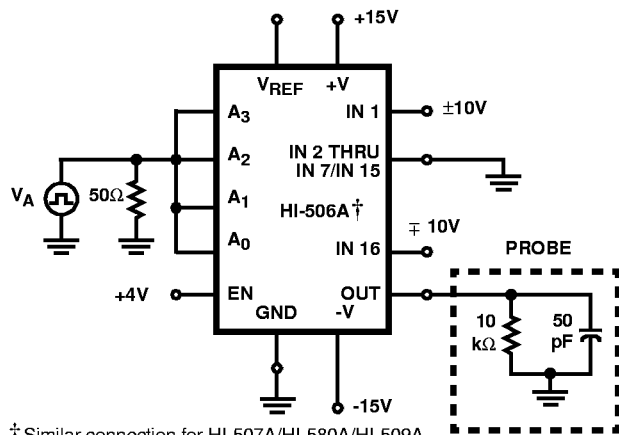


FIGURE 6B. TEST CIRCUIT

† Similar connection for HI-507A/HI-508A/HI-509A

Switching Waveforms

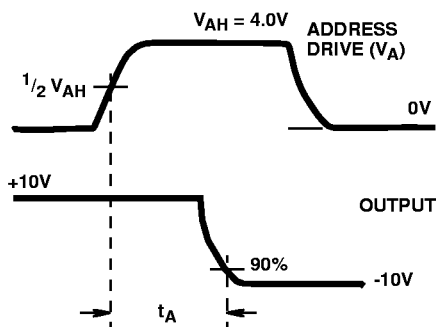


FIGURE 7A.

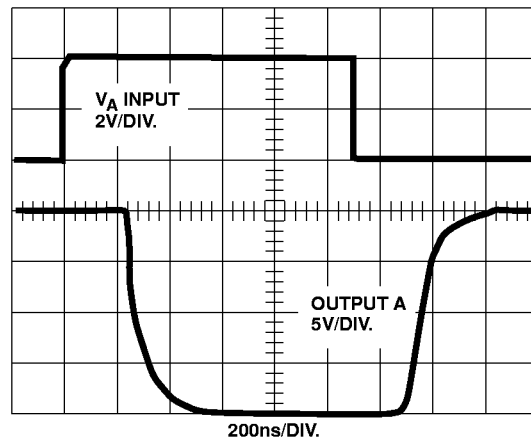
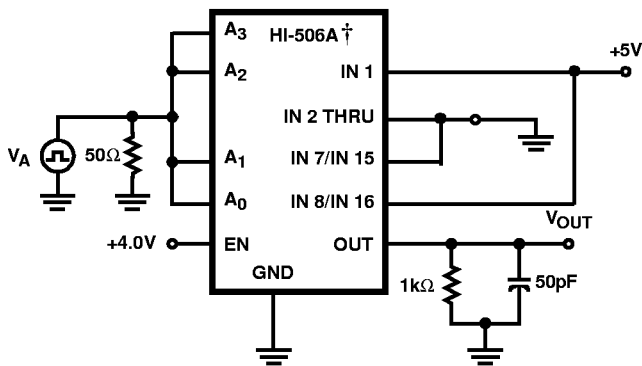


FIGURE 7B.

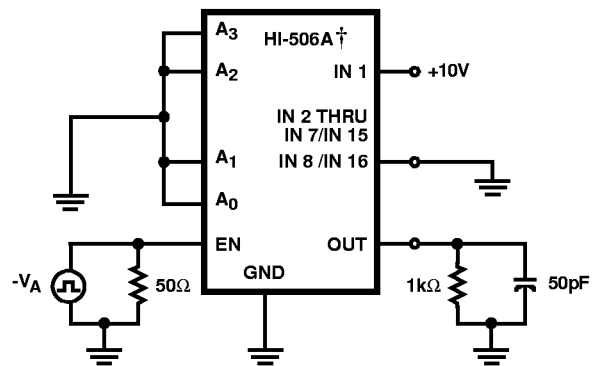
FIGURE 7. ACCESS TIME

HI-506A, HI-507A, HI-508A, HI-509A



† Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 8A.



† Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 9A.

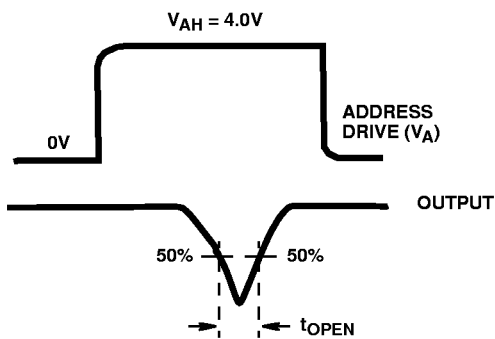


FIGURE 8B.

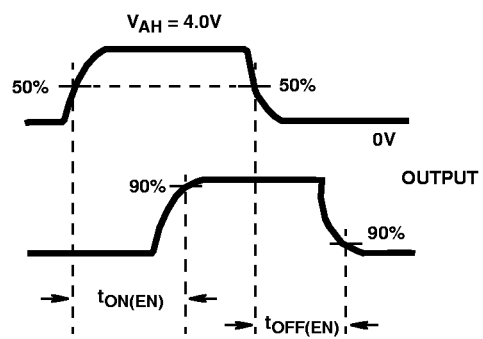


FIGURE 9B.

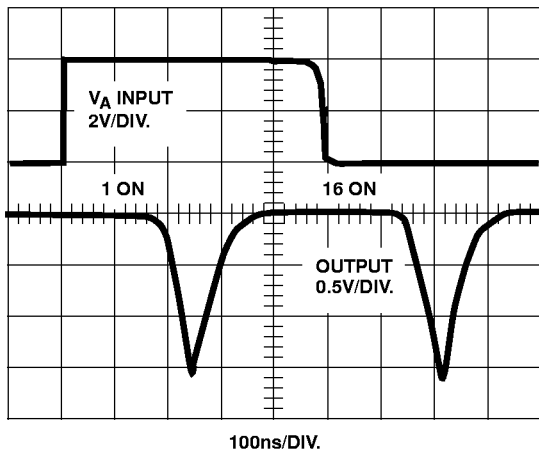


FIGURE 8C.

FIGURE 8. BREAK-BEFORE-MAKE DELAY

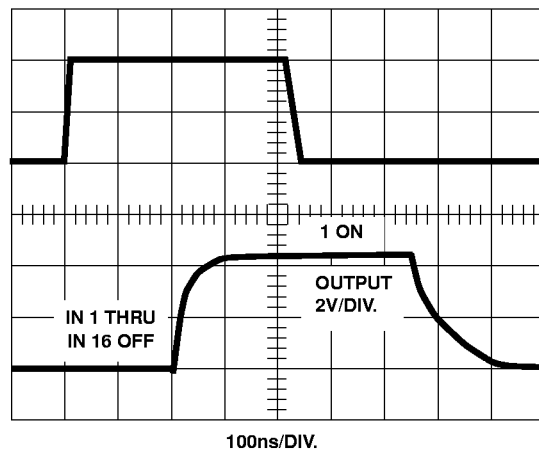


FIGURE 9C.

FIGURE 9. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

HI-506A, HI-507A, HI-508A, HI-509A

Truth Tables

HI-506A

A ₃	A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-508A

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A ₁	A ₀	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

HI-507A

A ₂	A ₁	A ₀	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-506A, HI-507A, HI-508A, HI-509A

Die Characteristics

DIE DIMENSIONS:

159 mils x 83.9 mils x 19 mils

METALLIZATION:

Type: CuAl

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

PASSIVATION:

Silox: $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

Nitride: $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

NOTE: The substrate appears resistive to the $-V_{\text{SUPPLY}}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{\text{SUPPLY}}$ potential.

WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

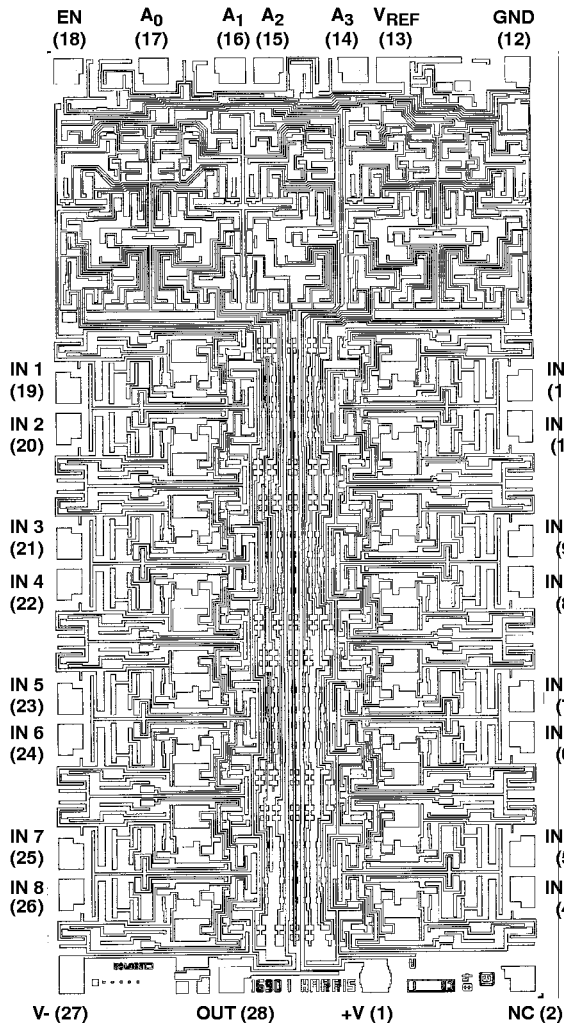
485

PROCESS:

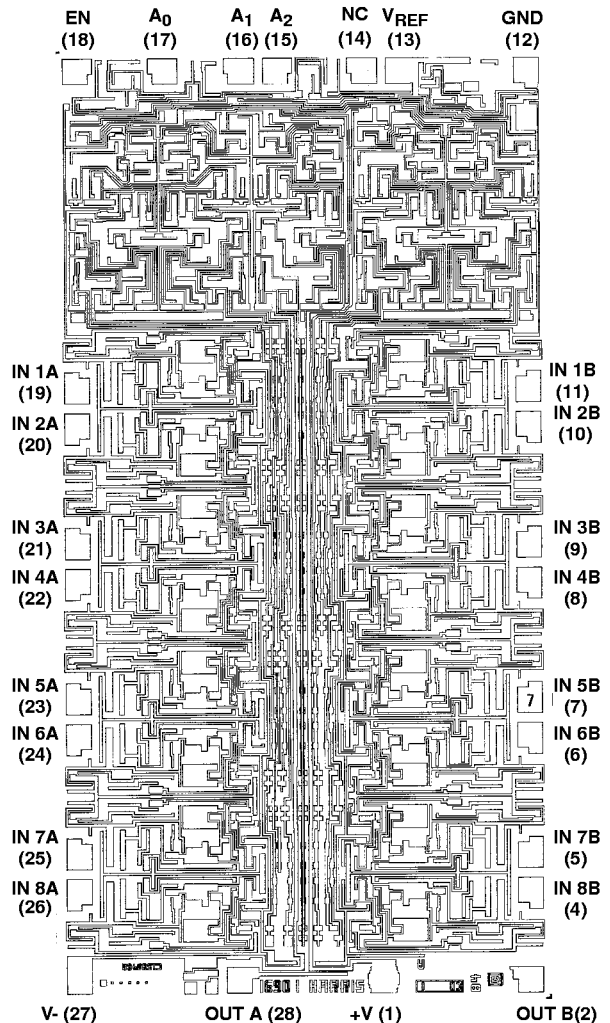
CMOS-DI

Metallization Mask Layouts

HI-506A



HI-507A



HI-506A, HI-507A, HI-508A, HI-509A

Die Characteristics

DIE DIMENSIONS:

108 mils x 83 mils

METALLIZATION:

Type: CuAl

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

PASSIVATION:

Silox: $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

Nitride: $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

NOTE: The substrate appears resistive to the $-V_{\text{SUPPLY}}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{\text{SUPPLY}}$ potential.

WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

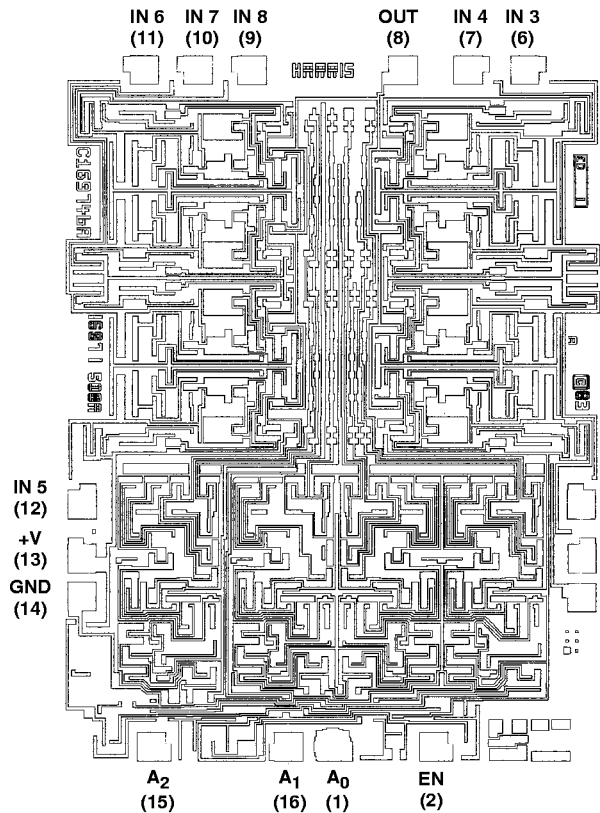
253

PROCESS:

CMOS-DI

Metallization Mask Layouts

HI-508A



HI-509A

