Data Sheet June 1999 File Number 3949.7

10-Bit, 125 MSPS, High Speed D/A Converter

The HI5721 is a 10-bit, 125 MSPS, high speed D/A converter. The converter incorporates a 10-bit, input data register with quadrature data logic capability and current outputs. The HI5721 features low glitch energy and excellent frequency domain specifications.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5721BIP	-40 to 85	28 Ld PDIP	E28.6
HI5721BIB	-40 to 85	28 Ld SOIC (W)	M28.3
HI5721-EVP	25	Evaluation Board (PDIP)	
HI5721-EVS	25	Evaluation Board (SOIC)	

Features

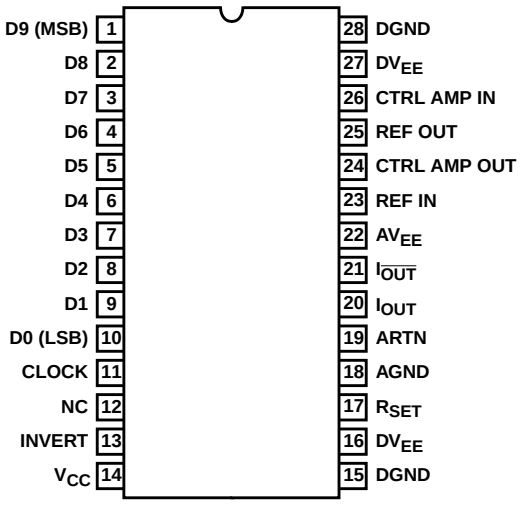
- Throughput Rate . . . . . 125 MSPS
- Low Power 700mW
- Integral Linearity Error . . . . . 1.5 LSB
- Low Glitch Energy . . . . . 1.5pV•s
- TTL/CMOS Compatible Inputs
- Improved Hold Time 0.5ns
- Excellent Spurious Free Dynamic Range
- Improved Second Source for the AD9721

Applications

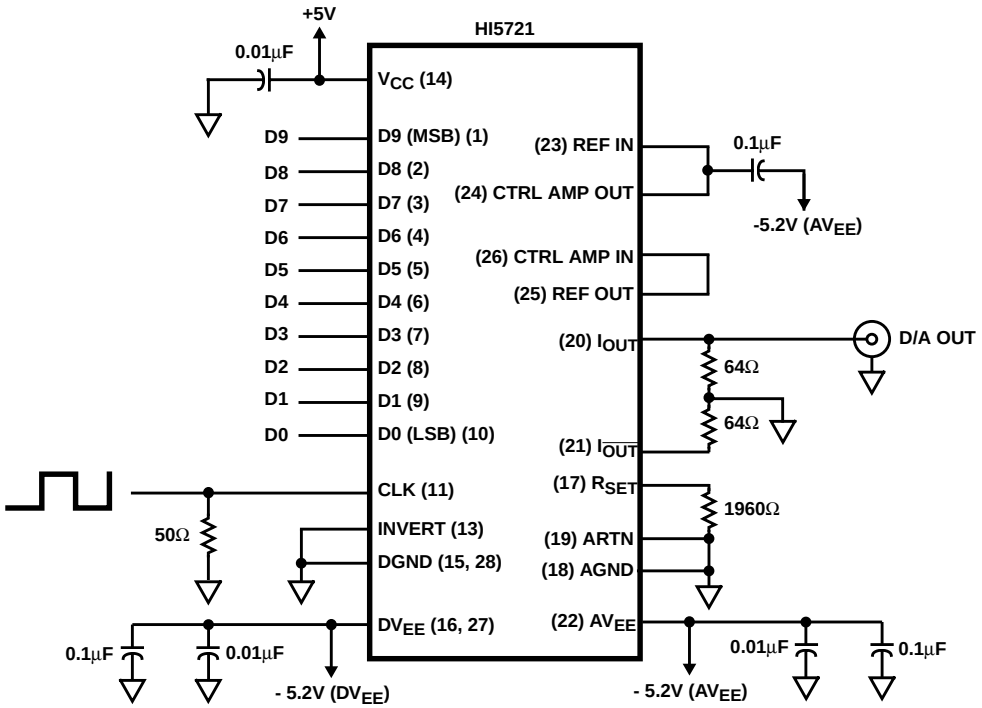
- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- HDTV
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Pinout

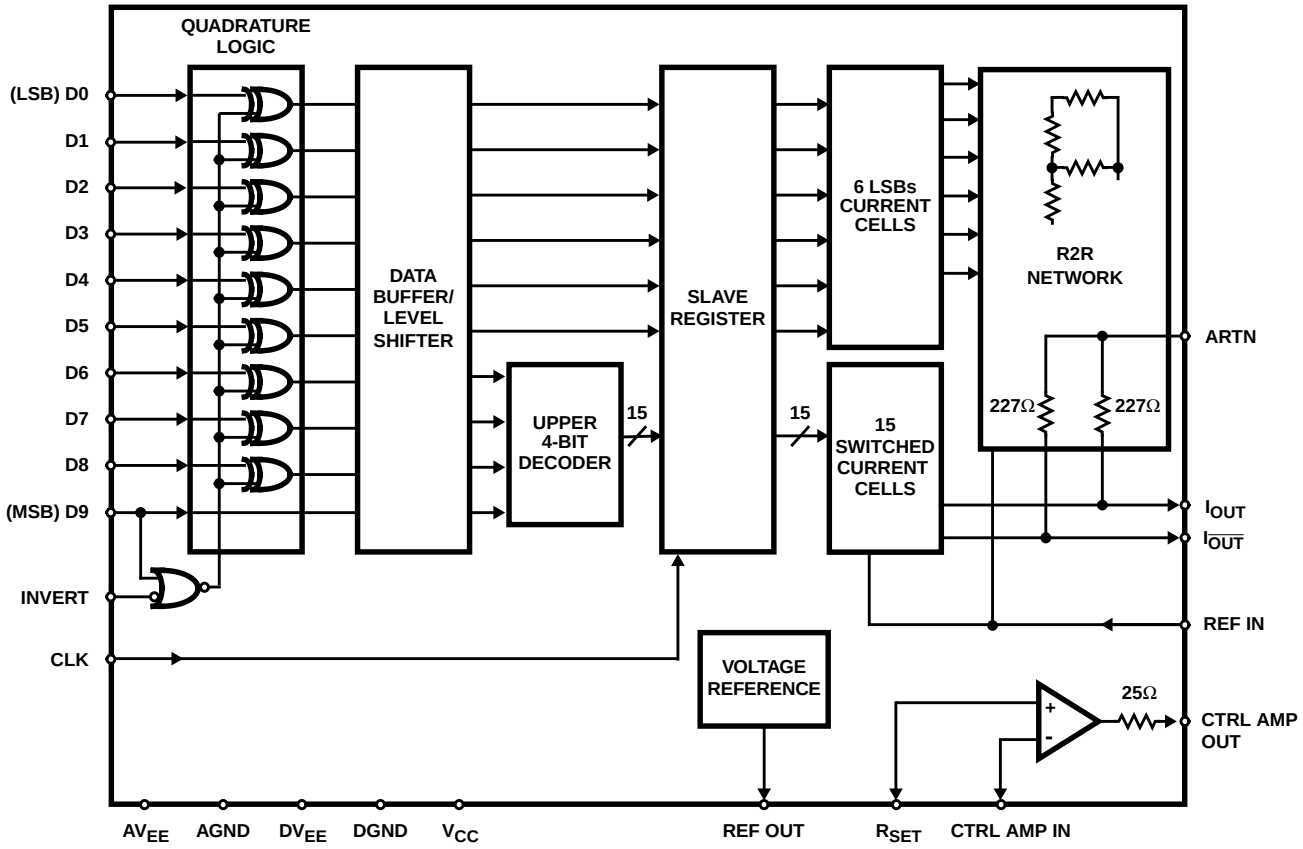
HI5721
(PDIP, SOIC)
TOP VIEW



Typical Applications Circuit



Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND . . . . . +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND . . . . . -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN . . . . . -5.5V
Digital Input Voltages (D9-D0, CLK, INVERT) . . . . . V_{CC} to -0.5 V
Internal Reference Output Current. 500µA
Control Amplifier Input Voltage Range. . . . . .AGND to -4.0V
Control Amplifier Output Current . . . . . ±2.5mA
Reference Input Voltage Range. . . . . -3.7 V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}(°C/W)
PDIP Package	55
SOIC Package	70

Maximum Power Dissipation
HI5721BIx 750mW
Maximum Junction Temperature
HI5721BIx . . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Note 4) ("Best Fit" Straight Line)	-	±0.5	±1.5	LSB
Differential Linearity Error, DNL	(Note 4)	-	±0.5	±1.0	LSB
Offset Error, I_{OS}	(Note 4)	-	16	75	µA
Full Scale Gain Error, FSE	(Notes 2, 4)	-	2	10	%
Offset Drift Coefficient	(Note 3)	-	0.1	-	µA/°C
Full Scale Output Current, I_{FS}		-	-20.48	-	mA
Output Voltage Compliance Range	(Note 3)	-1.5	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	125.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	4.5	-	ns
Output Voltage Small Step Settling Time, $t_{SETT\ SM}$	100mV Step to ±0.5 LSB Error Band, R_L = 50Ω (Note 3)	-	3.5	-	ns
Singlet Glitch Area, GE (Peak Glitch)	R_L = 50Ω (Note 3)	-	3.5	-	pV•s
Doublet Glitch Area, (Net Glitch)		-	1.5	-	pV•s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/µs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 62.5MHz Span (Notes 3, 5)	-	-59	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 62.5MHz Span (Notes 3, 5)	-	-53	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 50MHz Span (Notes 3, 5)	-	-59	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 50MHz Span (Notes 3, 5)	-	-51	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 5)	-	-75	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 5)	-	-70	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 5)	-	-75	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 5)	-	-72	-	dBc
Signal to Noise Ratio (SNR) to Nyquist (Ignoring the First 5 Harmonics)	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	54	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	51.5	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	54.5	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	50.3	-	dB
Signal to Noise Ratio + Distortion (SINAD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	52.4	-	dB
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	49.2	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	52.7	-	dB
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	47.6	-	dB
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	-57.8	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	-53.3	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.02MHz, (Notes 3, 5)	-	-57.9	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 25MHz (Notes 3, 5)	-	-51	-	dBc
Intermodulation Distortion (IMD) to Nyquist	f_{CLK} = 125 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 5)	-	57.3	-	dB
	f_{CLK} = 100 MSPS, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 5)	-	57.2	-	dB

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, CTRL AMP IN = REF OUT, T_A = 25°C for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HI5721BI T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, REF OUT	(Note 4)	-1.15	-1.25	-1.35	V
Internal Reference Voltage Drift	(Note 3)	-	100	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-50	-	+500	µA
Amplifier Input Impedance	(Note 3)	-	10	-	MΩ
Amplifier Large Signal Bandwidth	4.0V_{P-P} Sine Wave Input, to Slew Rate Limited (Note 3)	-	1	-	MHz
Amplifier Small Signal Bandwidth	1.0V_{P-P} Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	4.6	-	kΩ
Reference Input Multiplying Bandwidth	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	75	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 4)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 4)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 4)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 4)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 3 (Note 3)	2.0	-	-	ns
Data Hold Time, t_{HLD}	See Figure 3 (Note 3)	0.5	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 3 (Note 3)	-	4.5	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 3 (Note 3)	1.0	0.85	-	ns
POWER SUPPLY CHARACTERISITICS					
IDV_{EE}	(Note 4)	-	100	110	mA
IAV_{EE}	(Note 4)	-	-	15	mA
V_{CC}	(Note 4)	-	14	25	mA
Power Dissipation	(Note 4)	-	700	775	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5%	-	50	-	µA/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 640µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. All devices are 100% tested at 25°C. 100% productions tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
5. Spectral measurements made without external filtering.

Timing Diagrams

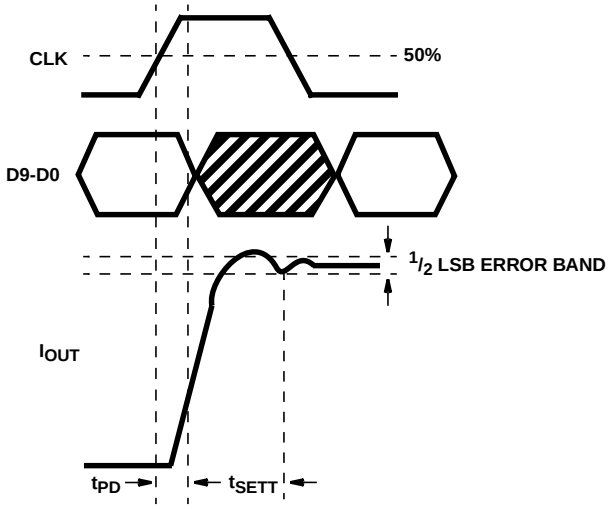


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

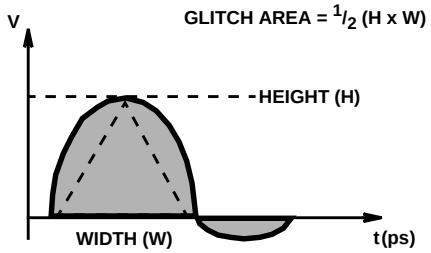


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

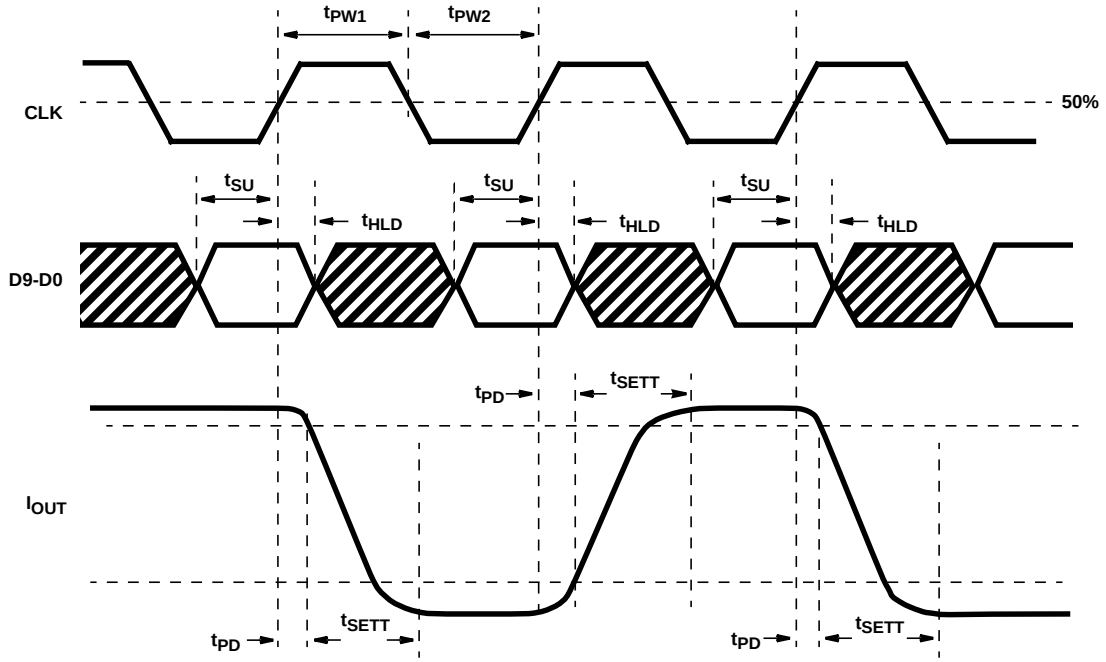


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

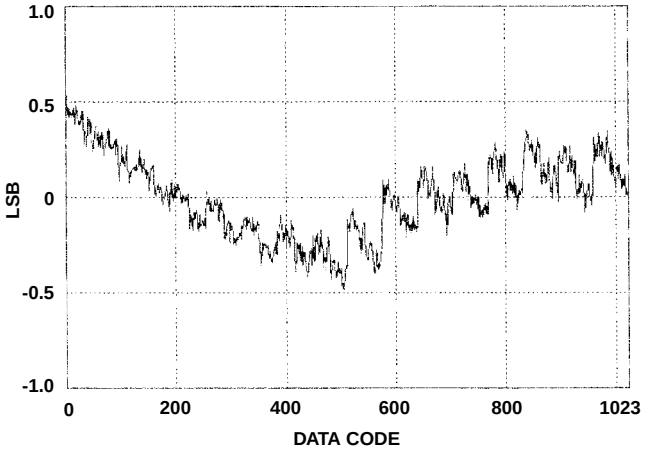


FIGURE 4. INTEGRAL NON-LINERARITY "BEST FIT" STRAIGHT LINE

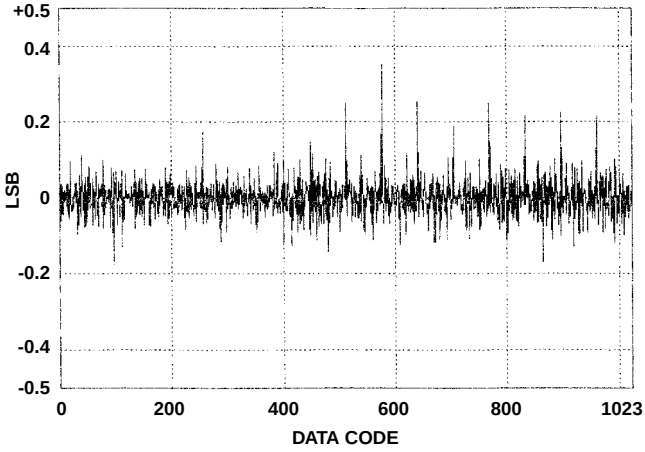


FIGURE 5. DIFFERENTIAL NON-LINEARITY

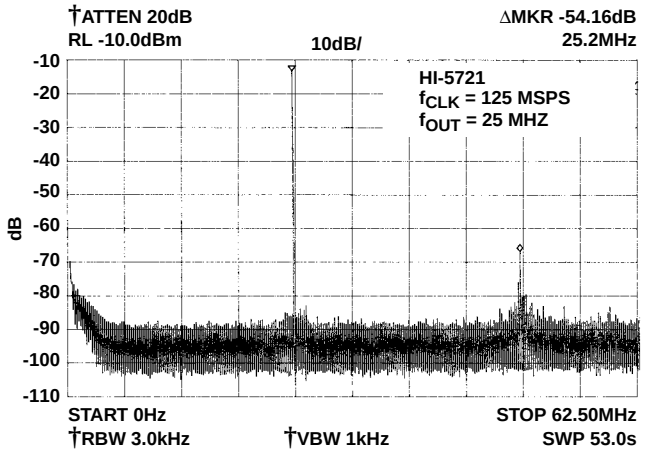


FIGURE 6. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 25MHz FUNDAMENTAL

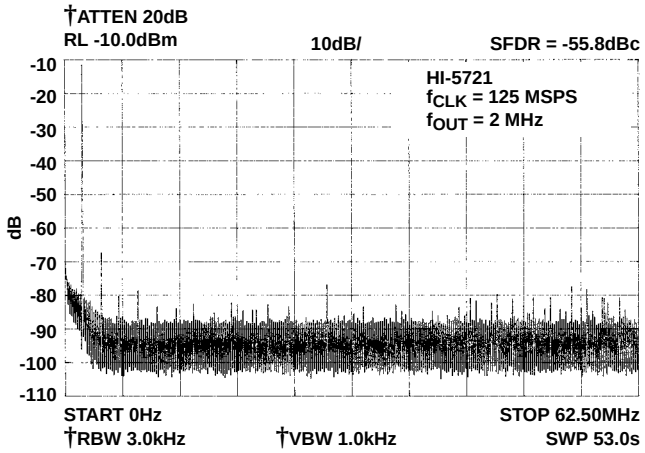


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 2MHz FUNDAMENTAL

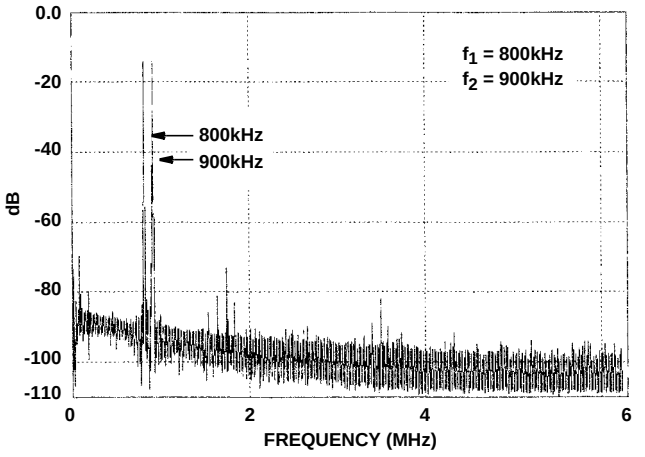


FIGURE 8. INTERMODULATION DISTORTION

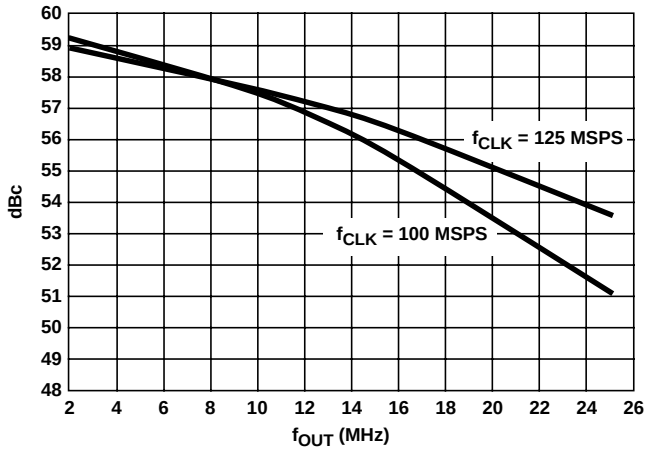


FIGURE 9. SPURIOUS FREE DYNAMIC RANGE (TO NYQUIST) vs OUTPUT FREQUENCY

Typical Performance Curves (Continued)

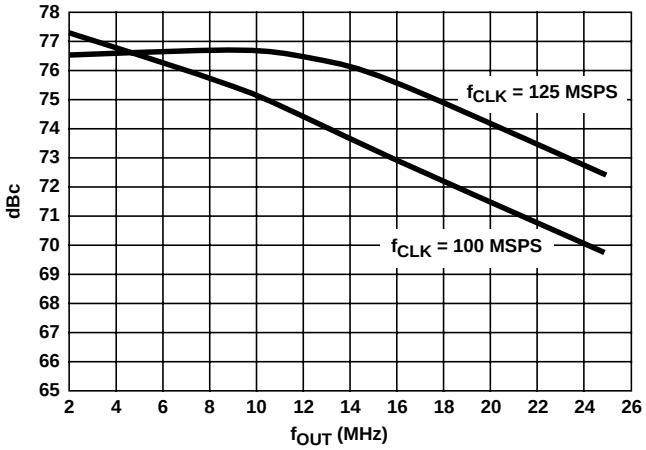


FIGURE 10. SPURIOUS FREE DYNAMIC RANGE (±1MHz WINDOW) vs FREQUENCY

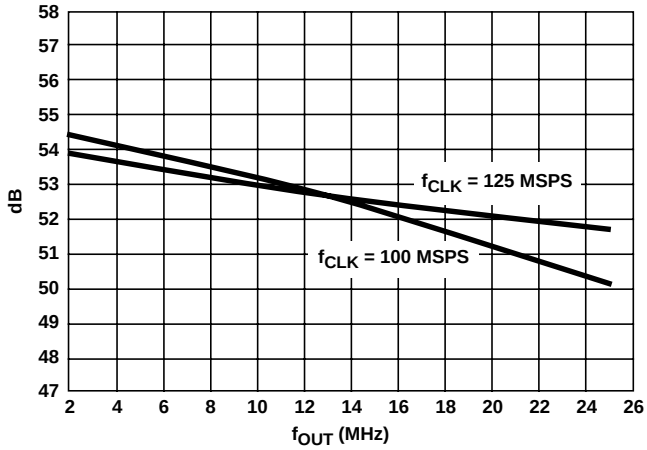


FIGURE 11. SIGNAL TO NOISE RATIO vs OUTPUT FREQUENCY

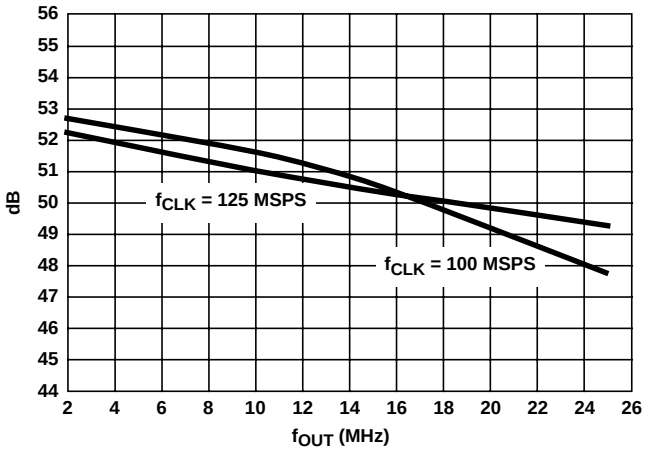


FIGURE 12. SIGNAL TO NOISE + DISTORTION vs OUTPUT FREQUENCY

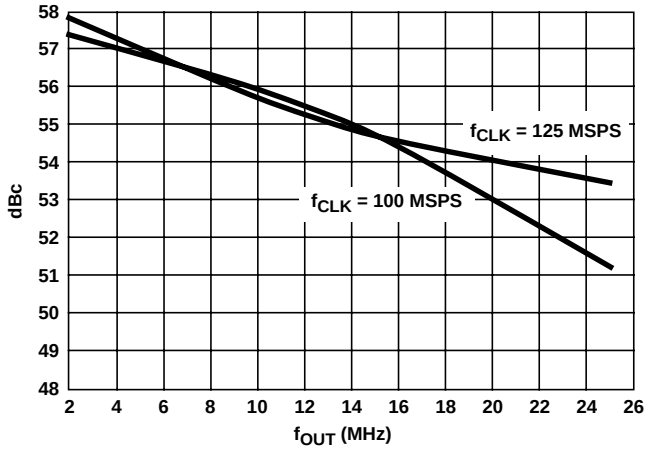


FIGURE 13. TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

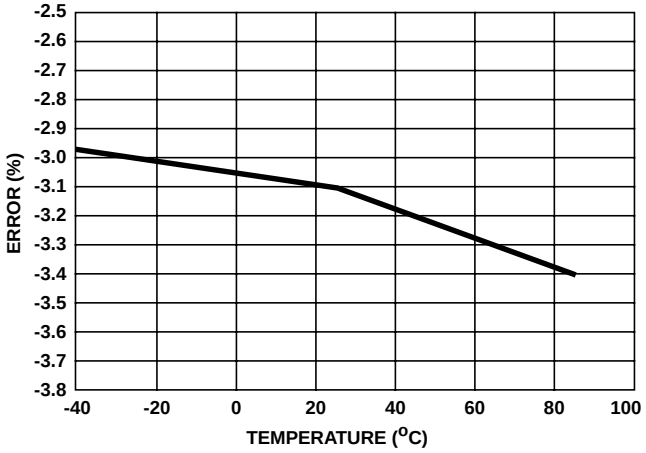


FIGURE 14. GAIN ERROR vs TEMPERATURE

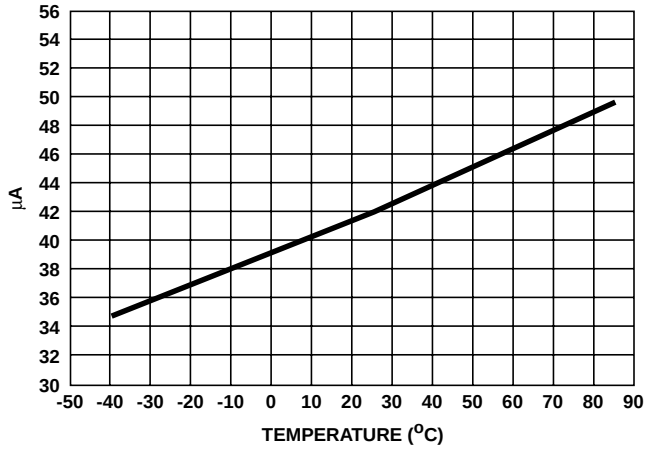


FIGURE 15. OFFSET ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

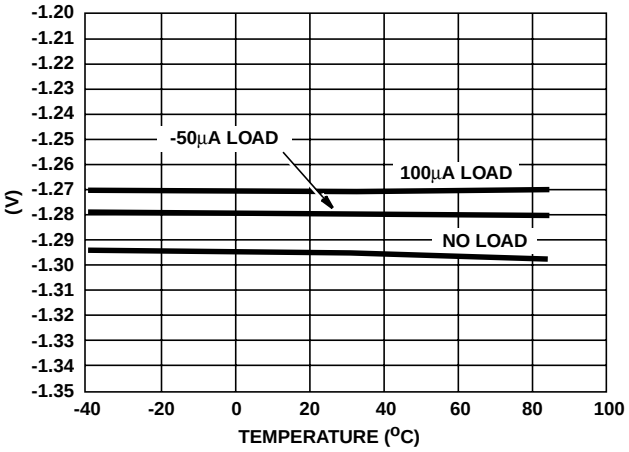
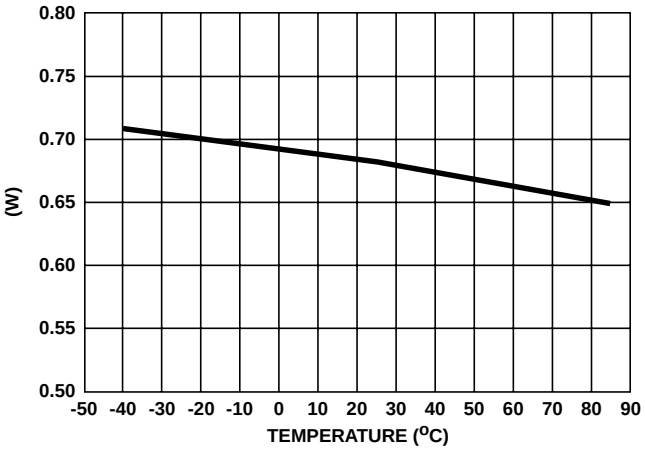


FIGURE 16. REFERENCE VOLTAGE vs TEMPERATURE



NOTE: Clock Frequency does not alter power dissipation.

FIGURE 17. POWER DISSIPATION vs TEMPERATURE

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB) through D9 (MSB)	Digital Data Bit 0, the Least Significant Bit through Digital Data Bit 9, the Most Significant Bit.
11	CLK	Data Clock pin 100kHz to 125 MSPS.
12	NC	No Connect.
13	INVERT	Data Invert control for bits D0 (LSB) through D8. D9 (MSB) is not affected.
14	V_{CC}	Digital Logic Supply +5V.
15, 28	DGND	Digital Ground.
16, 27	DV_{EE}	-5.2V Logic Supply.
17	R_{SET}	External resistor to set the full scale output current. I_{FS} = 32 x (CTRL AMP IN/R_{SET}). Typically 1960Ω.
18	AGND	Analog Ground supply current return pin.
19	ARTN	Analog Signal Return for the R/2R ladder.
20	I_{OUT}	Current Output pin.
21	I_{OUT}	Complementary Current Output pin.
22	AV_{EE}	-5.2V Analog Supply.
23	REF IN	Reference Input pin. Typically connected to CTRL AMP OUT and a 0.1µF capacitor should be connected to AV_{EE} to bypass the reference voltage. Provides a reference for the current switching network.
24	CTRL AMP OUT	Control Amplifier Output. Used to convert the internal reference or an external signal to the precision reference current.
25	REF OUT	Internal Reference Output. Output of the internal -1.25V (typical) bandgap voltage reference.
26	CTRL AMP IN	Control Amplifier Input. High impedance, inverting input of the reference control/buffer amplifier.

Detailed Description

The HI5721 is a 10-bit, current out D/A converter. The DAC can convert at 125 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch and maintain 10-bit linearity without laser trimming. The HI5721 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5721 consumes 700mW (typical) and has an improved hold time of only 0.5ns (typical). The HI5721 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5721 is a TTL/CMOS compatible D/A. The inputs can be inverted using the INVERT pin. When INVERT is LOW ('0') the input quadrature logic simply passes the data through unchanged.

When INVERT is HIGH ('1') bits D0 (LSB) through D8 are inverted. D9 is not inverted and can be considered a sign bit when enabling this quadrature compatible mode. The INVERT function can simplify the requirements for large sine wave lookup tables in a Numerically Controlled Oscillator. The NCO used in a DDS application would only have to store or generate 90 degrees of information and then use the INVERT control to control the sign of the output waveform.

Data Buffer/Level Shifters

Data inputs D0 (LSB) through D9 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R and Segmented Current source arrangement. Bits D0 (LSB) through D5 directly drive a typical R/2R network to create the binary weighted current sources. Bits D6 through D9 (MSB) pass through a "thermometer" encoder that converters the incoming data into 15 individual segmented current source enables. The split architecture helps to improve glitch while maintaining 10-bit linearity without laser trimming. The worst case glitch is more constant across the entire output transfer function.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5721 clock rate can run to 125 MSPS, to minimize reflections and clock noise into the part proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 125 MSPS clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$,

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5721 CLK pin as possible.

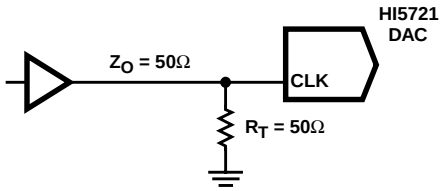


FIGURE 18. AC TERMINATION OF THE HI5721 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5721 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should be decoupled with a 0.1µF capacitor.

Reference

The internal reference in the HI5721 is a -1.25V (typical) bandgap voltage reference with a 100µV/^{O}C temperature drift (typical). The internal reference should be buffered by the Control Amplifier to provide adequate drive for the segmented current cells and the R/2R resistor ladder. Reference Out (REF OUT) should be connected to the Control Amplifier Input (CTRL AMP IN). The Control Amplifier Output (CTRL AMP OUT) should be used to drive the Reference Input (REF IN) and a 0.1µF capacitor to analog V- (AV_{EE}). This improves settling time by decoupling switching noise from the analog output of the HI5721.

The Full Scale Output Current is controlled by the CTRL AMP IN pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = ($V_{CTRL\ AMP\ IN}/R_{SET}$) x 32.

Multiplying Capability

The HI5721 can operate in two different multiplying configurations. First, using the CTRL AMP IN input pin, a -0.6V to -1.2V signal can be applied with a bandwidth up to 1MHz. To increase the multiplying bandwidth, the 0.1µF capacitor connected from REF IN to AV_{EE} can be reduced.

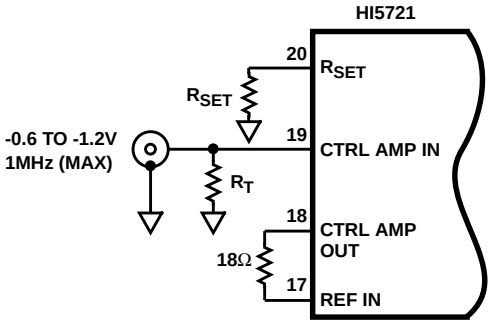


FIGURE 19. LOW FREQUENCY MULTIPLYING CIRCUIT

If higher multiplying frequencies are desired, the reference input can be directly driven. The analog signal range is -3.3V to -4.25V. The multiplying signal must be capacitively coupled into REF IN onto a DC bias between -3.3V to -4.25V (-3.8V typically).

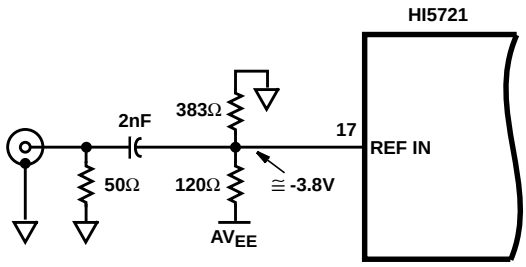


FIGURE 20. WIDEBAND MULTIPLYING CIRCUIT

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a load resistor. Both current outputs should have the same load resistor (64Ω typically). By using a 64Ω load on the output, a 50Ω effective output resistance (R_{OUT}) is achieved due to the 227Ω (±15%) parallel resistance seen looking back into the output. This is the nominal value of the R2R ladder of the DAC. The 50Ω output is needed for matching the output with a 50Ω line. The load resistor should be chosen so that the effective output resistance (R_{OUT}) matches the line resistance. The output voltage is:

$V_{OUT} = I_{OUT} \times R_{OUT}$.

I_{OUT} is defined in the reference section. The compliance range of the output is from -1.5V to 3V, with a $1V_{P-P}$ voltage swing allowed within this range. However, if it is desired that the output be offset above zero volts, it is necessary that pin 19 (ARTN) be connected to the same voltage as the load resistor, not to exceed 3V.

Glitch

TABLE 1. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D9-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
11 1111 1111	-20.48	0
10 0000 0000	-10.24	-10.24
00 0000 0000	0	-20.48

The output glitch of the HI5721 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Intersil HI5721 employes an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e., 01 1111 1111 to 10 0000 0000. But in the HI5721 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R/2R segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5721 the output is terminated into a 64Ω load. The glitch is measured at the major carrys throughout the DAC's output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 21 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt • seconds (pV • s).

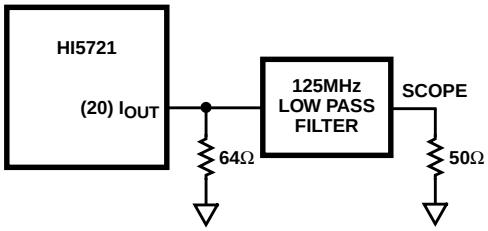


FIGURE 21. GLITCH TEST CIRCUIT

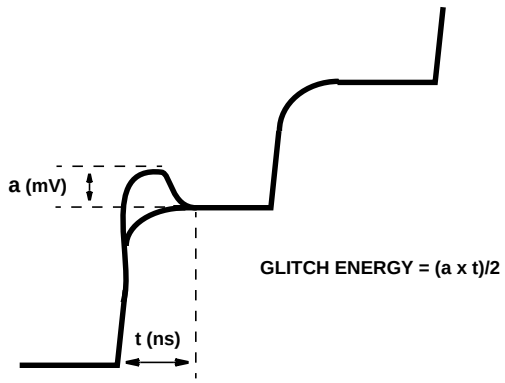


FIGURE 22. GLITCH ENERGY

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter to a voltage, an amplifier should be used as shown in Figure 23 below. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

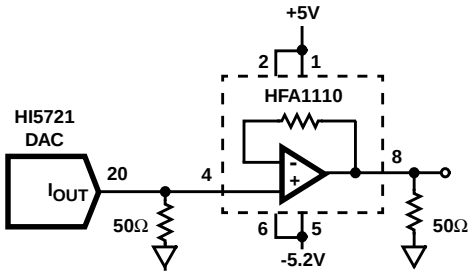


FIGURE 23. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Bipolar Applications

To convert the output to a bipolar ±2.0V output swing the following applications circuit is recommended. The Reference can only provide 100µA of drive, so it must be buffered to create the bipolar offset current needed to generate -2.0V output with all bits ‘off’. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the output voltage swing and error.

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit output, Numerically-Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 25 shows how to interface an HI5721 to the HSP45106.

Interfacing to the HSP45102 NCO-12

The HSP45102 is a 12-bit output Numerically Controlled Oscillator (NCO). The HSP45102 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 26 shows how to interface an HI5721 to the HSP45102.

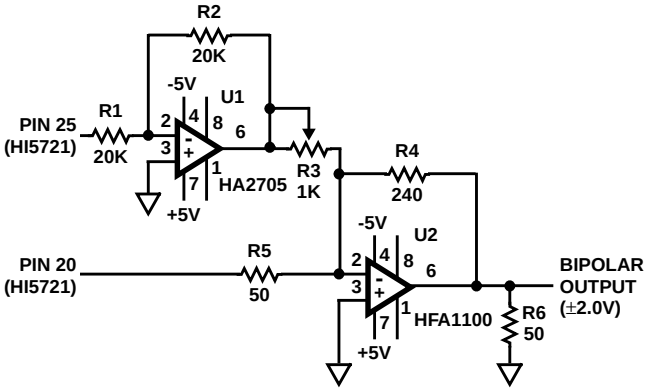


FIGURE 24. BIPOLAR OUTPUT CONFIGURATION

This high level block diagram is that of a basic PSK modulator. In this example the encoder generates the PSK waveform by driving the Phase Modulation Inputs (P1, P0) of the HSP45102. The P1-0 inputs impart a phase shift to the carrier wave as defined in Table 2.

TABLE 2. PHASE MODULATION INPUT CODING

P1	P0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

The 10 MSBs of the HSP45102 drive the 10-bit HI5721 DAC which converts the NCO output into an analog waveform. The output filter connected to the DAC can be tailored to remove unwanted spurs for the desired carrier frequency. The controller is used to load the desired center frequency and control the HSP45102. The HI5721 coupled with the HSP45102 make an inexpensive PSK modulator with Spurious Free operation down to -76dBc.

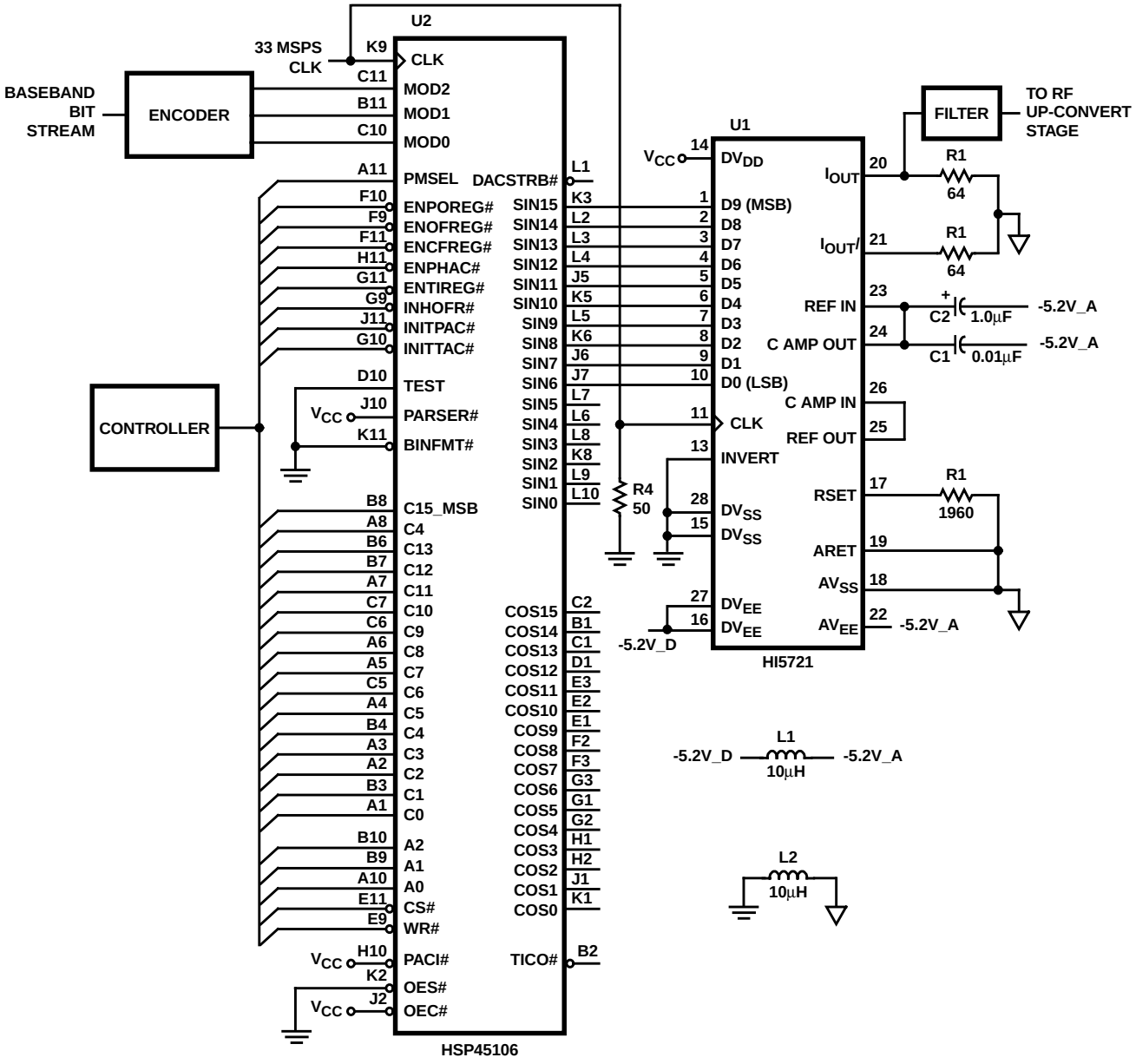


FIGURE 25. PSK MODULATOR USING THE HI5721 AND THE HSP45106 12-BIT NCO

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Feedthru is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an $^1/_2$ LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

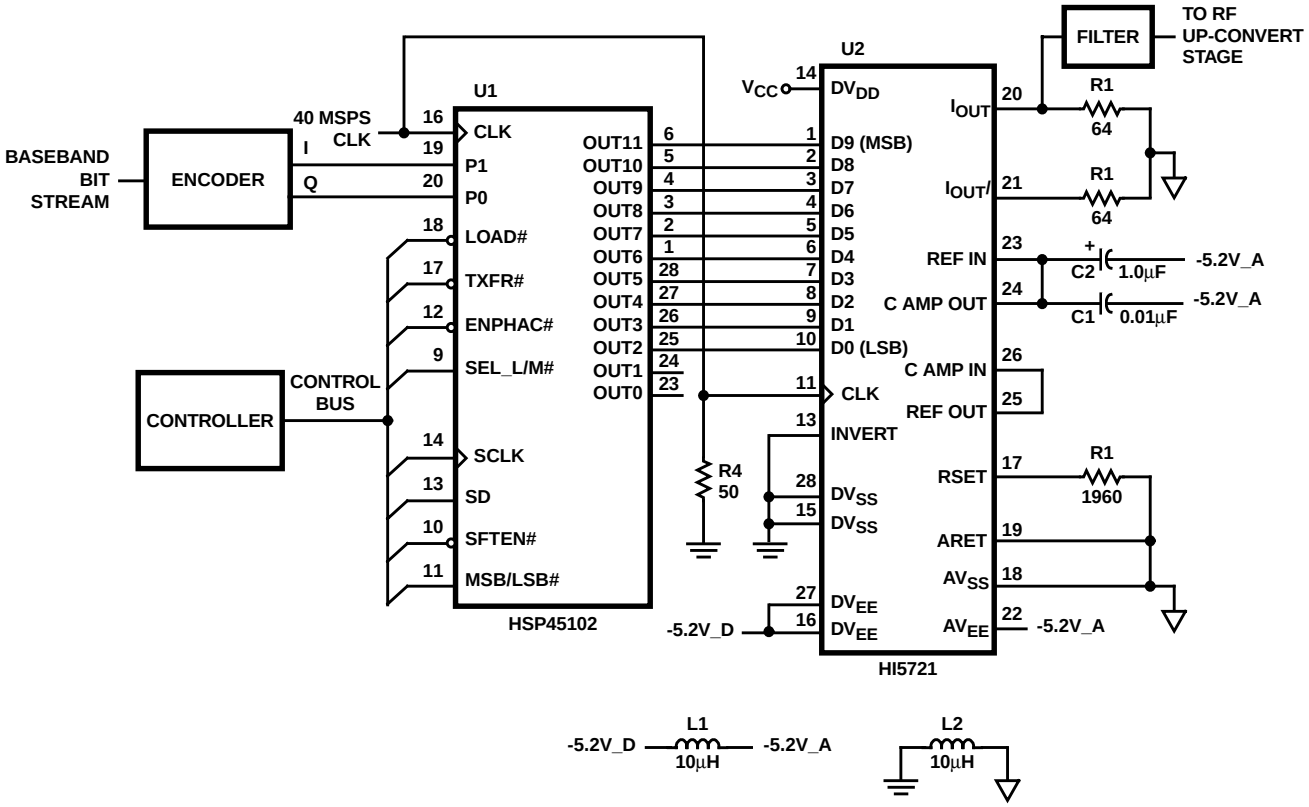


FIGURE 26. PSK MODULATOR USING THE HI5721 AND THE HSP45102 12-BIT NCO

Differential Phase, $\Delta\Phi$, is the phase error from and ideal sine wave.

Signal to Noise Ratio, SNR, is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of $^1/_2$ the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is

$$IMD = \frac{20\log\ (\text{RMS of sum and difference distortion products})}{(\text{RMS amplitude of the fundamental})}$$