HIP0045

1A/50V Octal Low Side Power Driver With Serial Bus Control and Fault Protection

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The HIP0045 is a logic controlled, eight channel Octal Serial Power Low Side Driver. The serial peripheral interface (SPI) utilized by the HIP0045 is a serial synchronous bus compatible with Intersil CDP68HC05, or equivalent, microcomputers. As shown in the Block Diagram for the HIP0045, each of the open drain MOS Output Drivers have individual protection for over-voltage and over-current. Each output channel has separate output latch control with fault unlatch and diagnostic or status feedback. Under normal ON conditions, each output driver is in a low voltage, high current state of saturated turn-on. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a fault is sensed, the respective output driver for Channels 0 - 5 have overcurrent latch-off. Channels 6 and 7 are configured for lamp drivers and have current limiting with over-temperature latch-off. Channels 0 and 1 have direct parallel drive control for PWM applications and are ORed with the SPI Bus control. All channels are SPI Bus controlled and sense the output states for diagnostic feedback.

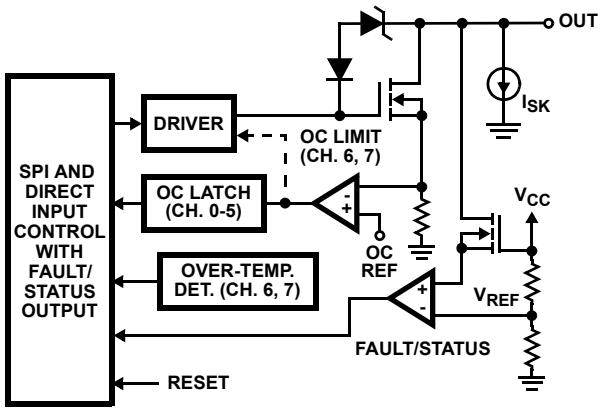
The HIP0045 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving relays, solenoids and lamps in applications where low standby power, high operating voltage, and high output current in high ambient temperature conditions is required.

The HIP0045 is in a 20 lead plastic Power SOP (PSOP) Package with an integral copper ‘slug’ to conduct heat directly to a PCB interface or heat sink on the bottom of the package.

Ordering Information

PART NO.	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HIP0045AB	-40 to 125	20 Ld PSOP	M20.433

Driver Block Diagram



Features

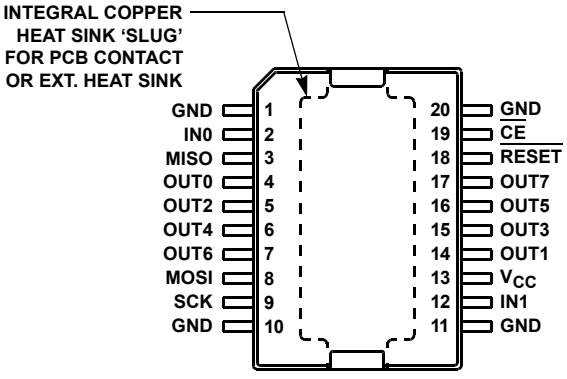
- Octal NDMOS Output Drivers in a High Voltage Power BiMOS Process
- Over-Stress Protection - Each Output:
  - Over-Current Protection . . . . . 1A Min
  - Over-Voltage Clamp Protection . . . . . 50V Typ
  - Thermal Shutdown Protection (2 Channels)
- Open-Load Detection
- Power BiMOS Output Configuration
  - Current Latch-Off Protection for 6 Channels; 2 with External Drive Input and ORed with SPI Bus Control
  - 2 Channels Configured for Lamp Drivers with Current Limiting and Over-Temperature Latch-Off
- High Speed CMOS Logic Control
  - SPI Bus Controlled Interface
  - Individual Output Latch
  - Individual Fault Unlatch and Feedback
  - Common Reset Line
- Low Quiescent Current . . . . . 5mA Max
- Ambient Operating Temp. Range. . . . . -40^{O}C to 125^{O}C

Applications

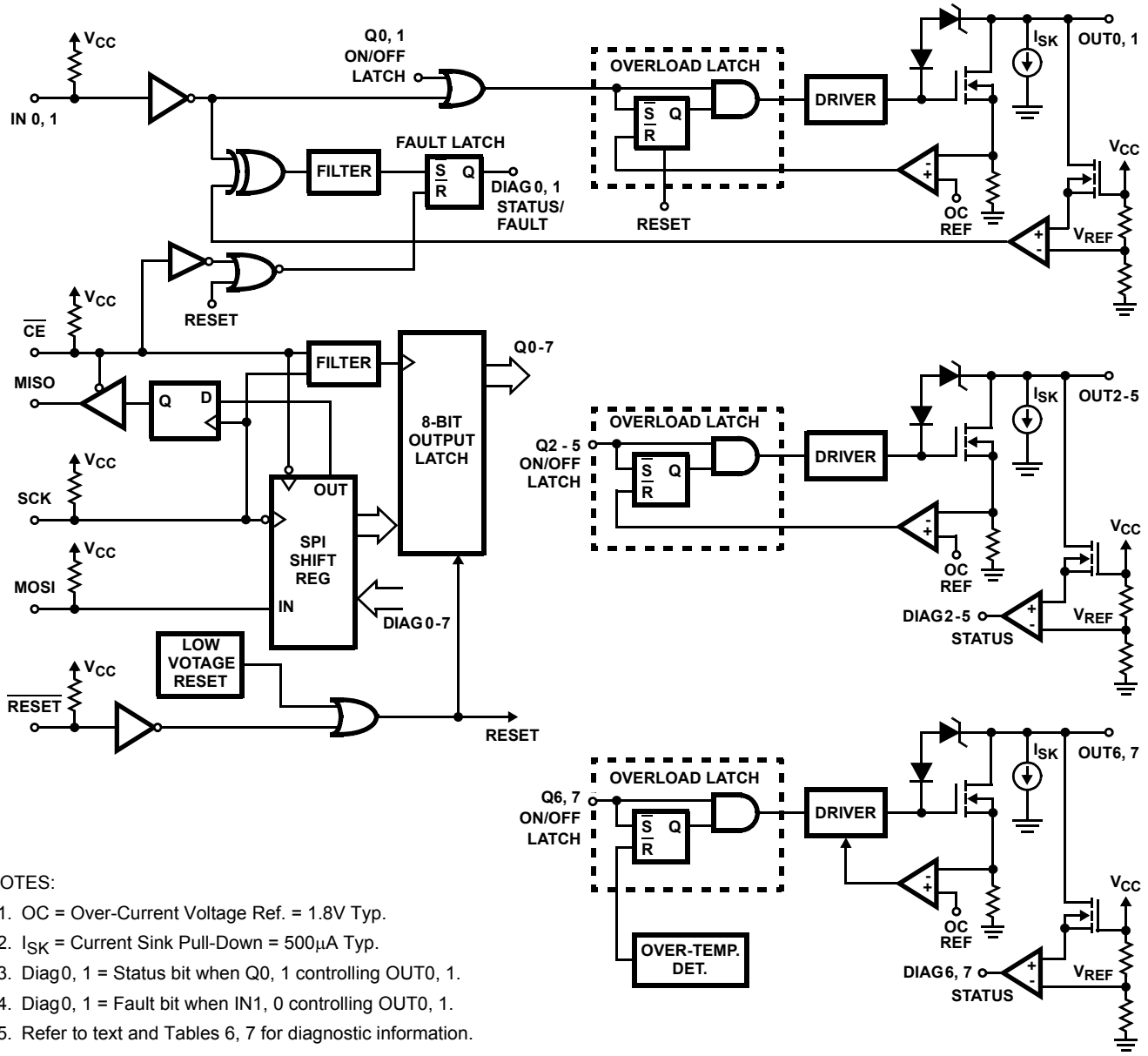
- Automotive and Industrial Systems
- Solenoids, Relays and Lamp Drivers
- Logic and µP Controlled Drivers
- Robotic Controls

Pinout

HIP0045 (PSOP WITH HEAT SLUG)
TOP VIEW



Detailed Block Diagram



NOTES:

1. OC = Over-Current Voltage Ref. = 1.8V Typ.
2. I_{SK} = Current Sink Pull-Down = 500µA Typ.
3. Diag 0, 1 = Status bit when Q0, 1 controlling OUT0, 1.
4. Diag 0, 1 = Fault bit when IN1, 0 controlling OUT0, 1.
5. Refer to text and Tables 6, 7 for diagnostic information.

Input to Output Control Tables

TABLE 1. OUTPUT 0

SPI BIT 0	IN0	OUT0
0	1	OFF
0	0	ON
1	0	ON
1	1	ON

TABLE 2. OUTPUT 1

SPI BIT 1	IN1	OUT1
0	1	OFF
0	0	ON
1	0	ON
1	1	ON

TABLE 3. OUTPUT 2 - 7

SPI BIT 2 - 7	OUT2 - 7
0	OFF
1	ON

TABLE 4. OUTPUT CONTROL REGISTER, Q0 - 7

Q1	Q3	Q5	Q7	Q0	Q2	Q4	Q6
(D7I)	(D6I)	(D5I)	(D4I)	(D3I)	(D2I)	(D1I)	(D0I)

MSB **LSB**

NOTE: The Output Control Register bits Q0 -7 have the same order as the Diagnostic Failure Register bits Diag0 - 7 as defined in Table 5. Data bits D0I - D7I give the MOSI SPI serial data input flow sequence.

Absolute Maximum Ratings

Maximum Output Voltage, V_{OUT} . . . . . -0.7 to V_{OC}
Peak Output Load Current, I_{LOAD} . . . . . As Specified for I_{SC}, I_{LIM}
Continuous Output Load Current, I_{OUT} (All 8 Outputs ON) 0.5A
Continuous Output Load Current, I_{OUT} (Any one Output ON) . . 1A
Total Average Current, I_{OUT} (All 8 Outputs) 4.5A
Reverse Peak Current Drive, Any one Output, I_{RD}; $t \leq 2ms$ . . . -3A
DC Logic Supply, V_{CC} . . . . . -0.3 to 7V
Input Voltage, All Inputs and Data Lines . . . . . -0.3 to V_{CC} +0.3V

Operating Conditions

Temperature Range . . . . . -40°C to 125°C
Logic Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PSOP Package	40	2

Maximum Junction Temperature, T_J . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . -55°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 265°C

Die Characteristics

Back Side Potential . . . . . V- (GND Pin, Heat Sink)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} Rated with standard PC Board, θ_{JC} rated with infinite heat sink.

Electrical Specifications

V_{CC} = 4.5V to 5.5V, T_A = -40°C to 125°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current, No Load	I_{CCO}	No Load	-	-	5	mA
Supply Current, Full Load	I_{CC}	All Outputs ON, 0.5A Load Per Output	-	-	5	mA
Output Clamping Voltage (Note 7)	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	45	-	62	V
Output Clamping Energy	E_{OC}	1ms Single Pulse Width, T_A = 25°C, (Refer to Figure 4 for SOA)	20	45	-	mJ
Output Leakage Current 1 (Note 8)	$I_{O\ LEAK1}$	V_{OUT} = 25V, Outputs OFF	-	-	100	µA
Output Leakage Current 2 (Note 8)	$I_{O\ LEAK2}$	V_{OUT} = 16V, Outputs OFF	-	-	100	µA
Output Leakage Current 3 (Note 8)	$I_{O\ LEAK3}$	V_{OUT} = 16V, Outputs OFF, V_{CC} = 1V	-	-	10	µA
Drain-to-Source On Resistance, OUT0 - 7	r_{DSON}	I_{LOAD} = 0.5A; T_J = 150°C	-	-	1.5	Ω
Output Capacitance	C_{OUT}	V_{OUT} = 16V, f = 1MHz	-	-	20	pF
Turn-On Delay, OUT0, 1	$t_{d(ON)}$	R_L = 500Ω, V_{CE} = 50% to V_{OUT} = 0.9 x V_{BATT}, $V_{IN0,1}$ = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	5	µs
Turn-On Delay, OUT2 - 7	$t_{d(ON)}$	R_L = 500Ω, V_{CE} = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	10	µs
Turn-Off Delay	$t_{d(OFF)}$	R_L = 500Ω, $V_{\overline{CE}}$ = 50% to V_{OUT} = 0.1 x V_{BATT}, $V_{IN0,1}$ = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	10	µs
Turn-On Voltage Slew-Rate, OUT2 - 7	$\frac{dV_{ON1}}{dt}$	For V_{OUT} = 90% to 30% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	0.7	3.5	V/µs
Turn-On Voltage Slew-Rate, OUT0, 1	$\frac{dV_{ON2}}{dt}$	For V_{OUT} = 90% to 30% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	2	10	V/µs
Turn-Off Voltage Slew-Rate, OUT0 - 7	$\frac{dV_{OFF1}}{dt}$	For V_{OUT} = 30% to 90% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	2	10	V/µs
Turn-Off Voltage Slew-Rate, OUT0 - 7	$\frac{dV_{OFF2}}{dt}$	For V_{OUT} = 30% to 80% of V_{OC}; V_{BATT} = 0.9 x V_{OC}, R_L = 500Ω	-	2	15	V/µs
FAULT PARAMETERS						
Reverse Current Drive, OUT0 - 7	I_{RD}		-500	-	-	mA
Reverse Voltage Drop, OUT0 - 7	V_{RD}	I_{OUT} = -3A, t ≤2ms	-1.5	-	-	V
ΔI_{CC} during Reverse Current Drive	ΔI_{CC}	I_{OUT} = -3A, t ≤2ms	-	-	100	mA

Electrical Specifications

V_{CC} = 4.5V to 5.5V, T_A = -40°C to 125°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Load Threshold Voltage	V_{REF}	Open Load Fault Condition, Fault Detected If $V_{OUT} < V_{REF}$	0.32 x V_{CC}	-	0.4x V_{CC}	V
Open Load Pull-Down Current	I_{SK}	No Load, $V_{OUT} = V_{BATT}$ = 16V	20	-	100	µA
Over-Current Shutdown Threshold, OUT0 - 5	I_{SC}	V_{CC} = 5V	1.05	1.4	2	A
Short Circuit Current Limit, OUT6, 7	I_{LIM}	V_{CC} = 5V	1.05	1.4	1.75	A
Short Circuit Shutdown Delay, OUT0 - 5	t_{SC}		0.2	-	12	µs
Disable Fault Detection Time, Channel IN0, IN1 After Input Switch Transition	t_{DF}		15	-	50	µs
Over-Temperature Detection Threshold	T_{OFF}		155	165	175	°C
LOGIC INPUTS ($\overline{\text{IN0}}$, IN1, MOSI, SCK, $\overline{\text{RESET}}$, $\overline{\text{CE}}$)						
Threshold Voltage at Falling Edge	V_T-		0.2xV_{CC}	-	-	V
Threshold Voltage at Rising Edge	V_T+		-	-	0.7xV_{CC}	V
Hysteresis Voltage	V_H	V_T+ - V_T-	0.65	-	-	V
Input Current	I_{IN}	$V_{IN} = V_{CC}$	-	-	+10	µA
Input Pull-Up Resistance	R_{IN}		50	80	200	kΩ
Input Capacitance	C_{IN}		-	-	10	pF
Input Frequency, IN0, IN15	f_{IN}		DC	-	2	kHz
Active Supply Range for Reset State Change at $\overline{\text{RESET}}$ Pin	V_{HC-C_RST}	$\overline{\text{RESET}}$ Pin Forced Reset. (Note: Normal V_{CC} Functional Operating Range is 4.0V to 5.5V)	3.1	-	5.5	V
Low V_{CC} Active Reset Threshold	V_{LCC_RST}	Low V_{CC} Forced Reset, (Low Voltage Reset Active for 0 < V_{CC} < V_{LCC_RST})	3.1	-	4	V
LOGIC OUTPUT (MISO)						
Data Output LOW Voltage	V_{SOL}	I_{SO} = -3.2mA	-	0.2	0.4	V
Data Output HIGH Voltage	V_{SOH}	I_{SO} = -4mA	V_{CC} - 0.4V	-	-	V
Output Three-State Leakage Current	I_{SOL}	$\overline{\text{CE}}$ = High, 0V ≤ V_{SO} ≤ V_{CC}	-10	-	+10	µA
Output Capacitance	C_{SO}	f_{OPER} = 3MHz	-	-	10	pF

Serial Peripheral Interface Timing

(MOSI, MISO Load Capacitor = 100pF, See Figure 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Clock Frequency, 50% Duty Cycle	f_{CLK}		3	-	-	MHz
Enable Lead Time (SCK Change Low to High after $\overline{\text{CE}}$ = Low)	t_{LEAD}		100	-	-	ns
Enable Lag Time (Time for SCK Low before $\overline{\text{CE}}$ goes High)	t_{LAG}		150	-	-	ns
Minimum Time SCK = High	t_{WSCKH}		160	-	-	ns
Minimum Time SCK = Low	t_{WSCKL}		160	-	-	ns
Data Setup Time (SCK Change from High to Low after MOSI Data Valid)	t_{SU}		20	-	-	ns
Data Hold Time (MOSI Data Hold Time SCK Change from High to Low)	t_H			-	20	ns
Enable Time from $\overline{\text{CE}}$ = Low to Data at MISO	t_{EN}		-	-	100	ns
Disable Time (Time for $\overline{\text{CE}}$ Low to High to Output Data Float)	t_{DIS}		-	-	100	ns

Serial Peripheral Interface Timing (MOSI, MISO Load Capacitor = 100pF, See Figure 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Data Valid Time, SCK to Data at MISO Valid	t_V	V_{CC} = 5V ±0.1V	-	-	100	ns
Time for SCK Low before $\overline{CE}$ Low (SCK Setup Time before $\overline{CE}$ High to Low Change)	t_{SCK_LEAD}		100	-	-	ns
Time for SCK High after $\overline{CE}$ High	t_{SCK_LAG}		150	-	-	ns
$\overline{CE}$ Pulse Filter Time			-	Note 9	-	ns

NOTES:

7. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns-on the MOSFET; holding the Drain at the Output Clamp Voltage, V_{OC}.
8. The measurement of Output Leakage Current includes the Output Pull-Down Current, I_{SK}. Each Output has a Current Pull-Down which is used to detect open load fault conditions.
9. The digital filter time for the output latch function determines if the output latch function will be enabled. The output latch function will only be enabled if a positive $\overline{CE}$ slope occurs after 8 SCK clock cycles or a multiple of 8 SCK cycles since the last $\overline{CE}$ negative slope change.

Timing Diagrams

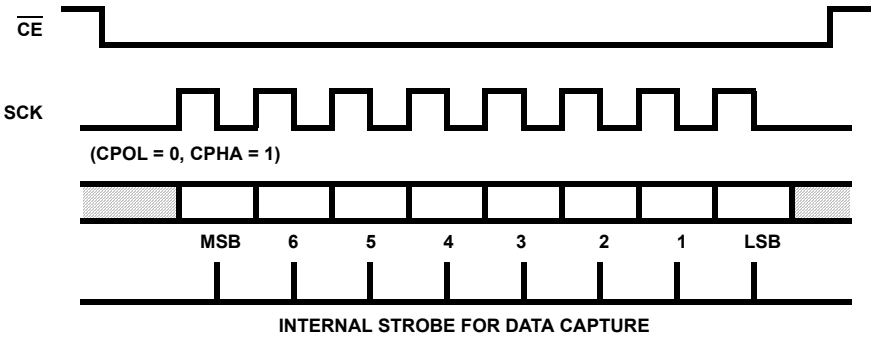


FIGURE 1A. DATA AND CLOCK TIMING DIAGRAM

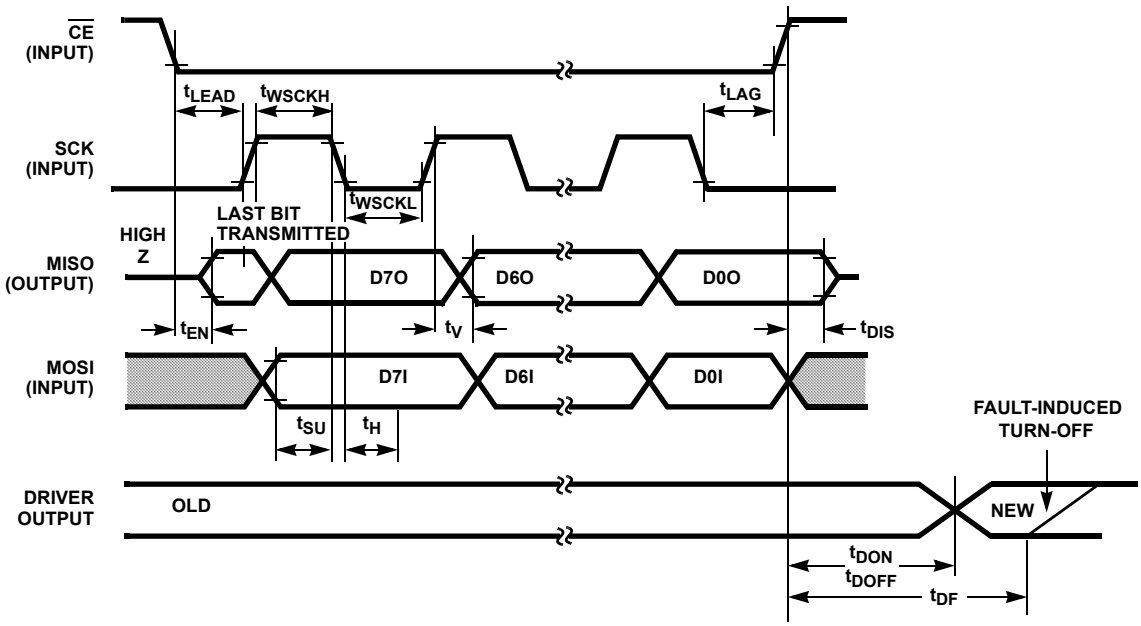


FIGURE 1B. SPI TIMING DIAGRAM

Timing Diagrams (Continued)

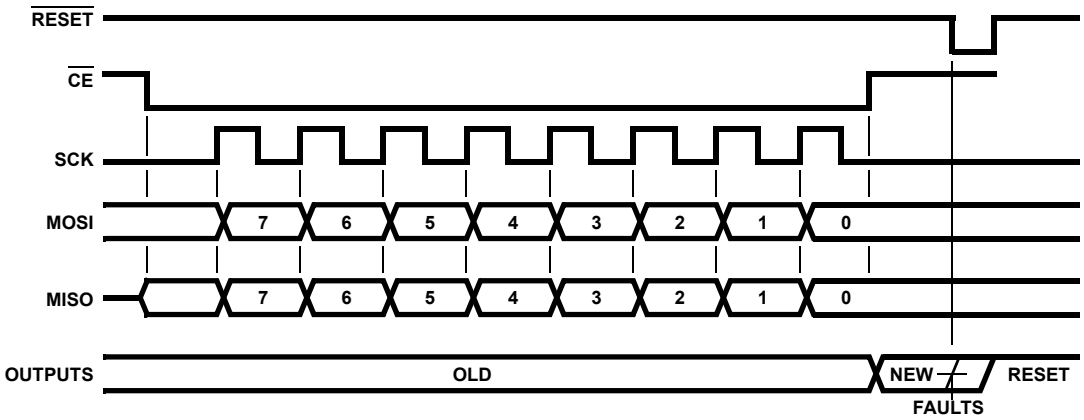


FIGURE 2. BYTE TIMING DIAGRAM WITH ASYNCHRONOUS RESET

Signal Pin Descriptions

Power Output Drivers, OUT0 - OUT7 - The input and output bits corresponding to Output 0 thru Output 7 are transmitted and received most significant bit (MSB) first via the SPI bus. Outputs OUT0 - 5 are provided with over-current shutdown. Current Limiting and Thermal Shutdown are provided on OUT6, 7 for application use as Lamp Drivers. After a fault shutdown, the control lines remain active. The fault latches must be cleared by turning the output off and on to reset the output to an ON state. OUT1, 2 latches may be cleared by the $\overline{\text{RESET}}$ pin.

$\overline{\text{RESET}}$ - Active low reset input. An internal pull-up is provided on-chip. When this input line is low, all output drivers are turned-off and the OUT1, 2 fault latches are cleared. An internal low voltage reset is ORed with the $\overline{\text{RESET}}$ input. When V_{CC} is less than V_{LCC_RST}, the internal reset is active.

$\overline{\text{CE}}$ - Active low chip enable. The falling edge of CE loads the shift register with the output status bits. Data is transferred from the shift register to the outputs on the rising edge of CE. The output driver for the MISO pin is enabled when CE goes low. CE must be a logic low prior to the first serial clock (SCK) and must remain low until after the last (eighth) serial clock cycle. All eight MOSI bits of input data must be loaded in the same sequence of SCK clock input. A digital filter is used in the $\overline{\text{CE}}$ line to insure that 8 (or a multiple of 8) clock cycles occurs while $\overline{\text{CE}}$ is active low. After SCK is low for a short period, t_{LAG}; CE may be changed from low to high to latch the input data. A low level on CE also activates an internal disable circuit used for unlatching output states that are in a fault mode as sensed by an out of saturation condition. A high on CE forces MISO to a high impedance state. Also, when CE is high, the octal driver ignores the SCK and MOSI signals.

IN0, 1 - IN0 and IN1 are Channels 0 and 1 direct parallel input controls. Refer to ‘Special Input Conditions for Channel 0, 1‘ in the following text.

SCK, MISO, MOSI - Refer to the ‘Serial Peripheral Interface’ (SPI) section in the following text.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a serial synchronous bus for control and data transfers. The Clock (SCK), which is generated by the microcomputer, is active only during data transfers. In systems using CDP68HC05 family microcomputers, the inactive clock polarity is determined by the CPOL bit in the microcomputer’s control register. The CPOL bit is used in conjunction with the clock phase bit, CPHA to produce the desired clock data relationship between the microcomputer and octal driver. The CPHA bit in general selects the clock edge which captures data and allows it to change states. For the HIP0045, the CPOL bit must be set to a logic zero and the CPHA bit to a logic one. Configured in this manner, MISO (output) data will appear with every rising edge of the SCK clock pulse, and MOSI (input) data will be latched into the shift register with every falling edge of the SCK clock pulse. Also, the steady state value of the inactive serial clock, SCK, will be at a low level. Timing diagrams for the serial peripheral interface are shown in Figure 1.

SPI Signal Descriptions

MOSI (Master Out/Slave In) - Serial data input. Data bytes are shifted in at this pin, most significant bit (MSB) first. The data is passed directly to the shift register which in turn controls the latches and output drivers.

MISO (Master In/Slave Out) - Serial data output. Data bytes are shifted out at this pin, most significant bit (MSB) first. This pin is the serial output from the shift register and is three stated when $\overline{\text{CE}}$ is high. Diagnostic Failure Register information is given in Tables 6 and 7. Determination of the fault condition may be done as a software sequence, based on MOSI data latched into the shift register and subsequent data clocked out of the MISO pin.

SCK - Serial clock input. The SCK signal clocks the shift register and new MOSI (input) data will be latched into the shift register on every falling edge of SCK. The SCK phase bit, CPHA=1 and the polarity bit, CPOL=0, must be set in the microcomputer's control register.

Functional Descriptions

The HIP0045 is a low quiescent power, high voltage, high current, octal, serial low side driver featuring eight channels of open drain MOS output drivers. Referring to the Detailed Block Diagram, the drivers have low r_{DSON} and low saturation voltage with over-voltage drain-to-gate zener clamp circuits. Each output is short circuit protected and suited for driving resistive or inductive loads such as solenoids, relays and lamps. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. Each channel is independently controlled by an output latch and a common $\overline{\text{RESET}}$ line that disables all eight outputs. Byte timing with asynchronous reset is shown in Figure 2.

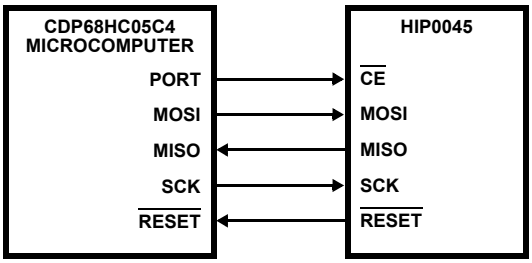


FIGURE 3. TYPICAL MICROCOMPUTER INTERFACE WITH THE HIP0045

The circuit receives 8-bit serial data by means of the serial input (MOSI), and stores this data in an internal register to control the output drivers. The serial output (MISO) provides 8-bit diagnostic data representing the voltage level at the driver output. This allows the microcomputer to diagnose the condition at the output drivers. The device is selected when the chip enable ($\overline{\text{CE}}$) line is low. When ($\overline{\text{CE}}$) is high, the device is deselected and the serial output (MISO) is placed in a three-state high impedance mode. The device shifts serial data on the rising edge of the serial clock (SCK), and latches data on the falling edge. On the rising edge of chip enable ($\overline{\text{CE}}$), new input data from the shift register is latched to control the output drivers. The falling edge of chip enable ($\overline{\text{CE}}$) transfers the output drivers fault information back to the shift register. The output drivers have low ON voltage at rated current, and are monitored by a comparator for an out of saturation condition, in which case the output driver with the fault becomes unlatched and diagnostic data is sent to the microcomputer via the MISO line. A typical microcomputer interface circuit is shown in Figure 3.

SPI Shift Register

The SPI shift register has both serial and parallel inputs and outputs. Serial output and input data are simultaneously transferred to and from the SPI bus. The serial input data is parallel latched into the 8-Bit Output Latch of the HIP0045 at the end of a data transfer. Diagnostic data, Diag0-7 is transferred to the shift register when $\overline{\text{CE}}$ goes low at the beginning of a data transfer cycle.

8-Bit Output Latch

The 8-Bit Output Latch is used to control the output drivers. New serial data is transferred from the shift register to the 8-Bit Output Latch when CE goes high. The 8-Bit Output Latch is cleared by an active low $\overline{\text{RESET}}$ signal.

Output Drivers

The output drivers provide an active low output of 500mA nominal with current limiting set to greater than 1.05A to allow for high inrush currents. In addition, each output is provided with a voltage drain-to-gate clamp circuit to limit inductive transients. Each output driver is also monitored by a comparator for an out of saturation condition. If the output voltage of an ON output pin exceeds the saturation voltage limit, a fault latch turns off the output. The threshold comparators are used to detect shorts to the power supply, shorts to ground and open loads. Each comparator provides status data to the shift register for diagnostic feedback. An internal pull-down current, I_{SK} at each output will provide an indicator for low output voltage if the output is programmed OFF and the output line is open. Refer to Tables 6 and 7 for Fault information versus output control and V_{REF}. Note that V_{REF} is the out-of-saturation threshold for an ON state. When the output is switched off and V_{REF} is low, an open-load or ground fault is indicated.

$\overline{\text{CE}}$ High to Low Transition

When $\overline{\text{CE}}$ is low the three-state MISO pin is enabled. On the falling edge of $\overline{\text{CE}}$, diagnostic and status data from the output voltage comparators will be latched into the shift register. During the time that $\overline{\text{CE}}$ is low, data bytes controlling the output drivers are shifted in at the MOSI pin most significant bit (MSB) first. Tables 1, 2 and 3 define the logic state for control of each output and Table 4 defines the control bit structure.

$\overline{\text{CE}}$ Low to High Transition

When the last serial data bit has been shifted into the MOSI pin, $\overline{\text{CE}}$ pin is pulled high to transfer data from the shift register into the 8-bit parallel output latch to activate the outputs. The serial clock input pin (SCK) should be low during $\overline{\text{CE}}$ transitions to avoid false clocking of the shift register. The SCK input is gated by $\overline{\text{CE}}$ so that the SCK input is ignored when $\overline{\text{CE}}$ is high.

Detecting Fault Conditions

Fault conditions may be checked as follows: SCK is always low when $\overline{CE}$ is changing. When $\overline{CE}$ goes low, the MISO output is taken out of the three-state mode and the Output status information is latched into the shift register. While $\overline{CE}$ is low, data bits in the shift register are transferred to the MISO output on each positive SCK clock transition and data bits present at the MOSI input are transferred into the shift register on each negative transition of SCK. To verify Status and Diagnostic conditions, clock in a new control byte and wait approximately 150µs to allow the outputs to settle. Clock in the same control byte and compare this to the data output at the MISO pin. If there is a disparity, use Tables 5, 6 and 7 to determine the fault or status condition. (Use Tables 1, 2, 3 and 4 to establish the ON/OFF conditions for each output).

Based on the needs of the application, a software sequence should be programmed into the microcontroller to set the corrective action of each fault condition.

TABLE 5. DIAGNOSTIC FAILURE REGISTER STRUCTURE

Diag1 (D7O)	Diag3 (D6O)	Diag5 (D5O)	Diag7 (D4O)	Diag0 (D3O)	Diag2 (D2O)	Diag4 (D1O)	Diag6 (D0O)
MSB							**LSB**

NOTE:

10. The Diagnostic Failure Register bits Diag0 -7 have the same order as the Control Register bits Q0 - 7 as defined in Table 4. Data bits D0O - D7O give the MISO SPI serial output flow sequence.

TABLE 6. DEFINITION OF Diag0, 1 FAULT BITS FOR OUT0, 1 IN PARALLEL-CONTROLLED MODE

OUTPUT STATE	V_{REF} STATUS	FAULT BIT	FAULT MODE
OFF	$>V_{REF}$	H	No Fault
OFF	$<V_{REF}$	L	Open Load or GND Short
ON	$<V_{REF}$	H	No Fault
ON	$>V_{REF}$	L	Short to V_{BATT}

TABLE 7. DEFINITION OF Diag0-7 STATUS BITS FOR OUT0-7

OUTPUT STATE	V_{REF} STATUS	STATUS BIT	FAULT MODE
OFF	$>V_{REF}$	H	No Fault
OFF	$<V_{REF}$	L	Open Load or GND Short
ON	$<V_{REF}$	L	No Fault
ON	$>V_{REF}$	H	Short to V_{BATT} (Chan. 0-7); or Over-Temperature Fault (Chan. 6, 7)

NOTES:

11. For Channel 0 (Diag0) and Channel 1 (Diag1): Fault Bit High = No Fault; Fault Bit Low = Fault Occurred.

12. V_{REF} is the threshold reference level for detecting an Open Load. Refer to the Electrical Specification for the V_{REF} voltage level.

Special Conditions for Channel 0, 1

Referring to the Detailed Block Diagram, Channel's 0, 1 are configured to externally provide control of the ON/OFF state. The inputs, IN0 and IN1, are ORed with the SPI ON/OFF control bit. In this configuration with IN0 and IN1 high, SPI control latches Diag0 and Diag1 as status bits. When the IN0 and IN1 inputs are active, a fault condition is detected by a comparison of IN0 and IN1 to OUT0 and OUT1 respectively causing the Fault Detector to latch a fault bit. The resulting Fault output is latched as diagnostic bit, Diag0 or Diag1. The Diag0 and Diag1 outputs give the status or fault condition of the output drivers as shown in Table 6. Fault detection is disabled during switching/settling time.

The Diag0 and Diag1 bits from Channel 0 and 1 respectively indicate a fault when the FAULT BIT is Low, given IN1 and IN0 control. Otherwise Diag0 and Diag1 are status bits when controlled by the SPI input. Note that the SPI Bit, given in Tables 1 and 2 overrides the ON state control from IN0 and IN1.

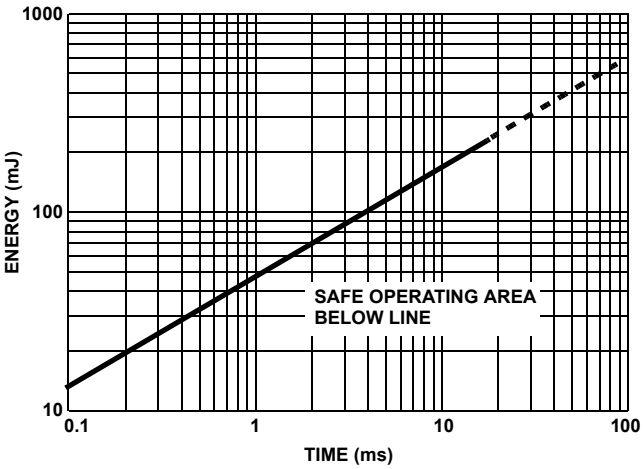
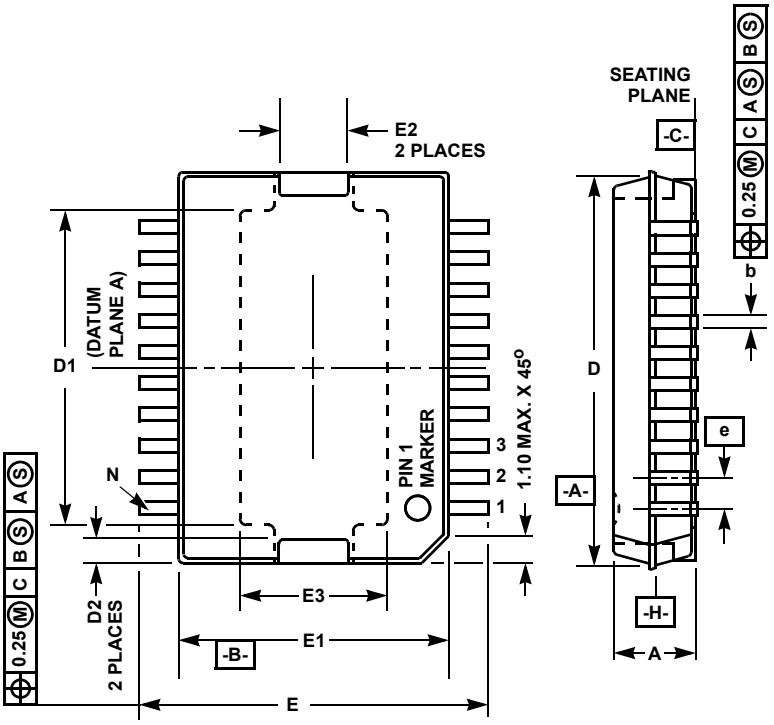
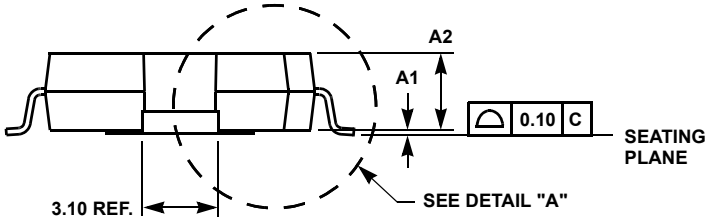
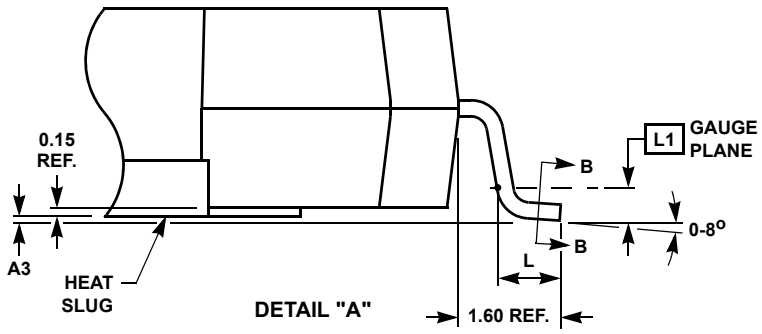


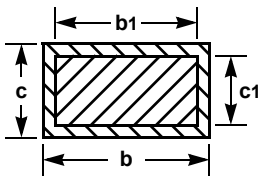
FIGURE 4. MAXIMUM SINGLE PULSE ENERGY SAFE OPERATING AREA FOR EACH CLAMPED OUTPUT DRIVER, $T_A = 25^oC$

Power Small Outline Plastic Package (PSOP)









SECTION "B-B"

M20.433

20 LEAD POWER SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.122	0.142	3.10	3.60	-
A1	0.004	0.012	0.10	0.30	-
A2	0.118	0.130	3.00	3.30	-
A3	0.000	0.004	0.00	0.10	-
b	0.016	0.021	0.40	0.53	6, 7
b1	0.016	0.020	0.40	0.50	6, 7
c	0.009	0.013	0.23	0.32	7
c1	0.009	0.011	0.23	0.29	7
D	0.622	0.630	15.80	16.00	3
D1	0.496	0.512	12.60	13.00	-
D2	-	0.043	-	1.10	-
E	0.547	0.571	13.90	14.50	-
E1	0.429	0.437	10.90	11.10	4
E2	-	0.114	-	2.90	-
E3	0.228	0.244	5.80	6.20	-
e	0.050 BSC		1.27 BSC		-
L	0.031	0.043	0.80	1.10	5
L1	0.014 BSC		0.35 BSC		-
N	20		20		-

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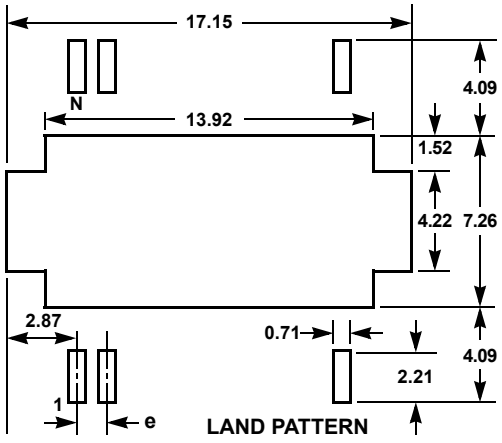
NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "C" is a reference datum. Seating plane is defined by lead tips only.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side. D measured at -H-.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side. E1 measured at -H-.
5. Dimension "L" is the length of terminal for soldering to a substrate.
6. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the lead width dimension at maximum material condition.
7. Section "B-B" to be determined at 0.10mm to 0.25mm from the lead tip.
8. Controlling dimension: MILLIMETER.
9. Dimensions conform with JEDEC Outline MO-166AA Issue B.



LAND PATTERN