OBSOLETE PRODUCT
No Recommended Replacement

August 1998 File Number 3208.2

Power Control IC Single Chip Dual Switching Power Supply

The HIP5062 is a complete power control IC, incorporating two high power DMOS transistors, CMOS logic and two low level analog control circuits on the same Intelligent Power IC. Both the standard “Boost” and the “SEPIC” (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor’s current and voltage capability (5A and 60V), multiple output power supplies with total output power capability up to 100W are possible.

Features

- Two Current Mode Control Regulators
- Two 60V, 5A On-chip DMOS Transistors
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
- Output Rise and Fall Times ~ 3ns
- Designed for 26V to 42V Operation

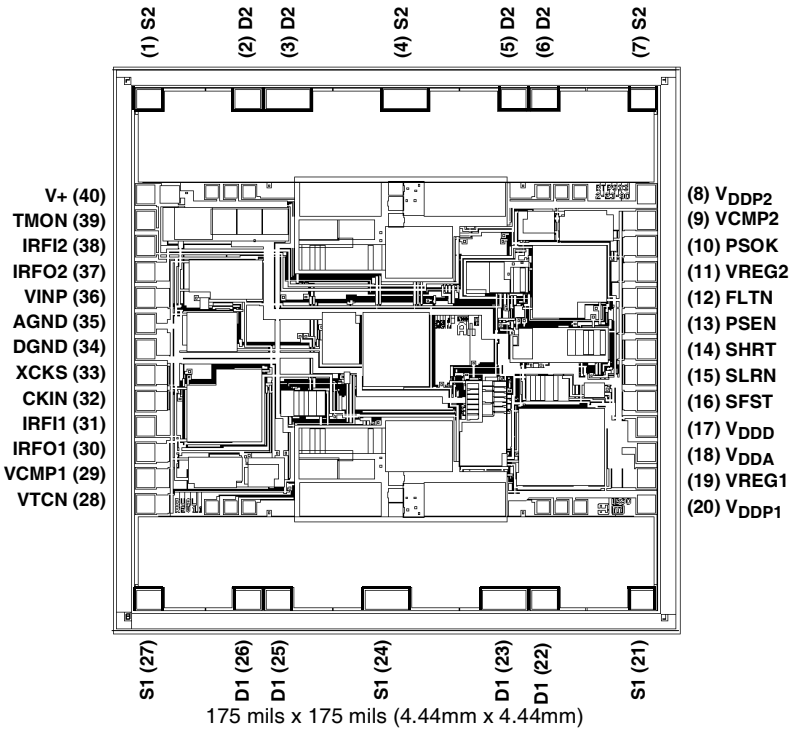
Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Ordering Information

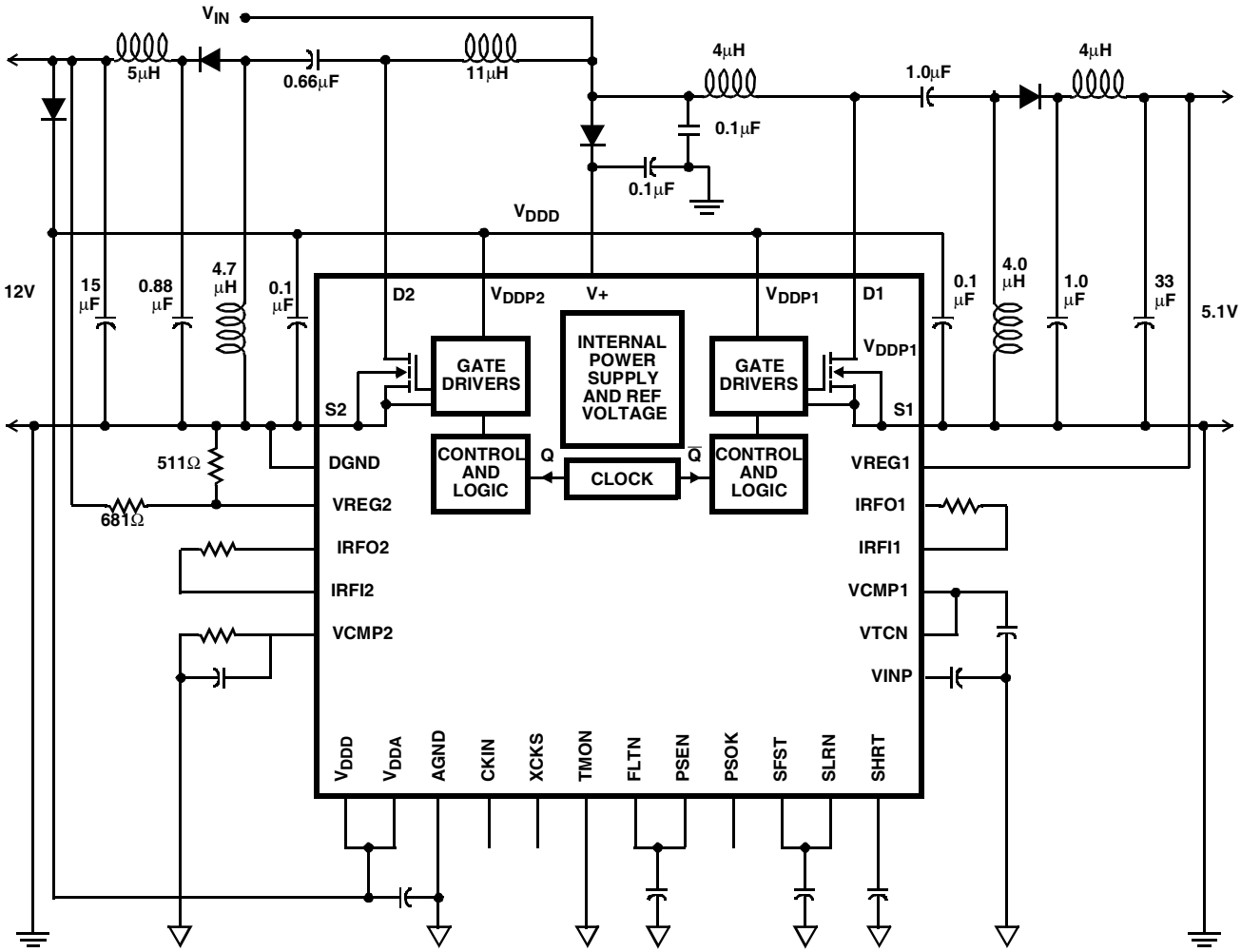
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5062DY	0^{o}C to +85^{o}C	40 Pad Chip
HIP5062DW	0^{o}C to +85^{o}C	Wafer

Chip



175 mils x 175 mils (4.44mm x 4.44mm)

Simplified Block Diagram



TYPICAL SEPIC CONFIGURATION

Absolute Maximum Ratings

DC Supply Voltage, V+. . . . . -0.3V to 42V
DMOS Drain Voltage . . . . . -0.3V to 60V
DMOS Drain Current 10A
DC Logic Supply. . . . . -0.3V to 16V
Output Voltage, Logic Outputs . . . . . -0.3V to 16V
Input Voltage, Analog and Logic. . . . . -0.3V to 16V
Operating Junction Temperature Range . . . . . .0^oC to $+110^oC$
Storage Temperature Range . . . . . -55^oC to $+150^oC$

Thermal Information

Thermal Resistance (θ_{JC})
(Solder Mounted to 0.050" Thick Copper Heat Sink) . . . . . $3^oC/W$ Max
Maximum Junction Temperature. . . . . $+110^oC$
(Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 36V, Channels 1 and 2, $T_J = 0^oC$ to $+110^oC$; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	V+ = 42V, PSEN = 12V	-	24.7	30	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 30V to 42V, I_{OUT} = 0mA	11.7	-	13.3	V
		V+ = 30V to 42V, I_{OUT} = 30mA	11.5	-	13.3	V
		SLRN = 12V, I_{OUT} = 0mA	11.5	-	13.3	V
VINP	Reference Voltage	VDDA = SLRN = 12V, I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$\lvert V_{IO} \rvert$	Input Offset Voltage (REG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	39	-	85	kΩ
g_m (VREG)	VREG Transconductance (I_{VCMP}/(VREG - VINP)	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance I_{VCMP}/(VREG - SFST)	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.05	-	6.5	V
CLOCK						
fq	Internal Clock Frequency	XCKS = 12V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages		33	-	66	$\%V_{DDD}$
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 2.5A, V_{DDD} = 11V, $T_J = +25^oC$	-	-	0.22	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	μA
CURRENT CONTROLED PWM						
$\lvert V_{IO} \rvert$ VCMP	Buffer Offset Voltage (VCOMP - V_{IFRO})	IFRO = 0mA to -5mA, VTCN = 0.2V to 7.6V, VCMP2 = 0.2V to 7.6V	-	-	125	mV

Electrical Specifications V+ = 36V, Channels 1 and 2, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH} IFRO	Voltage at IRFO that disables PWM. This is due to low load current		116	-	250	mV
I_{TH} IFRO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Conditions		6.85	-	7.65	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 7.7V	-75	-	-33	µA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch	V_{DDD} = 11V	-	5	-	V
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	2.0	-	3.2	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS}	Current Comparator Response Time (Note 1)	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/µs	-	30	-	ns
MCPW	Minimum Controllable Pulse Width (Note 1)		25	50	100	ns
MCPI	Minimum Controllable DMOS Peak Current (Note 1)		125	250	500	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		23	-	26.3	V
	Falling V+ Power-Off Set Voltage		-	15	-	V
	V+ Power-On Hysteresis		9.5	-	11.8	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply	V_{DDD} = 11V	3.6	-	6.5	V
r_{PSEN}	Internal Pull-Up Resistance, to V_{DDD}		-	12	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 11V	-1.5	-1.0	-0.65	µA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 11V, PSOK = 12V	-1	-	1	µA
V_{PSOK}	PSOK Low-State Voltage	SFST = 0V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}	V_{DDD} = 11V	8.1	-	9.9	V
THERMAL MONITOR						
TEMP	Substrate Temperature for Thermal Monitor to Trip (Note 1)	TMON = 0V	105	-	135	°C

NOTE:

1. Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1, 4, 7	S2	Source pads for the channel 2 regulator.
2, 3, 5, 6	D2	Drain pads for the channel 2 regulator.
8	V_{DDP2}	This pad is the power input for the channel 2 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1μF chip capacitor placed close to this pad and the DMOS source pads.
9	VCMP2	Output of the second channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
10	PSOK	This pad provides delayed positive indication when both supplies are enabled.
11	VREG2	Input to the transconductance error amplifier. The other common input for both amplifiers is VINP, Pad 36.
12	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced. V+ must be powered down to reset.
13	PSEN	This terminal is provided to activate the converter. When the input is low, the DMOS drivers are disabled. There is an internal 12K pull-up resistor on this terminal.
14	SHRT	50μA is internally applied to this node when there is an over-current condition.
15	SLRN	Control input to internal regulator that is used during the “start-up” of the supply. In normal operation this terminal starts at 0V and shuts down the internal regulator at approximately 9V. This pad is usually connected to SFST, pad 16.
16	SFST	Controls the rate of rise of both output voltages. Time is determined by an internal 1μA current source and an external capacitor.
17	V_{DDD}	Voltage input for the chip’s digital circuits. This pad also allows decoupling of this supply.
18	V_{DDA}	This is the analog supply and internal 12V regulator output usually used only during the start-up sequence. The internal regulator reduced to a nominal 9.2V when SLRN is returned to 12V. Output current capability is 30mA at both voltages.
19	VREG1	Input to channel one transconductance error amplifier. The other, common input for both amplifiers is VINP, pad 36.
20	V_{DDP1}	This pad is the power input for the channel 1 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1μF chip capacitor placed close to this pad and the DMOS source pads.
22, 23, 25, 26	D1	Drain pads for the channel 1 regulator.
21, 24, 27	S1	Source pads for the channel 1 regulator.
28	VTCN	Input to transconductance amplifier buffer for channel 1 only. Normally connected to VCMP1, pad 29.
29	VCMP1	Output of the first channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
30	IRFO1	A resistor placed between this pad and IRFI1 converts the VCMP1 signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP1 is 7.3V. Maximum output current should be kept below 10A.
31	IRFI1	See IRFO1.

Pin Descriptions (Continued)

PAD NUMBER	DESIGNATION	DESCRIPTION
32	CKIN	Clock input when XCKS is grounded.
33	XCKS	Grounding this terminal provides for the application of an external clock to CKIN input terminal. For normal internal clock operation, this terminal may be left floating or returned to 12V. There is an internal 30K pull-up resistor on this terminal.
34	DGND	Ground of the DMOS gate drivers. This pad is used for bypassing.
35	AGND	Analog ground.
36	VINP	Internal 5.1V reference. This point is usually bypassed.
37	IRFO2	A resistor placed between this pad and IRFI2 converts the VCMP2 signal to a current for the current sense comparator. The maximum current set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP2 is 7.3V. Maximum output current should be kept below 10A.
38	IRFI2	See IRFO2.
39	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Thermal shutdown occurs at a nominal junction temperature or $+120^{o}C$. This terminal is normally returned to ground.
40	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.1μF capacitor.

Functional Block Diagram