



DATA SHEET

(DOC No. HM01B0-DS)

>> **HM01B0**

1/11" 320 x 320 ▪ QVGA 60FPS
CMOS Image Sensor

Preliminary version 05 September, 2016

>> HM01B0 Ultra Low Power

1/11" 320 x 320 ▪ QVGA 60FPS CMOS Image Sensor



Himax Imaging, Inc.
http://www.himax.com.tw

September, 2016

Features

- Ultra Low Power Image Sensor designed for Always-on vision devices and applications
- High sensitivity 3.6μ BrightSense™ pixel technology
- 324 x 324 active pixel resolution with support for QVGA window, vertical flip and horizontal mirror readout
- <1.1mW QQVGA resolution at 30FPS,
< 2mW QVGA resolution at 30FPS
- Programmable black level calibration target, frame size, frame rate, exposure, analog gain (**up to 8x**) and digital gain (**up to 4x**)
- Automatic exposure and gain control loop with support for 50 / 60Hz flicker avoidance
- Flexible 1-bit, 4-bit and 8-bit video data interface with video frame and line sync
- Motion Detection circuit with programmable ROI and detection threshold with digital output to serve as an interrupt
- On-chip self oscillator
- I2C 2-wire serial interface for register access
- CSP and Bare Die sensor package option
- High CRA for low profile module design

Key Parameters

Sensor parameters	Value
Pixel Array (Active/ Effective)	324 x 324 / 320 x 320
Pixel Size	3.6μm x 3.6μm
Image Diagonal	1.63mm
Optical Format	Full frame 1/11"; QVGA 1/13"
Color Filter Array	Bayer, Monochrome
Shutter Type	Electronic Rolling Shutter
Frame Rate (Max.) (8-bit interface)	8-bit, 320p 45FPS @ 6MHz 8-bit, QVGA 60FPS @ 6MHz
Frame Rate _{MAX} (4-bit interface)	8-bit, 320p 45FPS @ 12MHz 8-bit, QVGA 60FPS @ 12MHz
Frame Rate _{MAX} (1-bit interface)	8-bit, 320p 30FPS @ 36MHz 8-bit, QVGA 45FPS @ 36MHz
S/N Ratio _{MAX}	38.7dB
Dynamic Range (1x / 8x)	64dB / 70dB
Sensitivity @ 530nm	5.6 V / Lux-sec
Pixel CRA _{MAX}	30°

Sensor parameters	Value
Supply Voltage (Typ.)	AVDD 2.8V
	DVDD (LDO) 1.5V (1.8, 2.8V)
	IOVDD 1.8 / 2.8V
Input Reference Clock	3 – 36MHz
Serial Interface	I2C, 400kHz max.
Video Data Interface	8-bit, 4-bit, 1-bit data output FVLD, LVLD, PCLK
Pixel Clock (PCLK) (MAX.)	36MHz
Output Format	6-bit / 8-bit RAW
Digital Output	Motion Interrupt (Active High)
Control Loop	Black Level, Exposure / Gain
Power Consumption (Typ.)	8-bit, QQVGA 30FPS 1.1mW
	8-bit, QVGA 30FPS <2mW
	8-bit, QVGA 60FPS <4mW
	Standby 200μW
Temperature	Operating -30 °C to 85 °C
	Stable Image -0 °C to 60 °C

Order Information

Part no.	Color option	Operating / Storage temperature	Package
HM01B0-AWA	RGB	- 20 °C to 85 °C / - 30 °C to 85 °C	CSP
HM01B0-MWA	Mono	- 20 °C to 85 °C / - 30 °C to 85 °C	CSP
HM01B0-AGA	RGB	- 20 °C to 85 °C / - 30 °C to 85 °C	Bare Die
HM01B0- MGA	Mono	- 20 °C to 85 °C / - 30 °C to 85 °C	Bare Die
HM01B0-ANA	RGB	- 20 °C to 85 °C / - 30 °C to 85 °C	NeoPAC
HM01B0- MNA	Mono	- 20 °C to 85 °C / - 30 °C to 85 °C	NeoPAC

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1/11" 320 x 320 ▪ QVGA 60FPS CMOS

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Revision History

September, 2016

Version	Date	Description of changes
01	2016/02/04	New setup.
02	2016/04/26	1. Add test pattern for QVGA mode. 2. Modify QVGA window readout and full frame size. 3. Modify clock divider. 4. Remove hardware trigger N frame output mode. 5. Modify IOVDD voltage to 1.8V /2.8V. 6. Correct AGAIN setting. 7. Constraint for line length and frame length. 8. The minimum integration time is 2 rows. 9. Modify PCLKO polarity in gate mode. 10. Correct wrong pin name HSYNC and VSYNC in IO control options. 11. Modify maximum frame rate from 51 FPS to 45 FPS for full frame. 12. Add description: QVGA do not support the Bayer sensor version. 13. Modify stop mode to standby mode in rest. 14. Add bare die package and 8 bit parallel interface for bare die.
03	2016/05/13	1. Modify the description in Monochrome QVGA using Pixel Binning and Features 2. Rename 5.2.1, 5.2.2, 5.3.1 and 5.3.2 3. Add output pin status control by register and remove IO status in table 4. 4. Remove register of GROU and RGB stat ratio. 5. Add sensor address control register. 6. Modify clock divider. 7. Add VSYNC, HSYNC shift register. 8. Modify power consumption QVGA 30FPS from 670 μ W to 1.1mW.
04	2016/08/22	Page 2 1. Modify 'Key Parameters'. Page 15 2. Modify 'Figure 4.1: ISP blocks'. Page 23~24 3. Modify chapter '6.1 Operating modes'. Page 24 4. Modify chapter '6.2 Reset'. Page 26 5. Modify chapter '6.4 Clock setup'. 6. Modify chapter '6.4.1 MCLK and self-oscillator mode switch'. Page 27 7. Modify 'Figure 6.5: Non-gated and gated serial data clock option'. Page 29 8. Modify 'Figure 6.7: 6-bit and 8-bit RAW output format on 4-bit data IO interface'. 9. Modify 'Figure 6.8: RAW output format on serial data IO interface'. Page 30 10. Add chapter '7.1 I2C slave address ID'. Page 32 11. Modify chapter '8.1 Frame retiming'. 12. Remove Modify 'Table 8.1: Global analog gain settings'. 13. Add chapter '8.3 Suggestion for analog gain and digital gain'. Page 38 14. Modify chapter '9.14 IO and clock control'.

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Revision History

September, 2016

Version	Date	Description of changes
		Page 40 15. Modify chapter '10.2 Operating voltages'. Page 41 16. Modify chapter '10.3 DC characteristics'. 17. Modify chapter '10.4 Master clock input (MCLK). Page 43 18. Modify chapter '10.6 Parallel interface timing characteristics'. Page 44 19. Modify chapter '10.7 Serial interface timing characteristics'.
05	2016/09/13	Page 2 1. Modify 'Order Information'. Page 12 2. Add chapter '1.3 NeoPAC'. Page 20 3. Add chapter '5.1.3 External LDO mode (NeoPAC)'. Page 23 4. Add chapter '5.2.3 2.8V / 1.8V dual supply mode (NeoPAC)'. Page 26 5. Add chapter '5.3.3 2.8V signal supply Mode (NeoPAC)'. Page 38 6. Modify chapter '9.3 Sensor exposure gain control', 0x020E & 0x020F description. Page 42 7. Modify chapter '9.14 IO and clock control', 0x3064 [2] description.

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Preliminary Version 05

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1. Package Information

1.1 Bare die

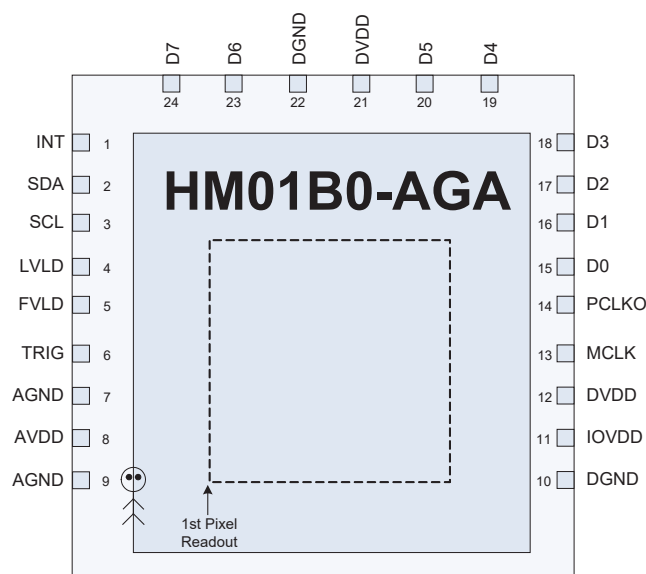


Figure 1.1: Bare die diagram (Top view)

Pin no.	Pin name	Type	Description
1	INT	Out	Interrupt output (Active High).
2	SDA	In/Out	Serial data I/O (Open drain).
3	SCL	In	I2C serial clock.
4	LVLD	Out	Line valid output.
5	FVLD	Out	Frame valid output.
6	TRIG	In	Frame trigger input (Internal pull down / Active high).
7	AGND	Ground	Analog ground.
8	AVDD	Power	Analog power (2.8V).
9	AGND	Ground	Analog ground.
10	DGND	Ground	Digital ground.
11	IOVDD	Power	IO power (1.8V/2.8V).
12	DVDD	Power	Digital power (1.5 V).
13	MCLK	In	Master clock input.
14	PCLKO / SCK	Out	Pixel clock / serial clock output.
15	D0 / SDO	Out	Data 0 output / Serial output.
16	D1	Out	Data 1 output.
17	D2	Out	Data 2 output.
18	D3	Out	Data 3 output.
19	D4	Out	Data 4 output.
20	D5	Out	Data 5 output.
21	DVDD	Power	Digital power (1.5 V).
22	DGND	Ground	Digital ground.
23	D6	Out	Data 6 output.
24	D7	Out	Data 7 output.

Table 1.1: Bare die pin description

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1.2 Chip scale package

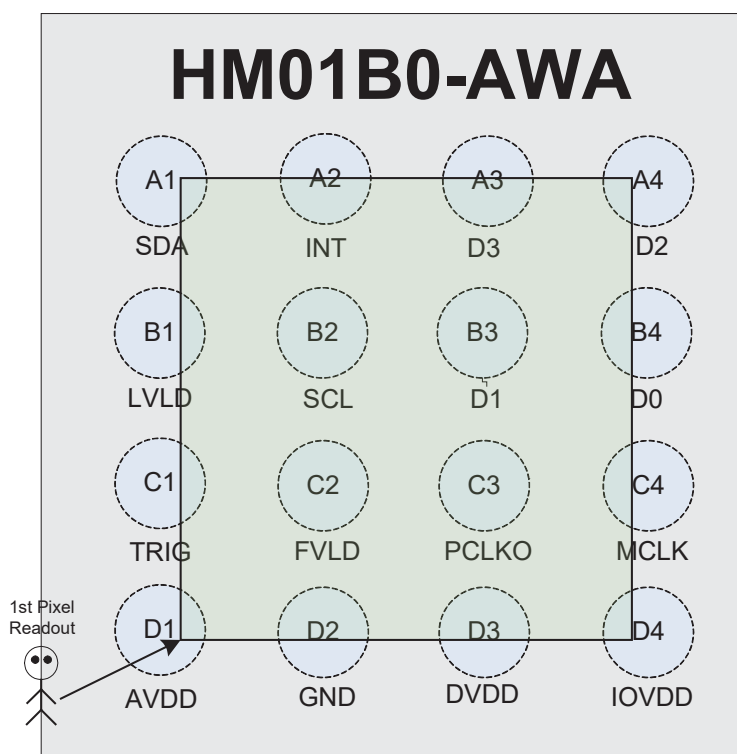


Figure 1.2: CSP pin diagram (Top view)

Pin no.	Pin name	Type	Description
A1	SDA	I/O	Serial Data I/O (Open Drain).
A2	INT	OUTPUT	Interrupt Output (Active High).
A3	D3	OUTPUT	Data 3 output.
A4	D2	OUTPUT	Data 2 output.
B1	LVLD	OUTPUT	Line valid output.
B2	SCL	INPUT	I2C serial clock.
B3	D1	OUTPUT	Data 1 output.
B4	D0/SDO	OUTPUT	Data 0 / Serial data output.
C1	TRIG	INPUT	Frame trigger input (Internal pull down active high).
C2	FVLD	OUTPUT	Frame valid output.
C3	PCLKO / SCK	OUTPUT	Pixel clock / serial clock output.
C4	MCLK	INPUT	Master clock input.
D1	AVDD	POWER	Analog power (2.8V).
D2	GND	GROUND	Ground.
D3	DVDD	POWER	Digital power (1.5 V).
D4	IOVDD	POWER	IO power (1.8V / 2.8V).

Table 1.2: CSP pin description

1.3 NeoPAC

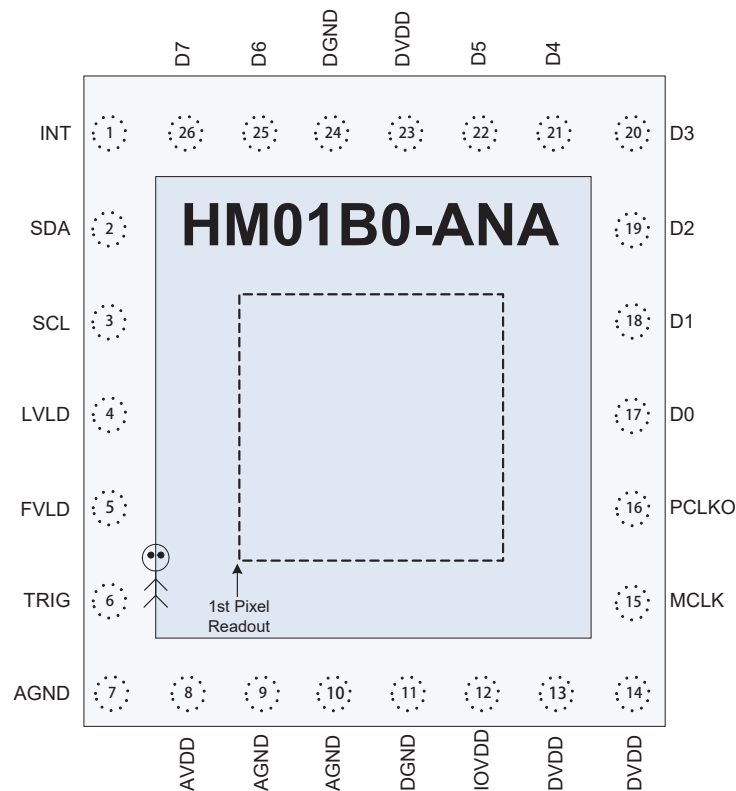


Figure 1.3: NeoPAC diagram (Top view)

Pin no.	Pin name	Type	Description
1	INT	Out	Interrupt output (Active High).
2	SDA	In/Out	Serial data I/O (Open drain).
3	SCL	In	I2C serial clock.
4	LVLD	Out	Line valid output.
5	FVLD	Out	Frame valid output.
6	TRIG	In	Frame trigger input (Internal pull down / Active high).
7	AGND	Ground	Analog ground.
8	AVDD	Power	Analog power (2.8V).
9	AGND	Ground	Analog ground.
10	AGND	Ground	Analog ground.
11	DGND	Ground	Digital ground.
12	IOVDD	Power	IO power (1.8V/2.8V).
13	DVDD	Power	Digital power (1.5 V).
14	DVDD	Power	Digital power (1.5 V).
15	MCLK	In	Master clock input.
16	PCLKO / SCK	Out	Pixel Clock / Serial clock output.
17	D0 / SDO	Out	Data 0 output / Serial output.
18	D1	Out	Data 1 output.
19	D2	Out	Data 2 output.
20	D3	Out	Data 3 output.
21	D4	Out	Data 4 output.
22	D5	Out	Data 5 output.
23	DVDD	Power	Digital power (1.5 V).
24	DGND	Ground	Digital ground.
25	D6	Out	Data 6 output.
26	D7	Out	Data 7 output.

Table 1.3: NeoPAC pin description

2. Sensor Overview

The HM01B0 is an Ultra Low Power Image Sensor (**ULPIS**) that enables the integration of an “Always-on” camera for computer vision applications such as gestures, intelligent ambient light and proximity sensing, tracking and object identification. The unique architecture of the sensor enables the sensor to consume very low power of <4mW at QVGA 60FPS, <2mW at QVGA 30FPS, and <1.1mW at QQVGA 30FPS.

The HM01B0 contains 324 x 324 pixel resolutions and supports a 324 x 244 window mode which can be readout at a maximum frame rate of 60FPS, and a 2x2 monochrome binning mode with a maximum frame rate of 120FPS. The video data is transferred over a configurable 1-bit, 4-bit or 8-bit video interface with support for frame and line synchronization. The sensor integrates a black level calibration circuit, automatic exposure and gain control loop, self-oscillator and motion detection circuit with interrupt output to reduce host computation and commands to the sensor to optimize the system power consumption.

The sensor is available in a Chip Scale Package (**CSP**) or bare die and measures less than 5mm². The sensor supports single, dual or triple power supply configuration and requires only 3 passive components enabling a highly compact camera module design for devices such as IoT, wearable, smart building, smart phone, tablets and slim notebooks.

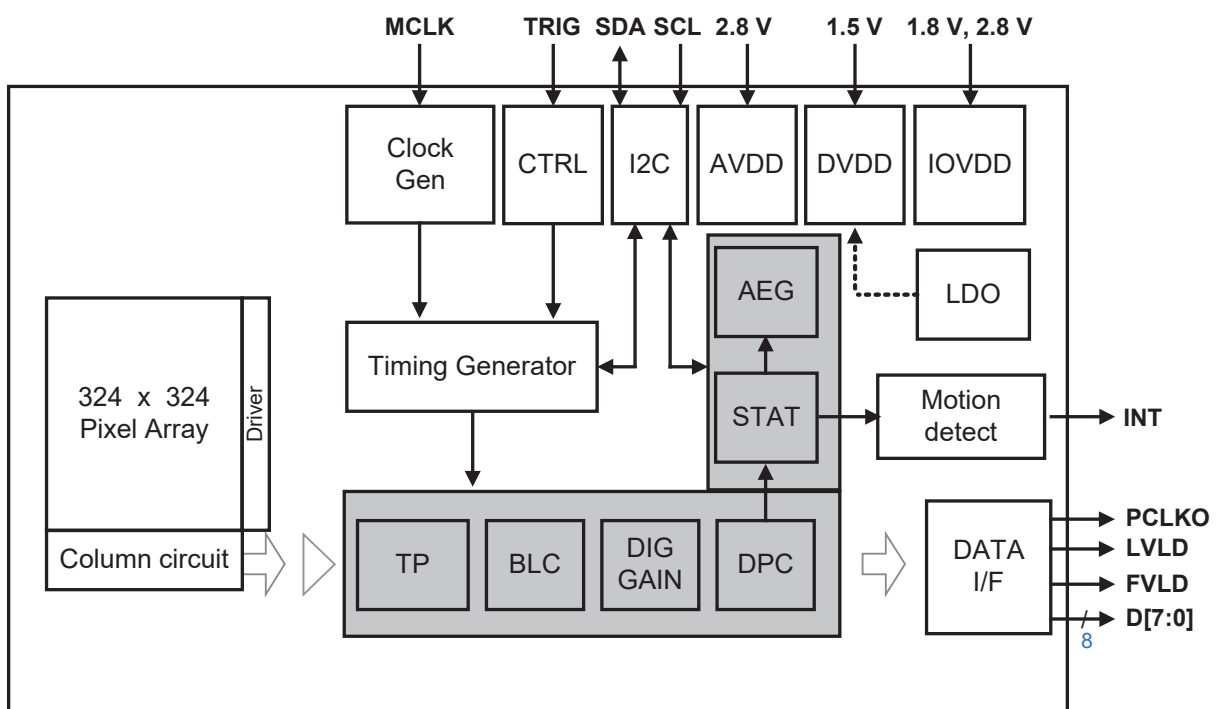


Figure 2.1: HM01B0 block diagram

3. Sensor Core and Function Description

3.1 Sensor array

The HM01B0 consists of an active pixel array of 324 columns and 324 rows. The sensor maximum effective resolution is 320 columns and 320 rows which include 4 border pixels.

For the sensors with color filter, the even numbered rows contain the Blue (**B**) and Green (**G₁**) pixel, and the odd numbered row contains the Red (**R**) and Green (**G₂**) pixels; the even numbered columns contain the Green (**G₂**) and Blue (**B**) pixels, and the odd column contains the Red (**R**) and Green (**G₁**) pixels. Optically black rows are used by the sensor for black level calibration. Programmable horizontal and vertical blanking time adjusts the line width and frame height, respectively.

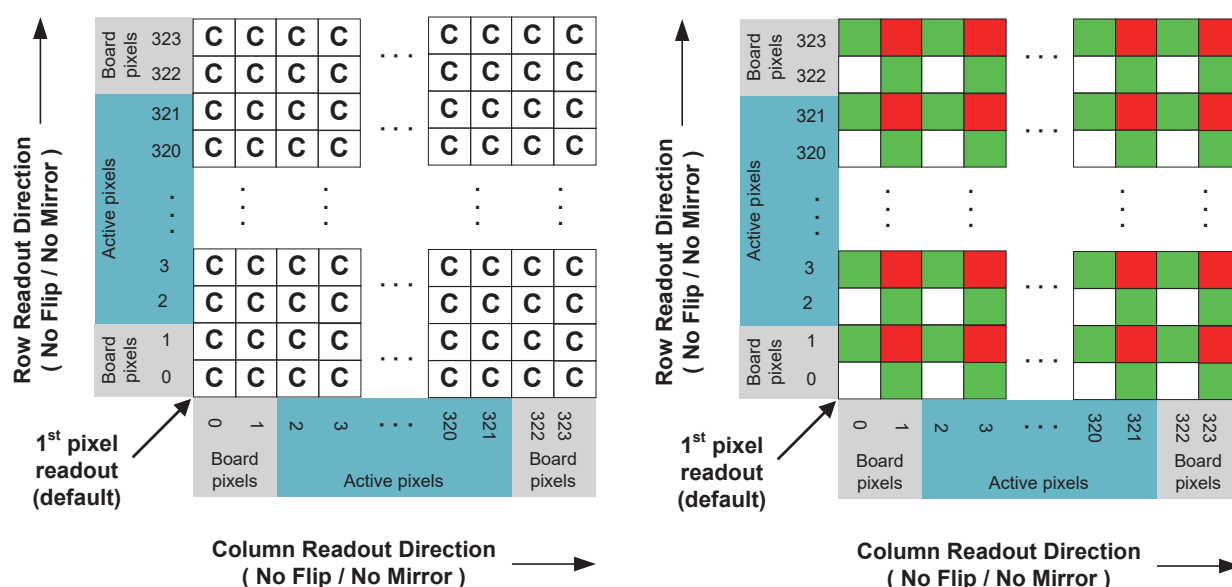


Figure 3.1: Full resolution pixel readout (Monochrome)

3.2 QVGA window readout

The QVGA sensor window with an active resolution of 324 x 244 pixels is programmed by setting register 0x3010[0] to 1. The location of the window is fixed such that the coordinate of the first pixel read out location is 0, 40.

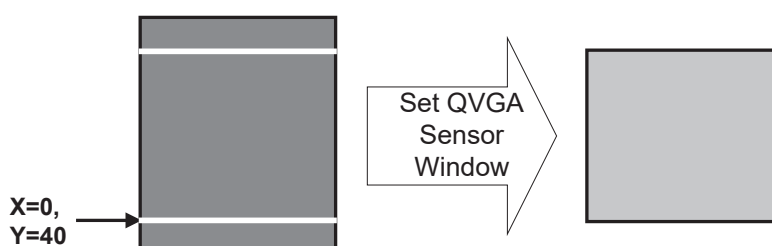


Figure 3.2: QVGA resolution pixel readout

3.3 Monochrome QVGA using pixel binning

QQVGA do not support the Bayer sensor version and only for the monochrome sensor version, 2 x 2 binning can be enabled to average 4 pixels in to 1 pixel which reduces resolution by a factor of four to QVGA, and improves S/N ratio.

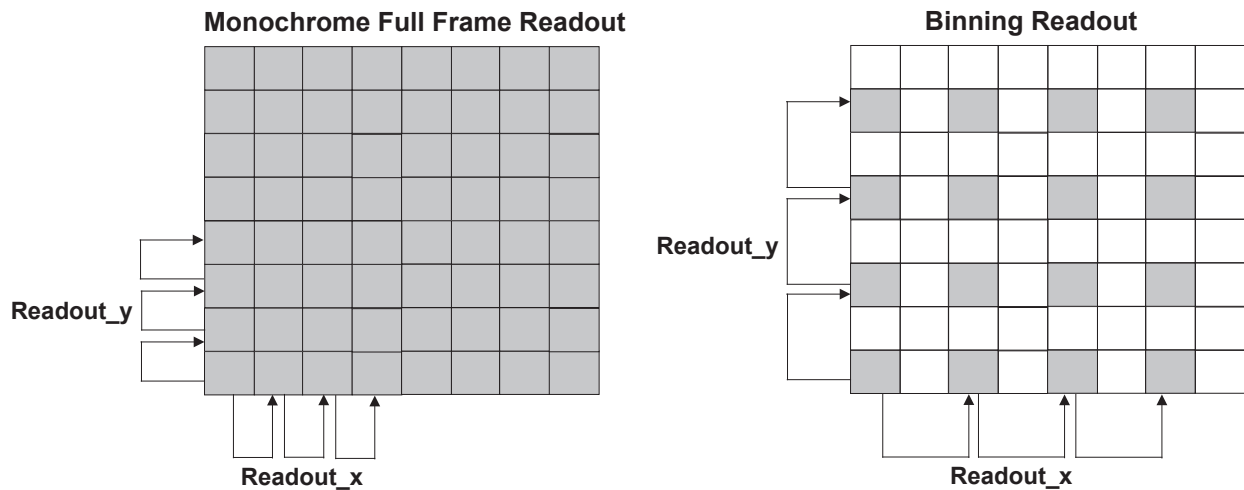


Figure 3.3: Monochrome full frame and binning readout mode

3.4 Horizontal and vertical mirror

The sensor readout can be mirrored in the vertical and / or horizontal direction where the window center will remain unchanged. The horizontal and vertical mirror readout can be applied in Full, QVGA, and binning mode.

In the color sensor version, the color of the first pixel read out will change according to the selected mirror mode as shown in the figure below.

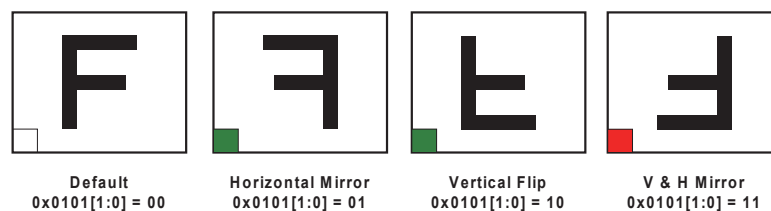


Figure 3.4: Horizontal and vertical mirror readout modes

4. Image Signal Processor Functional Description

The sensor ISP features can be configured by the host through the serial register interface. Please contact Himax Imaging for application notes and information.

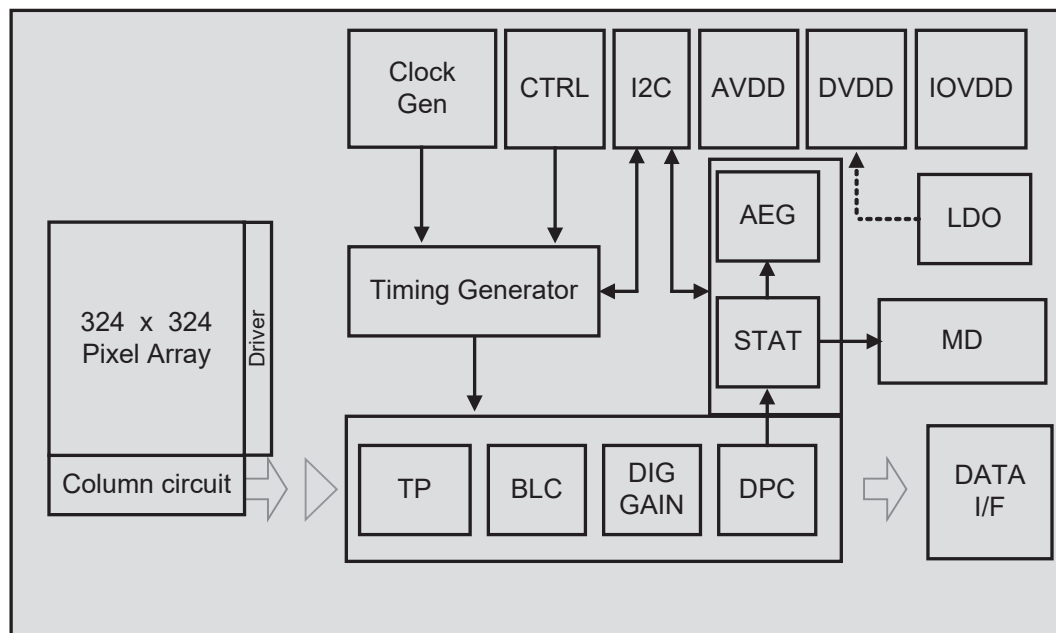


Figure 4.1: ISP blocks

Block acronym	Block name	Description	Register range	Register enable bit
TP	Test Pattern	Two test patterns are supported (See figure below): a. Walking 1's b. Color bar	0x0601	0x0601[0]
BLC	Black Level Correction	Adjusts the black level of the frame to the target programmed value based on optical black pixel data	0x1003 0x1007	0x1000[0] 0x1006[0]
DIG GAIN	Digital Gain	Global digital gain applied to the video data. Programmed in 2.6 format (2-bit integer, 6-bit floating)	0x020E 0x020F	-
DPC	Defective Pixel Correction	Correct single hot and cold pixel using neighboring "good" pixel data. Selectable for monochrome and Bayer.	0x100B 0x100C	0x1008[2:0]
STAT_MD	Statistics	6 or 8-bit average motion statistics for programmable window	0x2011 ~ 0x2018	0x2000[2:1]
AEG	Automatic Exposure Gain	Control loop which adjusts the sensor exposure, analog and digital gain to the user-defined target luminance value. The AEG can be programmed to avoid 50Hz and 60Hz flicker.	0x2101 ~ 0x2113	0x2100[0]
MD	Motion Detection	Detect for presence of motion within programmable Motion Region of Interest (separate statistics from AEC). The status of the motion detection, including triggered interrupt can be accessed through the registers.	0x2153 ~ 0x215B	0x2150[0]

Table 4.1: Digital ISP block

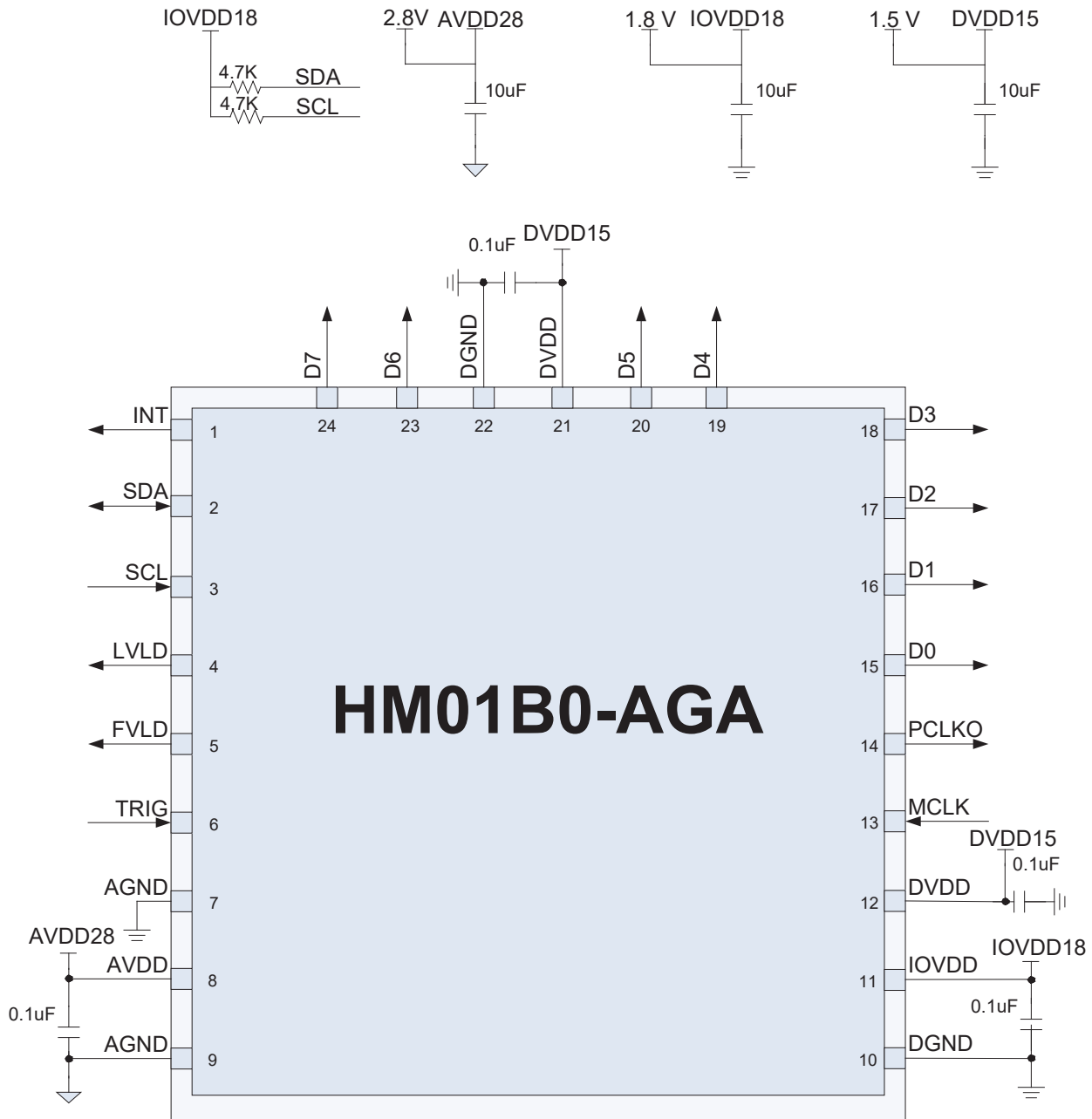


Figure 4.2: Test image patterns

5. Typical Application Circuit

5.1 Triple supply

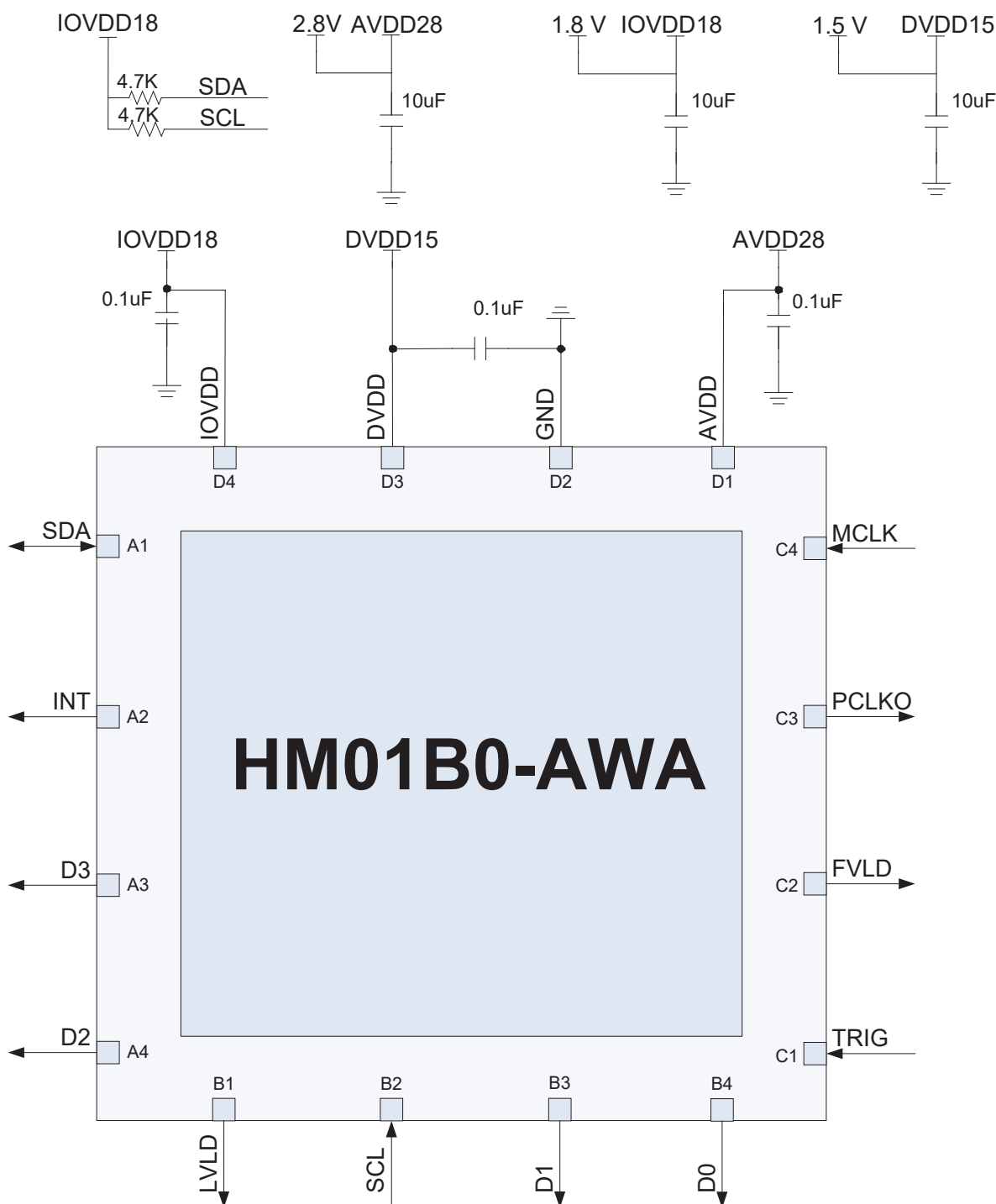
5.1.1 External LDO mode (Bare die)



- Note:** (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) 4-bit data format will output data on D0 ~ D3.
 (3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
 (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.1: Triple supply (2.8V / 1.8V / 1.5V) application circuit for bare die

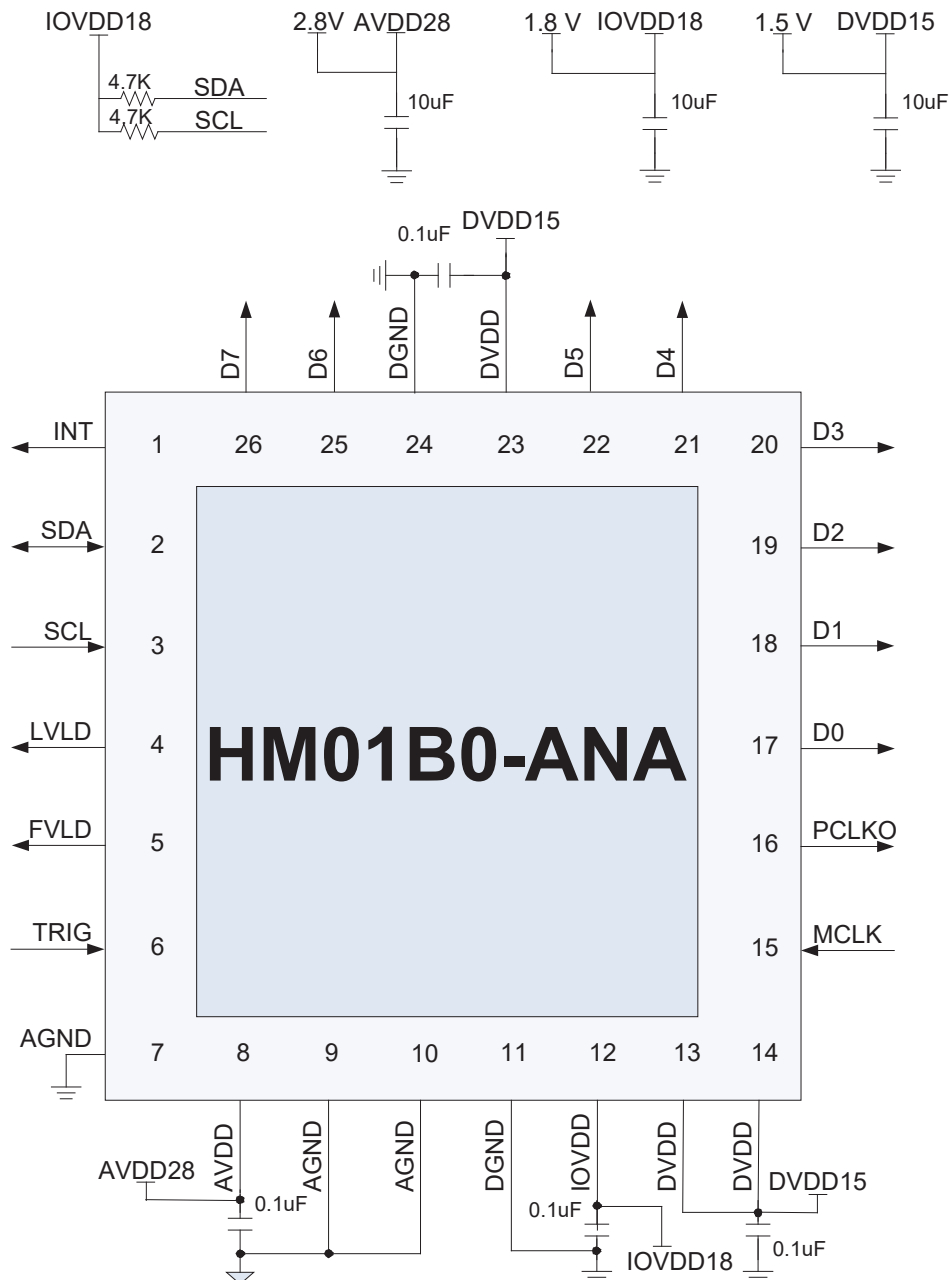
5.1.2 External LDO mode (CSP)



Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.

Figure 5.2: Triple supply (2.8V / 1.8V / 1.5V) application circuit for CSP

5.1.3 External LDO mode (NeoPAC)

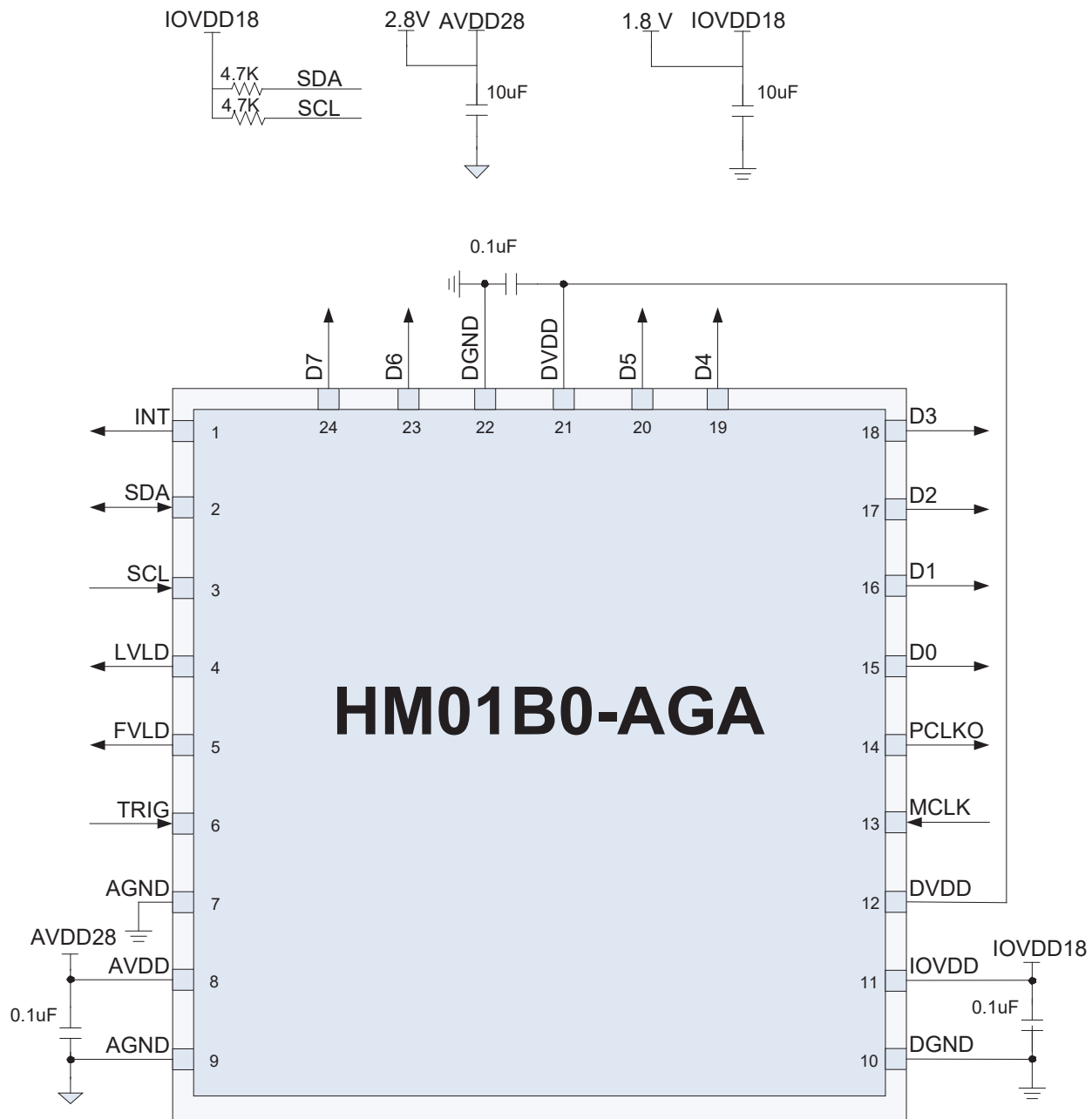


- Note:**
- (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 - (2) 4-bit data format will output data on D0 ~ D3.
 - (3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
 - (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.3: Triple supply (2.8V / 1.8V / 1.5V) application circuit for NeoPAC

5.2 Dual supply

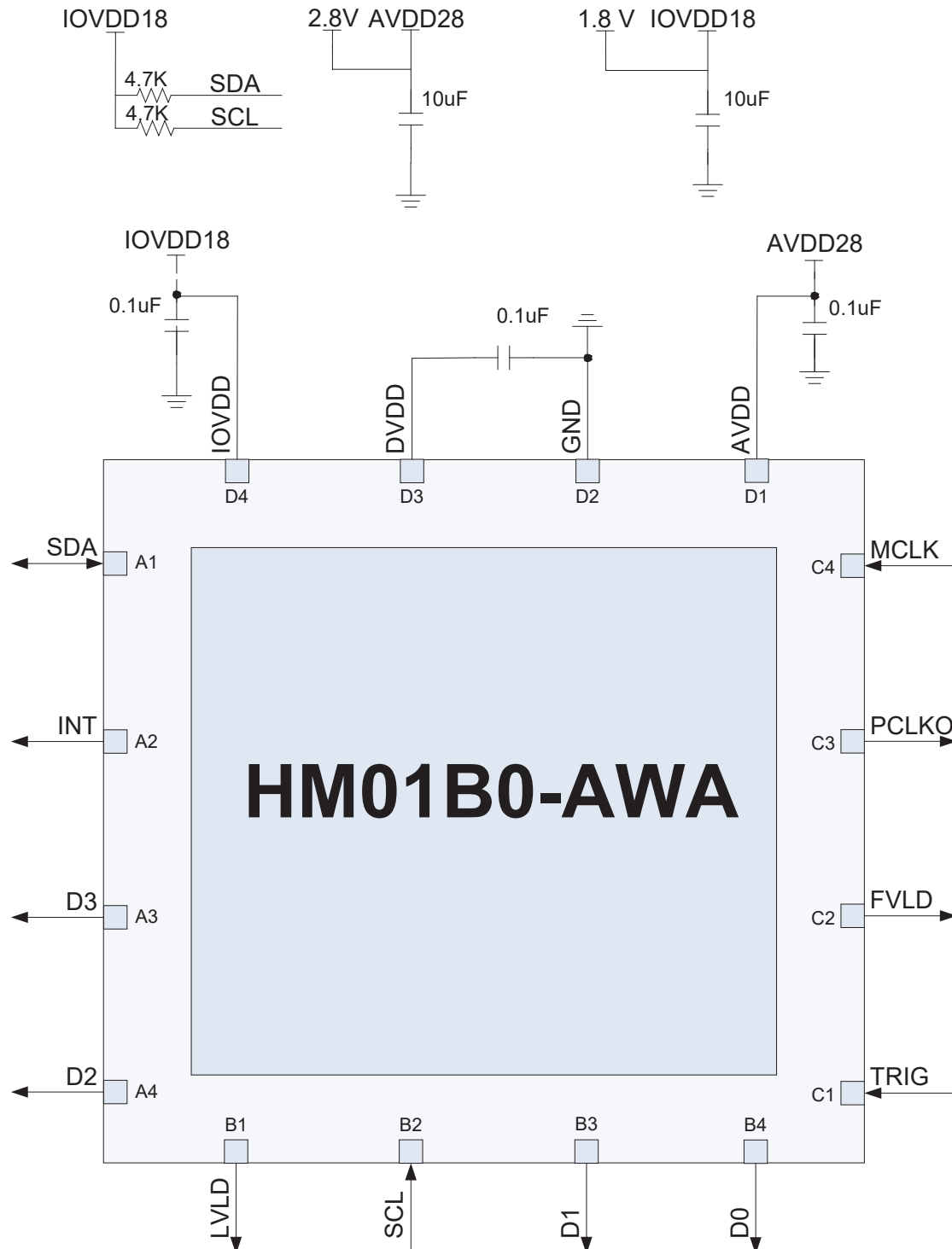
5.2.1 2.8V / 1.8V dual supply mode (Bare die)



- Note:** (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) 4-bit data format will output data on D0 ~ D3.
 (3) Pull-up resistor of 4.7k Ω to correct I/O voltage is recommended for SDA / SCL.
 (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.4: Dual supply (2.8V / 1.8V) application circuit for bare die

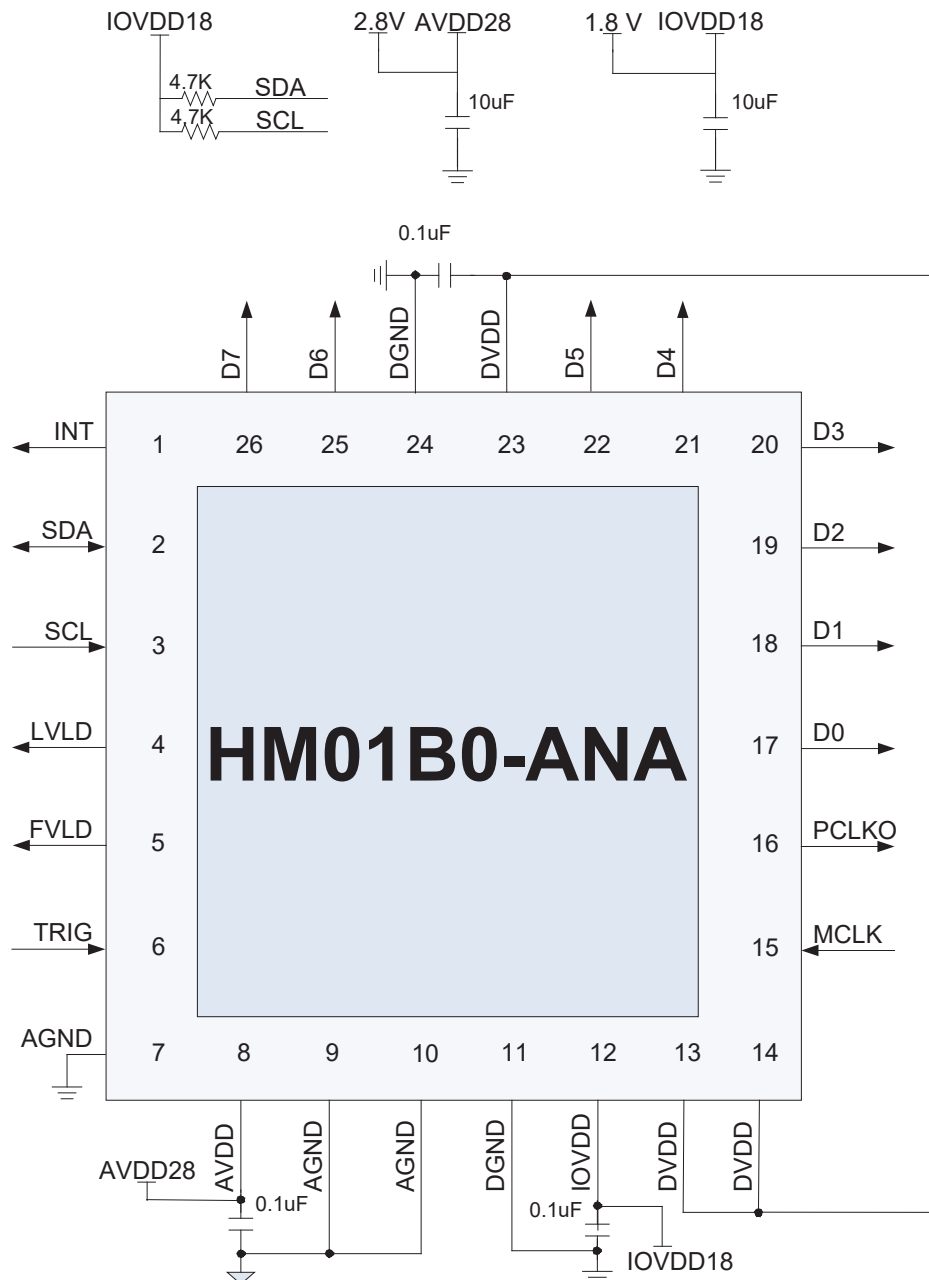
5.2.2 2.8V / 1.8V dual supply mode (CSP)



Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) Pull-up resistor of 4.7k Ω to correct I/O voltage is recommended for SDA / SCL.

Figure 5.5: Dual supply (2.8V / 1.8V) application circuit for CSP

5.2.3 2.8V / 1.8V dual supply mode (NeoPAC)

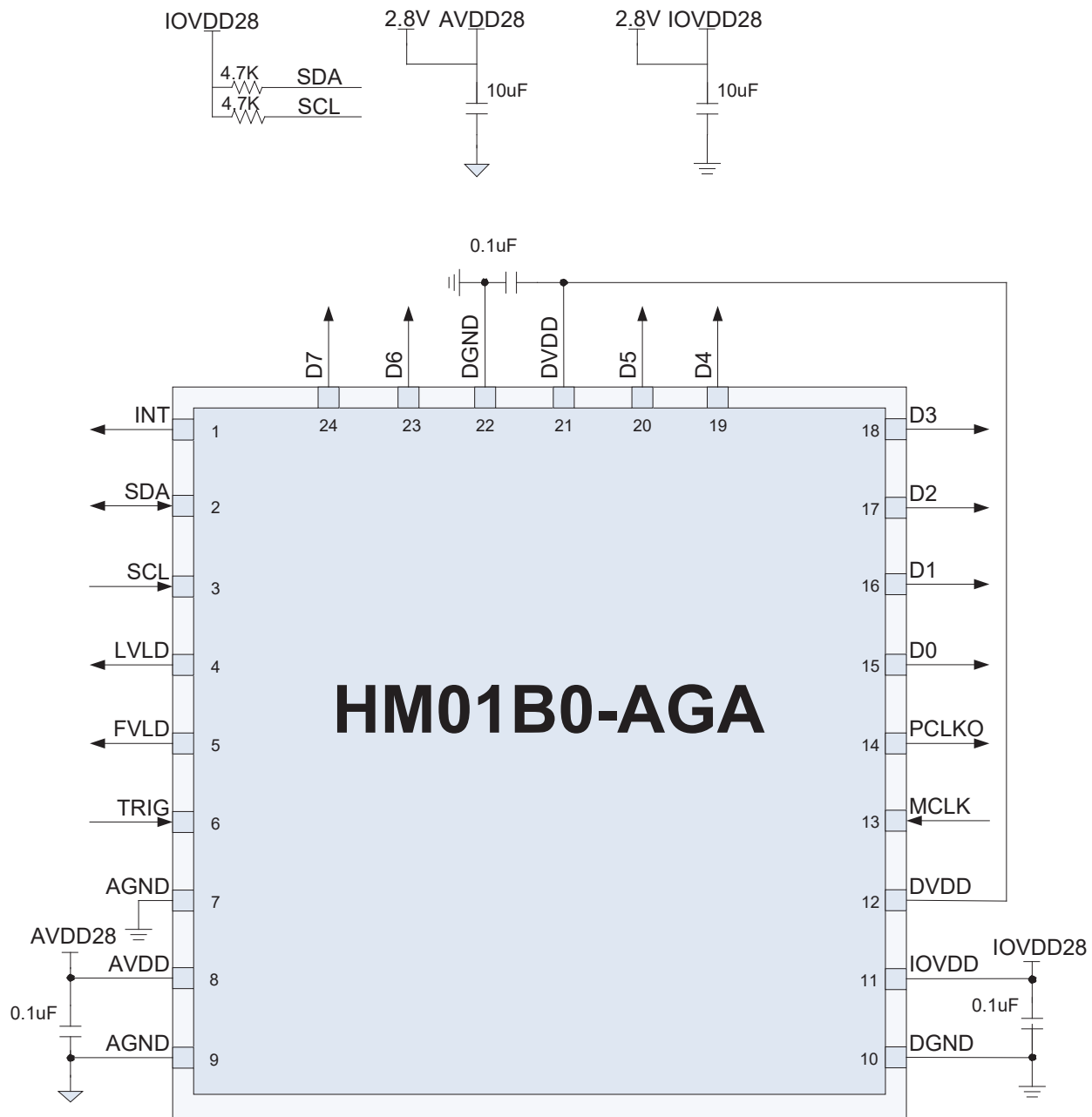


- Note:** (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) 4-bit data format will output data on D0 ~ D3.
 (3) Pull-up resistor of 4.7k Ω to correct I/O voltage is recommended for SDA / SCL.
 (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.6: Dual supply (2.8V / 1.8V) application circuit for NeoPAC

5.3 Single supply

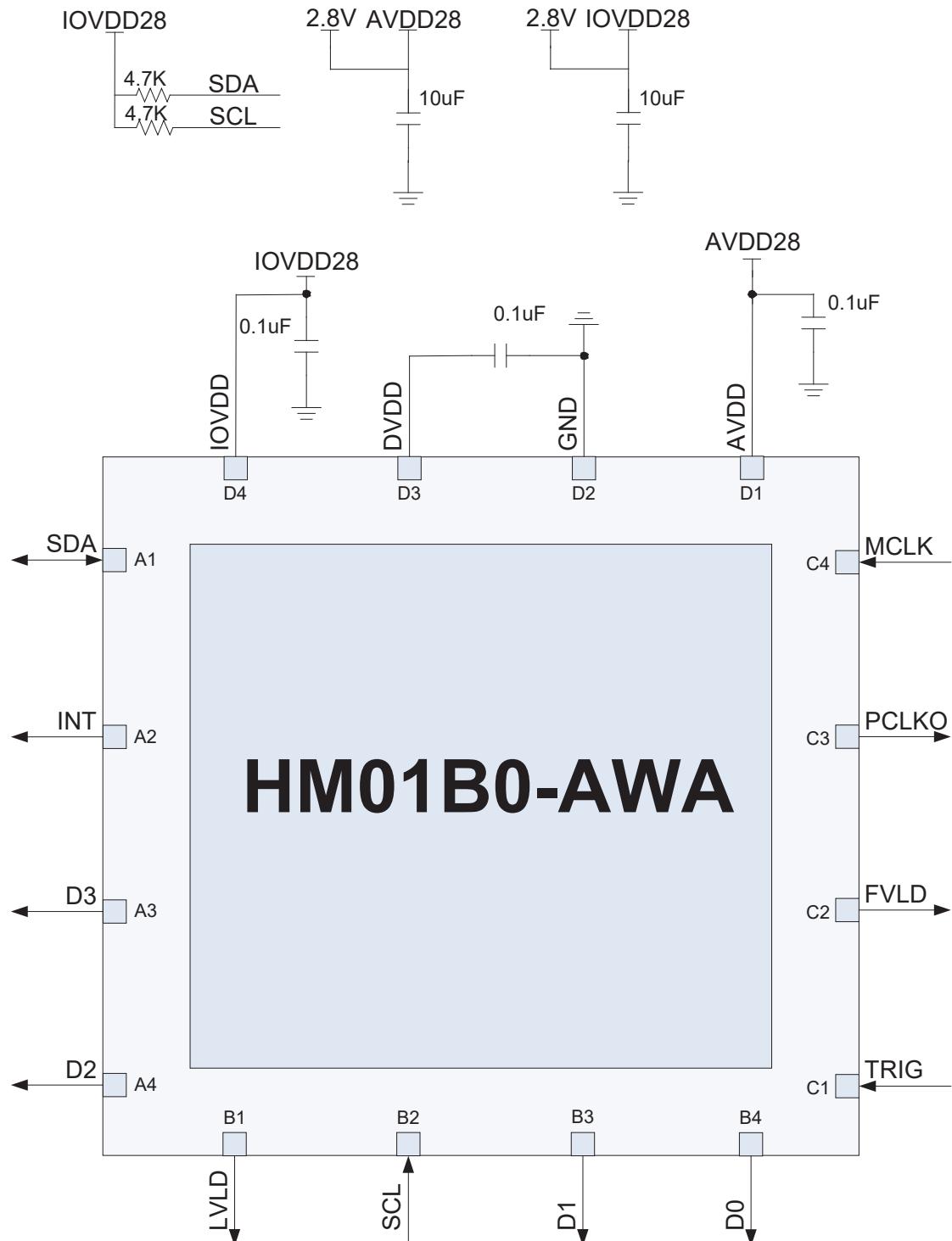
5.3.1 2.8V signal supply mode (Bare die)



- Note:** (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) 4-bit data format will output data on D0 ~ D3.
 (3) Pull-up resistor of 4.7k Ω to correct I/O voltage is recommended for SDA / SCL.
 (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.7: Single supply 2.8V application circuit for bare die

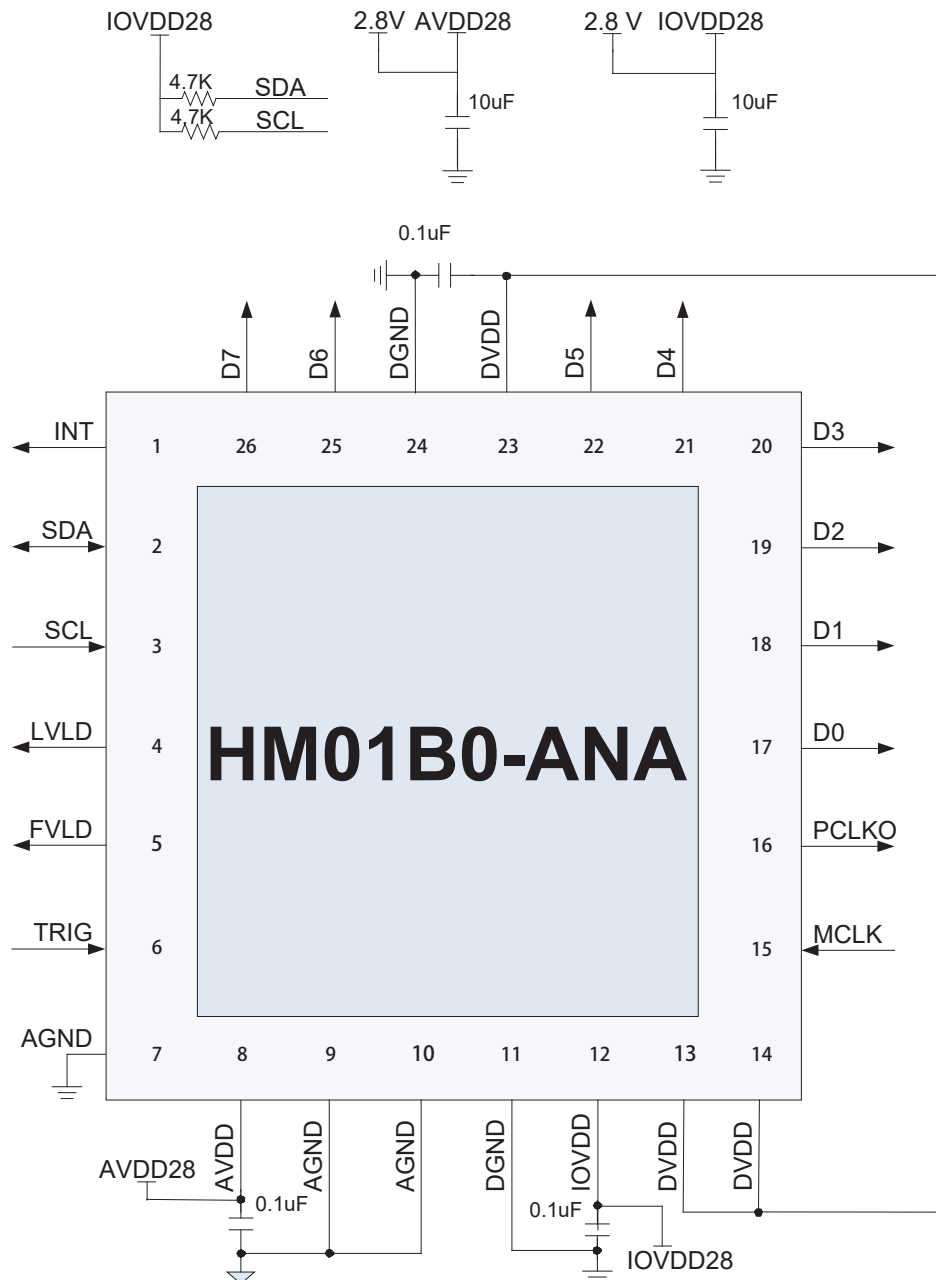
5.3.2 2.8V signal supply Mode (CSP)



Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) Pull-up resistor of 4.7k Ω to correct I/O voltage is recommended for SDA / SCL.

Figure 5.8: Single supply 2.8V application circuit for CSP

5.3.3 2.8V signal supply Mode (NeoPAC)



- Note:** (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
 (2) 4-bit data format will output data on D0 ~ D3.
 (3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
 (4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.9: Single supply 2.8V application circuit for NeoPAC

6. System Level Description

6.1 Operating modes

The HM01B0 supports five modes of operation as shown in the table below.

Mode	Description	Power	Register values	I2C	CLOCK	Digital
Power off	No power supplied to sensor	Off	-	-	-	-
S/W standby	Low-power consumption, no video	On	Retained	On	On or Off	Standby mode
Streaming 1	Mode_select [2:0]=001 I2C triggered streaming enable	On	Retained	On	On	On
Streaming 2	Mode_select [2:0]=011 I2C triggered frame; output register programmed number of frames(0x3020[7:0]), then enters s/w standby and clears Mode_select register bit to 000	On	Retained	On	On	On
Streaming 3	Mode_select [2:0]=101 Digital input pin (TRIG) frame trigger	On	Retained	On	On	On

Table 6.1: Operating modes

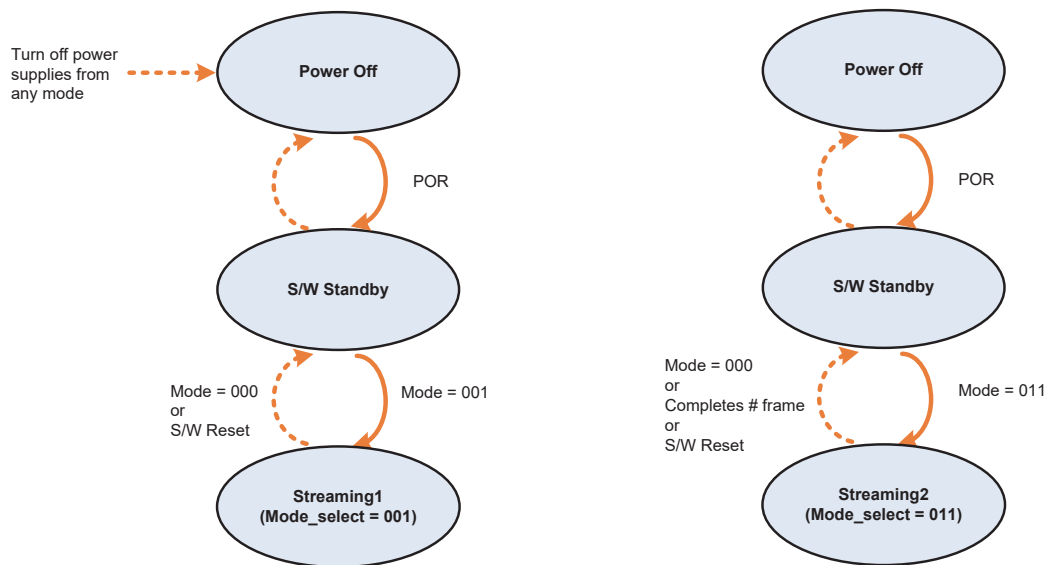


Figure 6.1: State diagram (I2C trigger)

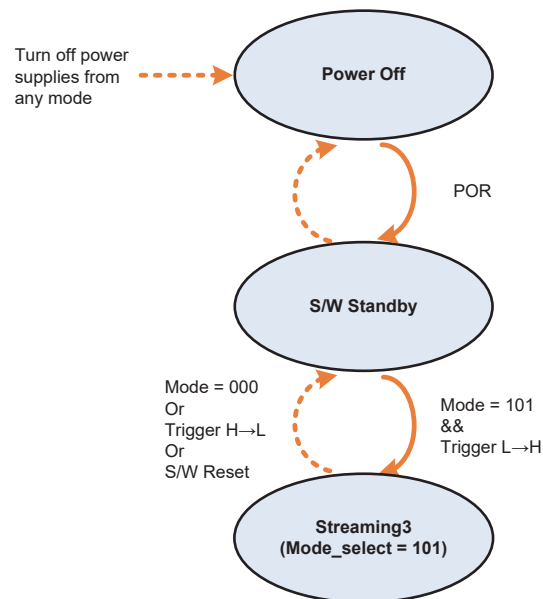


Figure 6.2: State diagram (Hardware pin trigger)

The HM01B0 supports hardware trigger mode. The user can control the sensor to stream on/off by setting “TRIG” pin high/low. This operating mode can also be used to synchronize multiple HM01B0 sensors if all the sensors have a common master clock input (MCLK). The parallel interfaces of all the sensors are exactly synchronized and the user can use the pixel clock of one sensor to latch other’s sensor data.

Output Format	Mode	MCLK (MHz)	Sensor_Core (MHz)	Sensor_Register (MHz)	PCLKO (MHz)	Maximum FPS
8-bit	SYNC	3-24	MCLK/2,4	MCLK	Sensor_Core	60
	Non-SYNC	3-36	MCLK/2,4,8	MCLK/1,2,4,8	Sensor_Core	60
4-bit	SYNC	3-24	MCLK/2,4	MCLK	2x Sensor_Core	60
	Non-SYNC	3-36	MCLK/2,4,8	MCLK/1,2,4,8	2x Sensor_Core	60
1-bit	SYNC	3-36	MCLK/8	MCLK	MCLK	45
	Non-SYNC	3-36	MCLK/8	MCLK/1,2,4,8	MCLK	45

Table 6.2: MCLK configuration for SYNC and non-SYNC mode

6.2 Reset

The HM01B0 provides two methods of reset methods: Power On Reset (POR) and software reset.

During power up, an internal POR circuit applies a system reset until the DVDD supply reaches a monitored voltage threshold. This insures that the supply voltage is stable and the sensor is properly initialized.

Software reset is applied by writing register value 0 or 1 to register bit SW_RESET[0] (0x0103[0]). When reset is applied, the sensor will return to “Standby Mode” and reset all serial interface registers to its default values.

6.3 Power up sequence

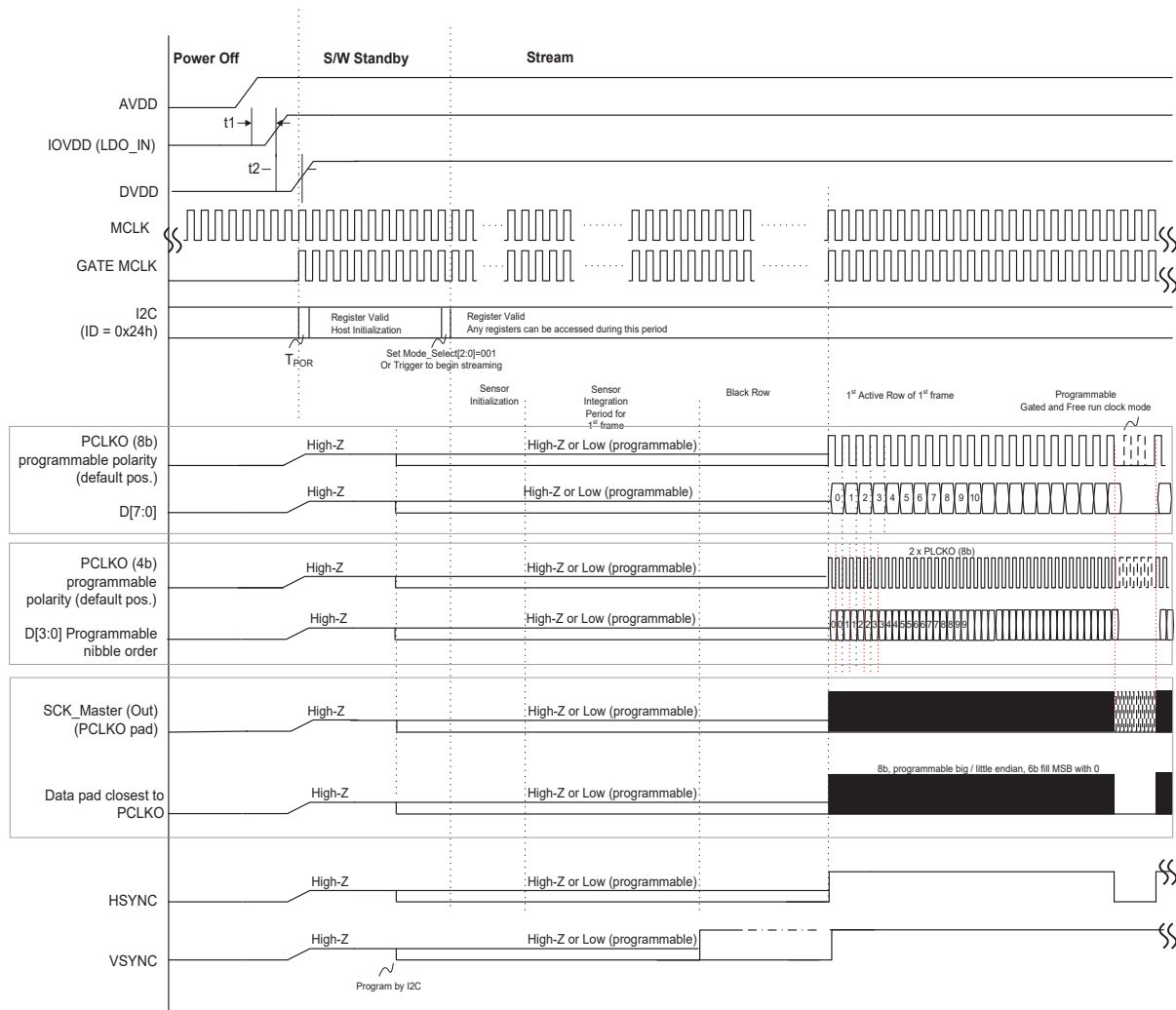


Figure 6.3: Power up sequence

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
t1	AVDD to IOVDD	0	-	∞	sec.
t2	IOVDD to DVDD	0	-	∞	sec.
t _{POR}	Power On Reset time	50	-	-	µsec

Table 6.3: Power up sequence timing

6.4 Clock setup

Reference clock to the sensor can be provided externally through the MCLK pin, or generated by the on-chip self-oscillator. The sensor will automatically select the self-oscillator when the reference clock is not present at the MCLK pin.

- The self-oscillator is only use for motion detection and don't care that much on flicker.
- The frequency for Sensor_Core and Sensor_Register are $1/8 \times \text{MCLK}$ in self-oscillator mode.

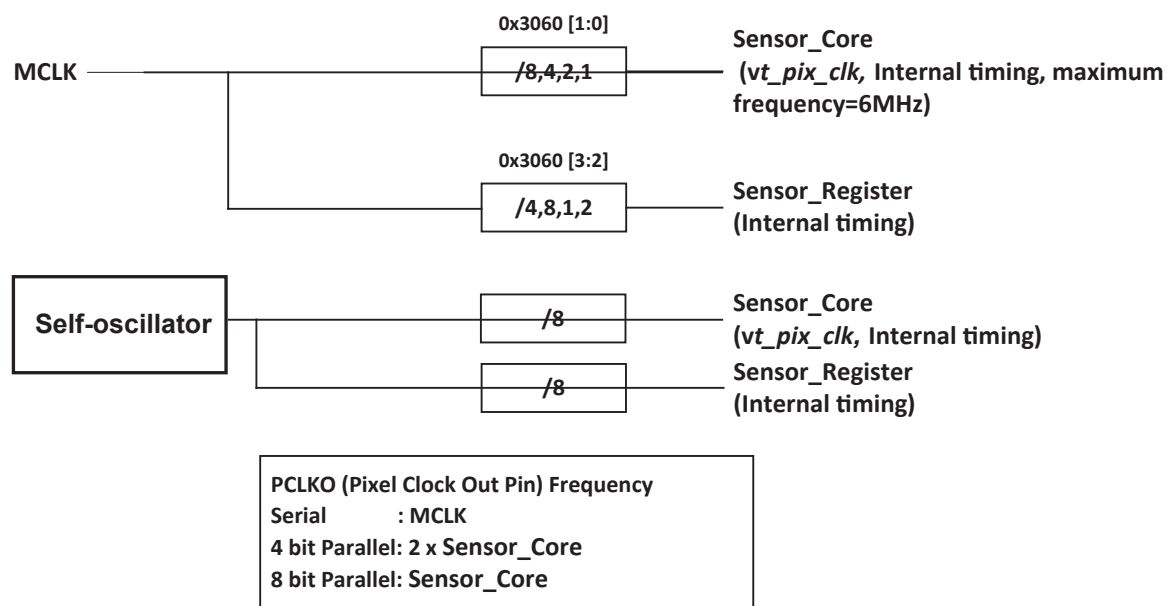


Figure 6.4: Clock dividers

6.4.1 MCLK and self-oscillator mode switch

- The Register 0x3067[0] set to 1 before MCLK off for MCLK mode to self oscillator mode.
- The Register 0x3067[0] set to 0 before self oscillator mode off for self oscillator mode to MCLK mode.

6.5 IO control options

Options for IO pins can be programmed based on the following table. Please consult Himax Imaging FAE for additional information.

Output pin	Drive strength control	Polarity	Interface bit width	Sync advance	MSB / LSB	PCLKO clock gating
D[7:4]	-	-	0x3059[6:5] 00=8-bit 10=4-bit 01=1-bit	-	0x3060[4] ⁽¹⁾ 0=MSB 1=LSB	-
D[3:1]	0x3063[2:0]	-		-		-
D[0]	0x3062[6:4]	-		-		-
LVLD	-	-	-	0x3023 [4:0] 0 ~ 20 PCLK	-	-
FVLD	-	-	-	0x3022 [3:0] 0 ~ 12 Row	-	-
PCLKO	0x3062[2:0]	0x3068[0] 0: Rising edge 1: Falling edge	-	-	-	0x3060[5] 0: Non-gated 1: Gated clk
INT	-	-	-	-	-	-

Note: (1) 1-bit / 4-bit data mode only.

Table 6.4: IO control options

The status for output pins in standby/streaming mode can be control by register 0x3065[1:0]

Register 0x3065 [1:0]	Pin	Standby mode	Streaming mode
0	Output pins	Hi-z	Driving
	INT	Hi-z	Driving
1	Output pins	Driving	Driving
	INT	Driving	Driving
2	Output pins	Hi-z	Hi-z
	INT	Hi-z	Driving
3	Output pins	Hi-z	Hi-z
	INT	Driving	Driving

Table 6.5: Output pin status

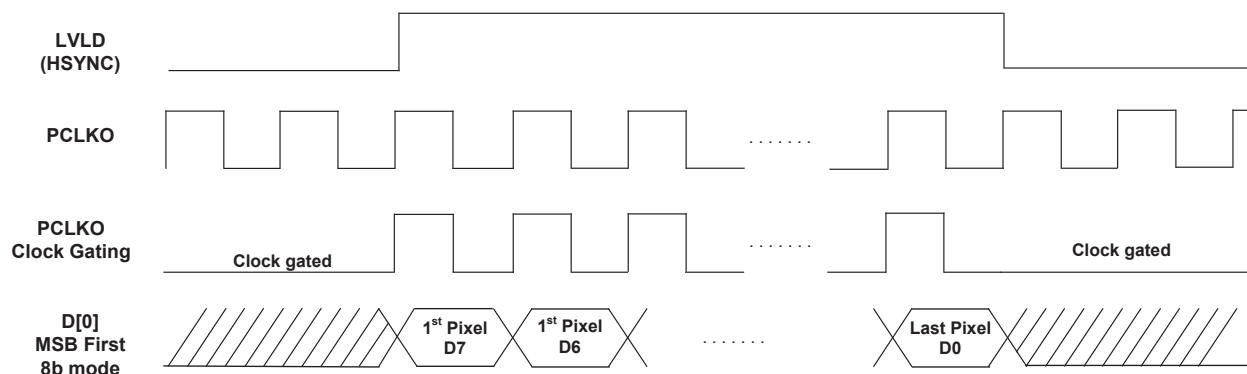


Figure 6.5: Non-gated and gated serial data clock option

6.6 Data format control

Output data bit	Mode of operation	0x3059[6] 4bit_en	0x3059[5] serial_en	0x3060[5] gated_en	0x3060[4] msb_en
8	Non-gated	0	0	0	0
8	Gated	0	0	1	0
4	Non-gated; LSB	1	0	0	0
	Non-gated; MSB	1	0	0	1
	Gated; LSB	1	0	1	0
	Gated; MSB	1	0	1	1
1	Non-gated; LSB	0	1	0	0
	Non-gated; MSB	0	1	0	1
	Gated; LSB	0	1	1	0
	Gated; MSB	0	1	1	1

Table 6.6: Data format control setting summary

The HM01B0 supports RAW8 and RAW6 data format. The default is 8-bit data format, and 6bit data format is selected by setting register bit DATAFORMAT 0x3011 [0] = 1.

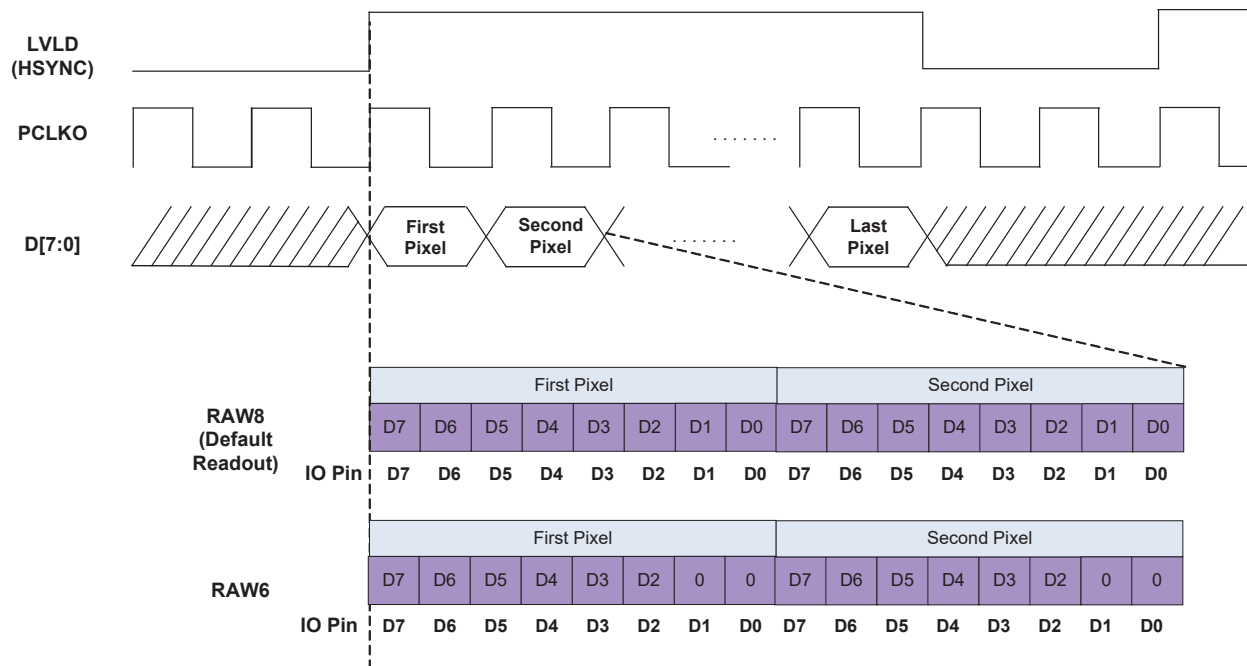


Figure 6.6: 6-bit and 8-bit RAW output format on 8-bit data IO interface

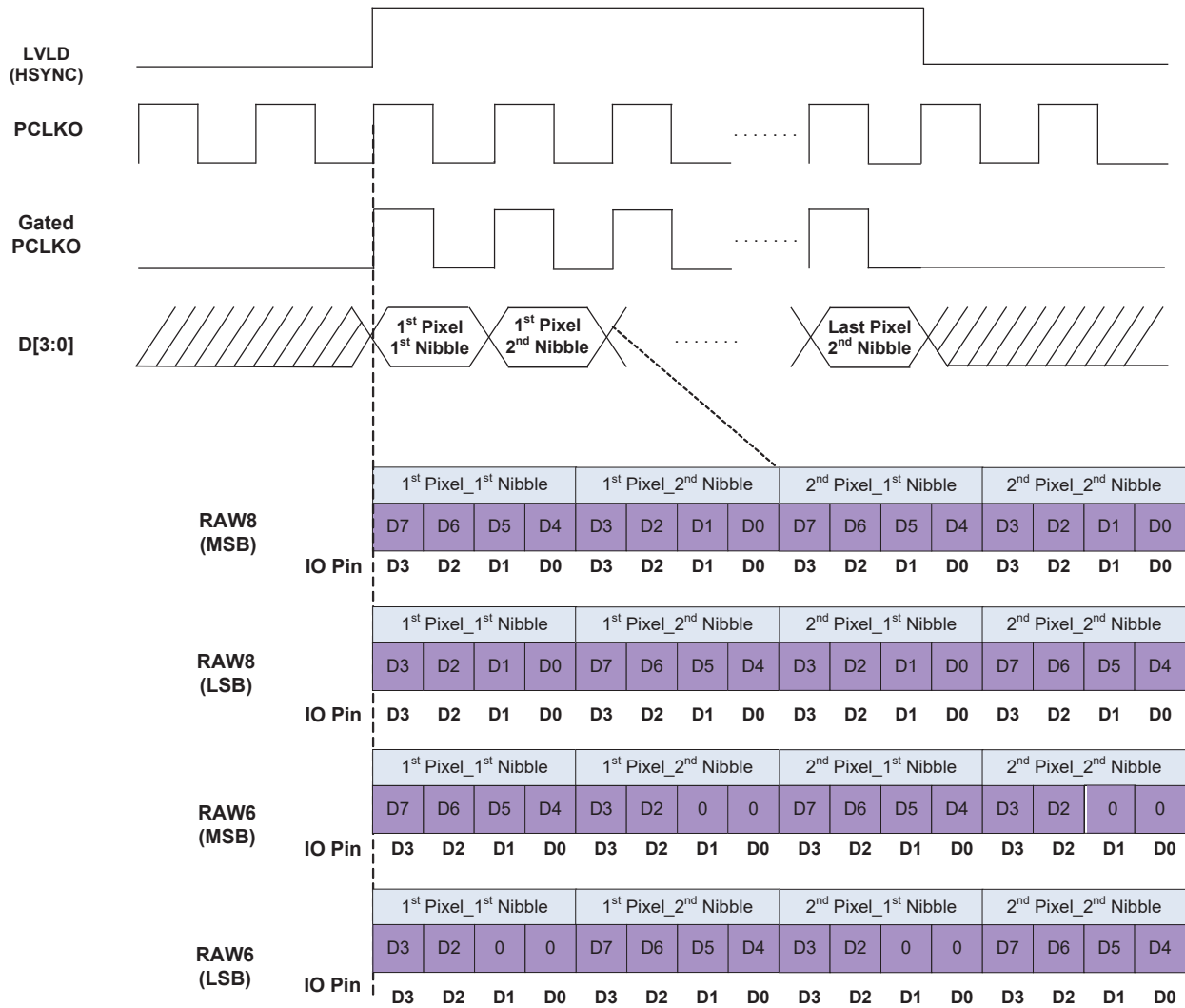


Figure 6.7: 6-bit and 8-bit RAW output format on 4-bit data IO interface

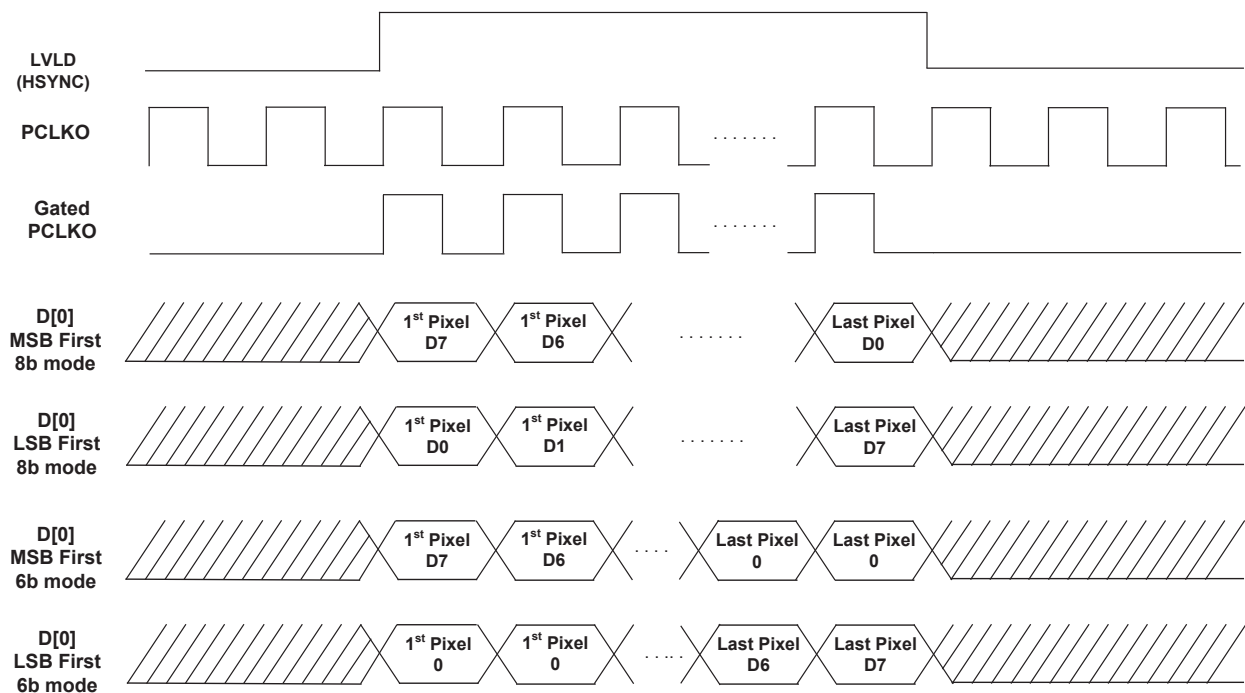


Figure 6.8: RAW output format on serial data IO interface

7. Serial Interface Description

The 2-wire serial interface provides read/write access to the sensor registers

- 2-wire serial interface consists of SDA (**Bidirectional serial data**) and SCL (**Serial clock**) pins.
- HM01B0 uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

7.1 I2C slave address ID

- The address of the sensor is 0x24.
- The address of the sensor can be changed by register 0x3401[6:0] when register 0x3400[0] set to 1. The address of the sensor get restored back to default (0x24) after rebooting.

7.2 Start / Stop conditions

The start and stop conditions on the serial bus is issued by the Host.

SDA Transition	SCL	Condition
High to Low	High	Start
Low to High	High	Stop

Table 7.1: Serial interface start and stop transition

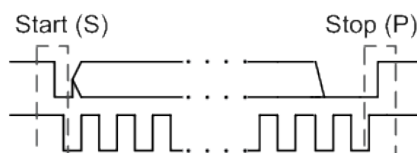


Figure 7.1: 2-wire serial interface start and stop condition

7.3 Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL is High. The SDA signal can transition when SCL is Low.

7.4 Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an acknowledgement (**ACK**) or a no-acknowledgement bit (**No ACK**).

7.5 Acknowledge / No acknowledgement

Each 8-bit is followed by an Acknowledge (ACK) or No-Acknowledge (No ACK) bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin (Pulled high). The No-Ack bit is used to terminate a read sequence.

7.6 Write sequence

The write sequence is initiated by the Host with Start (S) condition, followed by 8-bit device slave ID (write ID)

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address (high byte first, then low byte), then the register data. After each byte, the sensor will issue an ACK or NO ACK signal.
- The write operation is completed when the Host asserts a stop condition

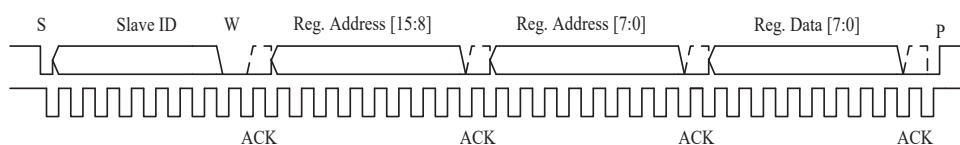


Figure 7.2: 2-wire serial interface 16-bit address write

7.7 Read sequence

The read sequence is initiated by Host with Start (S) condition, followed by the 8-bit device slave ID (write ID).

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address (high byte first, then low byte), then the register data. After each byte, the sensor will issue an ACK or NO ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID (Read ID).
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

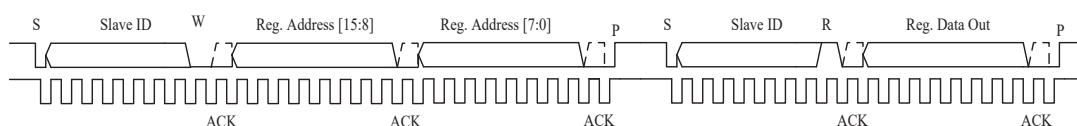


Figure 7.3: 2-wire serial interface 16-bit address read

8. Sensor Core Control

8.1 Frame retiming

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of the frame boundary. In the Register Table section of this document, the registers that require retiming, such as gain and integration (**exposure**), are indicated by the designator **CMU (Command Update)**.

Changes to retimed registers take effect at the boundary of the second subsequent frame (**N+2**) as shown in the figure below. When the register 0x3035 [7] is set to 1, both analogy and digital gain can be applied at frame N+1 if no other CMU register settings are updated within the same retiming cycle.

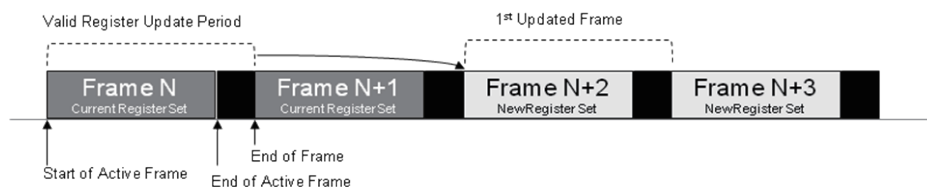


Figure 8.1: (N+2) command update (CMU) timing

8.2 Analog gain control

Analog gain follows the equation 2^N where N is set by ANALOG_GLOBAL_GAIN 0x0205 [6:4]. The valid programmable values for the analog gain register are defined in table below.

Code (hex)	Gain (x)	Gain (dB)
0x00	1	0
0x10	2	6
0x20	4	12
0x30	8	18

Table 8.1: Global analog gain settings

8.3 Suggestion for analog gain and digital gain

- Analogy gain x digital gain $\leq 16x$ for machine version
- Analogy gain x digital gain $\leq 8x$ for human version

8.4 Exposure control

The HM01B0 supports coarse integration control with a programmable resolution of 1 row. The minimum integration time is 2 rows. The exposure time of the sensor is calculated using the following equation:

- A. $\text{Integration time (seconds)} = \text{coarse_integration} \times \text{line_length_pck} / \text{vt_pix_clk (MHz)} \times 1 \times 10^6$
- B. $\text{Coarse_integration_time} \leq (\text{frame_length_lines} - 2)$

8.4.1 50Hz / 60Hz flicker avoidance

To avoid flicker, the sensor exposure time should be set in intervals of 1/100 seconds or 1/120 seconds for 50Hz or 60Hz flicker avoidance, respectively.

- A. $\text{Integration Step Size (60Hz Avoidance)} = \text{vt_pix_clk (MHz)} \times 1 \times 10^6 / \text{line_length_pck} / 120$
- B. $\text{Integration Step Size (50Hz Avoidance)} = \text{vt_pix_clk (MHz)} \times 1 \times 10^6 / \text{line_length_pck} / 100$

8.5 Frame rate control

The frame rate of the sensor is calculated based on the Video Timing Clock and uses the following equations:

- A. $65535 \geq \text{line_length_pck} \geq \text{min_line_length_pck}$
- B. $65535 \geq \text{frame_length_lines} \geq \text{min_frame_length_lines}$
- C. $\text{frame rate} = \text{vt_pix_clk (MHz)} \times 1 \times 10^6 / (\text{frame_length_lines} \times \text{line_length_pck})$

Minimum value	Full frame	QVGA	QQVGA
min_line_length_pck	0x0178	0x0178	0x00D7
min_frame_length_lines	0x0158	0x0104	0x0080

Table 8.2: Constraint for line length and frame length

9. Register Table

9.1 Sensor ID

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0000	[7:0]	MODEL_ID_H [15:8]	RO	16-bit sensor Part number (HM01B0)	-	0x01
0x0001	[7:0]	MODEL_ID_L [7:0]			-	0xB0
0x0002	[7:0]	SILICON_REV	RO	Silicon Revision Number	-	-
0x0005	[7:0]	FRAME_COUNT	RO	Frame counter	-	0xFF
0x0006	[7:0]	PIXEL_ORDER	RO	[1:0] Color Sensor Pixel Order 0 – GR 1 – RG 2 – BG 3 – GB	-	0x02

9.2 Sensor mode control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0100	[2:0]	MODE_SELECT	RW	[2:0] Sensor mode selection 000: Standby 001: Streaming 011: Streaming 2 (Output N frames) 101: Streaming 3 (Hardware Trigger)	-	0x00
0x0101	[1:0]	IMAGE_ORIENTATION	RW	Image Orientation [0]:Horizontal Mirror En [1]:Vertical Flip Enable	Y	0x00
0x0103	[0]	SW_RESET	W	software reset	-	0xFF
0x0104	[0]	GRP_PARAM_HOLD	W	Group parameter hold 0 – consume 1 – hold	-	0xFF

9.3 Sensor exposure gain control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0202	[7:0]	INTEGRATION_H [15:8]	RW	Coarse integration time in lines (16-bit UINT)	Y	0x01
0x0203	[7:0]	INTEGRATION_L [7:0]	RW		Y	0x08
0x0205	[6:4]	ANALOG_GAIN	RW	Analog Global Gain code (8-bit UINT)	Y	0x00
0x020E	[1:0]	DIGITAL_GAIN_H [9:8]	RW	Digital Global Gain code (8-bit UINT)	Y	0x01
0x020F	[7:2]	DIGITAL_GAIN_L [7:2]	RW		Y	0x00

9.4 Frame timing control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0340	[7:0]	FRAME_LENGTH_LINES_H [15:8]	RW	frame_length_lines (16-bit UINT)	Y	0x02
0x0341	[7:0]	FRAME_LENGTH_LINES_L [7:0]	RW		Y	0x32
0x0342	[7:0]	LINE_LENGTH_PCK_H [15:8]	RW	line_length_pck (16-bit UINT)	Y	0x01
0x0343	[7:0]	LINE_LENGTH_PCK_L [7:0]	RW		Y	0x72

9.5 Binning mode control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0381	[0]	Reserved	RW	Set to 1	Y	0x01
0x0383	[1:0]	Readout_x	RW	Read out for x [1:0] : 1 : full 3 : Horizontal BIN2 timing enable	Y	0x01
0x0385	[0]	Reserved	RW	Set to 1	Y	0x01
0x0387	[1:0]	Readout_y	RW	Readout for y [1:0] : 1 : full 3 : Vertical BIN2 timing enable	Y	0x01
0x0390	[1:0]	BINNING_MODE	RW	[0] Vertical Binning [1] Horizontal Binning	Y	0x00

9.6 Test pattern control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x0601	[7:0]	TEST_PATTERN_MODE	RW	Test Pattern Mode [0] : test pattern enable [4] : mode selection 0 : color bar 1 : walking 1	-	0x00

9.7 Black level control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x1000	[7:0]	BLC_CFG	RW	bic configuration [0] : bic en	-	0x01
0x1003	[7:0]	BLC_TGT	RW	Black level target 0-255	-	0x20
0x1006	[0]	BLI_EN	RW	BLI enable	-	0x00
0x1007	[7:0]	BLC2_TGT	RW	BLC2 target, set to the same level as BLC target	-	0x20

9.8 Sensor reserved

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x1008	[7:0]	DPC_CTRL	RW	DPC control [2:0] : DPC option 0: dpc off 1: option1- mono 3: option1- bayer 5: option2- bayer [3]: boundary bypass enable	-	0x00
0x100B	[7:0]	SINGLE_THR_HOT	RW	Single hot pixel threshold	-	0xFF
0x100C	[7:0]	SINGLE_THR_COLD	RW	Single cold pixel threshold	-	0xFF

9.9 VSYNC,HSYNC and pixel shift register

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x1012	[2:0]	VSYNC_HSYNC_PIXEL_SHIFT_EN	RW	Shifting enable [0]: vsync shift enable [1]: hsync shift enable [2]: pixel shift enable	-	0x07

9.10 Statistic control and read only

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x2000	[7:0]	STATISTIC_CTRL	RW	ROI statistic control [0] : AE stat en [1] : MD LROI stat en [2] : Set to 1 [4] : Ave. 8/16 frame select	-	0x07
0x2011	[0]	MD_LROI_X_START_H	RW	motion detection LROI (x start High Byte)	-	0x00
0x2012	[7:0]	MD_LROI_X_START_L	RW	motion detection LROI (x start Low Byte)	-	0x48
0x2013	[0]	MD_LROI_Y_START_H	RW	motion detection LROI (y start High Byte)	-	0x00
0x2014	[7:0]	MD_LROI_Y_START_L	RW	motion detection LROI (y start Low Byte)	-	0x70
0x2015	[0]	MD_LROI_X_END_H	RW	motion detection LROI (x end High Byte)	-	0x00
0x2016	[7:0]	MD_LROI_X_END_L	RW	motion detection LROI (x end Low Byte)	-	0xDB
0x2017	[0]	MD_LROI_X_END_H	RW	motion detection LROI (y end High Byte)	-	0x00
0x2018	[7:0]	MD_LROI_X_END_L	RW	motion detection LROI (y end Low Byte)	-	0xB3

9.11 Automatic exposure gain control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x2100	[7:0]	AE_CTRL	RW	AE Control loop enable [0] : AE en	-	0x01
0x2101	[7:0]	AE_TARGET_MEAN	RW	AE target mean	-	0x3C
0x2102	[7:0]	AE_MIN_MEAN	RW	AE min mean	-	0x0A
0x2103	[7:0]	CONVERGE_IN_TH	RW	Converge in threshold	-	0x03
0x2104	[7:0]	CONVERGE_OUT_T H	RW	Converge out threshold	-	0x05
0x2105	[7:0]	MAX_INTG_H	RW	Maximum INTG High Byte	-	0x01
0x2106	[7:0]	MAX_INTG_L	RW	Maximum INTG Low Byte	-	0x54
0x2107	[7:0]	MIN_INTG	RW	Minimum INTG	-	0x02
0x2108	[7:0]	MAX_AGAIN_FULL	RW	Maximum Analog gain in full frame mode	-	0x03
0x2109	[7:0]	MAX_AGAIN_BIN2	RW	Maximum Analog gain in bin2 mode	-	0x04
0x210A	[7:0]	MIN_AGAIN	RW	Minimum Again	-	0x00
0x210B	[7:0]	MAX_DGAIN	RW	Maximum Dgain	-	0xC0
0x210C	[7:0]	MIN_DGAIN	RW	Minimum Dgain	-	0x40
0x210D	[7:0]	DAMPING_FACTOR	RW	Damping factor	-	0x20
0x210E	[7:0]	FS_CTRL	RW	Flicker Step control [0] : FS en [1] : frequency selection 0 : 50Hz 1 : 60Hz	-	0x03
0x210F	[7:0]	FS_60HZ_H	RW	Flicker Step 60Hz parameter High Byte	-	0x00
0x2110	[7:0]	FS_60HZ_L	RW	Flicker Step 60Hz parameter Low Byte	-	0x3C
0x2111	[7:0]	FS_50HZ_H	RW	Flicker Step 50Hz parameter High Byte	-	0x00
0x2112	[7:0]	FS_50HZ_L	RW	Flicker Step 50Hz parameter Low Byte	-	0x32
0x2113	[7:0]	FS_HYST_TH	RW	Flicker Step hysteresis threshold	-	0x66

9.12 Motion detection control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x2150	[7:0]	MD_CTRL	RW	Motion Detection control [0] : MD LROI en [1] : Set to 1	-	0x03
0x2153	[0]	I2C_CLEAR	W	I2c clear	-	0x00
0x2155	[7:0]	WMEAN_DIFF_TH_H	RW	wMean difference threshold H	-	0x7D
0x2156	[7:0]	WMEAN_DIFF_TH_M	RW	wMean difference threshold M	-	0x4B
0x2157	[7:0]	WMEAN_DIFF_TH_L	RW	wMean difference threshold L	-	0x05
0x2158	[7:0]	MD_THH	RW	MD threshold H	-	0x80
0x2159	[7:0]	MD_THM1	RW	MD threshold M1	-	0x32
0x215A	[7:0]	MD_THM2	RW	MD threshold M2	-	0x19
0x215B	[5:0]	MD_THL	RW	MD threshold L	-	0x03

9.13 Sensor timing control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x3010	[7:0]	QVGA_WIN_EN	RW	[0]: QVGA enable	Y	0x00
0x3011	[6:0]	SIX_BIT_MODE_EN	RW	[0] : 6 bit mode enable [6:4] : Reserved	-	0x70
0x3020	[7:0]	PMU_PROGRAMMABLE_FRAMECNT	RW	PMU AutoSleep Framecnt	-	0x00
0x3022	[4:0]	ADVANCE_VSYNC	RW	Advance VSYNC field from 0 to 20 (1LSB=1 Row period)	-	0x02
0x3023	[5:0]	ADVANCE_HSYNC	RW	Advance Hsync field from 0 to 20 (1LSB=1 Pixel Clock)	-	0x02
0x3035	[7]	EARLY_GAIN	RW	Applies gain in N+1 frame if Integration is not updated in the same CMU frame [7] : early_gain_en	-	0xF3

9.14 IO and clock control

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x3059	[7:0]	BIT_CONTROL	RW	Interface bit width control [4:0] : Reserved [5] : serial_en [6] : 4-bit enable	-	0x02
0x3060	[7:0]	OSC_CLK_DIV	RW	Clock divider, gating and LDO control [1:0] : vt_sys_div 00 : /8 01 : /4 10 : /2 11 : /1 [3:2] : vt_reg_div 00 : /4 01 : /8 10 : /1 11 : /2 [4] : msb_en [5] : gated_clk_en [6] : dvdd_ldo_en_d	-	0x0A
0x3061	[7:0]	ANA_Register_11	RW	[3:1]: ldo_stb_d [5]: main LDO power down enable	-	0x00
0x3062	[7:0]	IO_DRIVE_STR	RW	IO drive strength control [3:0] : PCLKO [7:4] : D[0]	-	0x00
0x3063	[3:0]	IO_DRIVE_STR2	RW	IO drive strength control [3:0] : D[3:1]	-	0x00
0x3064	[2]	ANA_Register_14	RW	Trigger SYNC mode enable [2] : Trigger SYNC mode enable	-	0x00
0x3065	[1:0]	OUTPUT_PIN_STATU S_CONTROL	RW	Output pin status control [1:0]	-	0x00
0x3067	[1:0]	ANA_Register_17	RW	[0] : OSC MCLK switch 0 : OSC mode en 1 : MCLK mode en [1] : Trigger signal sync with MCLK polarity 0 : rising edge 1 : falling edge	-	0x00
0x3068	[0]	PCLK_POLARITY	RW	PCLKO Polarity [0] : pclk_polarity 0 : rising edge 1 : falling edge [7:4]: Reserved	-	0x20

9.15 I2C slave registers

Address	Byte	Register name	Type	Description	CMU	Default (HEX)
0x3400	[0]	I2C_ID_SEL	RW	[0] : I2C ID Selection 0 : Vender defined. 1 : User defined.	-	0x00
0x3401	[6:0]	I2C_ID_REG	RW	[6:0] : User defined I2C ID	-	0x30

10. Electrical Specification

10.1 Absolute maximum ratings

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
Ambient storage temperature		T_{ST}	-30	-	85	°C
Operating temperature		T_{OP}	-20	-	85	°C
Stable image temperature ⁽¹⁾		T_{SI}	0	-	60	°C
Analog supply voltage		$V_{DD-A \text{ MAX}}$	-0.3	-	4.0	V
Digital supply voltage		$V_{DD-D \text{ MAX}}$	-0.3	-	2.0	V
IO supply voltage		$V_{DD-IO \text{ MAX}}$	-0.3	-	4.0	V
DC input voltage		DC_{IN}	-0.3	-	$V_{DD-IO} + 0.3$	V
ESD rating	Human Body Model	ESD	-	2000	-	V
	Machine Model		-	200	-	V

Note: (1) The sensor will produce stable images within the temperature range and the operating limits of the electrical specification. The image quality is not guaranteed when operating the sensor beyond the stable image temperature specification.

(2) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 10.1: Absolute maximum ratings

10.2 Operating voltages

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Analog supply voltage	V_{DD-A}	2.6	2.8	3.0	V
Digital supply voltage	V_{DD-D}	1.35	1.5	1.65	V
LDO supply voltage	$V_{DD-LDOIN}$	1.7	1.8 or 2.8	3.0	V
IO supply voltage	V_{DD-IO}	1.7	1.8 or 2.8	3.0	V

Table 10.2: Operating voltages

10.3 DC characteristics

The power consumptions are measured in sense ($C_L = 5\text{pF}$).

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Average Current Consumption						
I _{DD-AVDD}	Active current	External Internal LDO Mode, 8-bit RAW, QVGA @ 60fps, PCLKO gated, V _{DD-A} = 2.8V, V _{DD-D} = 1.5V, V _{DD-IO} = 1.8V	-	271	-	μA
I _{DD-DVDD}			-	1201	-	
I _{DD-IOVDD}			-	287	-	
I _{DD-AVDD}	Active current	Internal LDO Mode, 8-bit RAW, QVGA @ 60fps, PCLKO gated, V _{DD-A} = 2.8V, V _{DD-IO} = 2.8V	-	278	-	μA
I _{DD-IOVDD}			-	1746	-	
DD-STANDBY	Standby	External Internal LDO Mode, V _{DD-A} = 2.8V, V _{DD-D} = 1.5V, V _{DD-IO} = 1.8	-	105.7	-	μA
DD-STANDBY	Standby	Internal LDO Mode, V _{DD-A} = 2.8V, V _{DD-IO} = 2.8V	-	142.3	-	μA
Digital Inputs (MCLK, TRIG, SCL)						
V _{IL}	Input Voltage Low	-	GND - 0.3	-	0.3V _{DD-IO}	V
V _{IH}	Input Voltage High	-	0.7V _{DD-IO}	-	V _{DD-IO} + 0.3	V
C _{IN}	Input Capacitance	-		4	-	pF
Digital Output						
V _{OL}	Output Voltage Low	-	-	-	0.2V _{DD-IO}	V
V _{OH}	Output Voltage High	-	0.8V _{DD-IO}	-	-	V
C _{OUT}	Output Capacitance	-	-	4	-	pF
R _{OUT}	Output Resistance	-	-	1	-	Ω
I _{oz}	Tri-state Leakage Current	-	-	-	10	μA

Table 10.3: DC characteristics

10.4 Master clock input (MCLK)

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
MCLK	Input frequency	-	3	-	36	MHz
MCLK _{DUTY}	Input clock duty cycle	-	45	-	55	%

Table 10.4: Master Clock (MCLK) timing

10.5 Serial bus characteristics

Symbol	Parameter	Condition	Spec.			Unit
			Min.	Typ.	Max.	
F_{SCL}	Input clock frequency	-	100	-	400	kHz
t_{SCL}	Input clock period	-	2.5	-	10	μ s
-	Input clock duty cycle	-	40	50	60	%
t_{RT}	Rise time of SCL/SDA	-	-	-	$0.12T_{SCL}$	ns
t_{FT}	Fall time of SCL/SDA	-	-	-	$0.12T_{SCL}$	ns
t_{HD_SU}	Start setup time	Write	T_{MCLK}	-	-	ns
t_{HD_STA}	Start hold time	Write	$3T_{MCLK}$	-	-	ns
t_{HD_DAT}	Data hold time	Write	5	-	-	ns
t_{SU_DAT}	Data setup time	Write	$3T_{MCLK}$	-	-	ns
t_{SU_STP}	Stop setup time	Write	$3T_{MCLK}$	-	-	ns
t_{HD_STP}	Stop hold time	Write	T_{MCLK}	-	-	ns
t_{HD_DATR}	Data hold time	Read	$3T_{MCLK}$	-	-	ns
t_{SU_DATR}	Data setup time	Read	$T_{SCL}/2 - t_{HD_DATR}$	-	-	ns
C_{SDA_LOAD}	SDA maximum load capacitance	-	-	-	4.2	pF
R_{SDA}	SDA pull-up resistor	-	500	-	-	$\square$

Note: (1) T_{MCLK} = Cycle time of MCLK, T_{SCL} = Cycle time of SCL.

Table 10.5: Serial bus interface timing

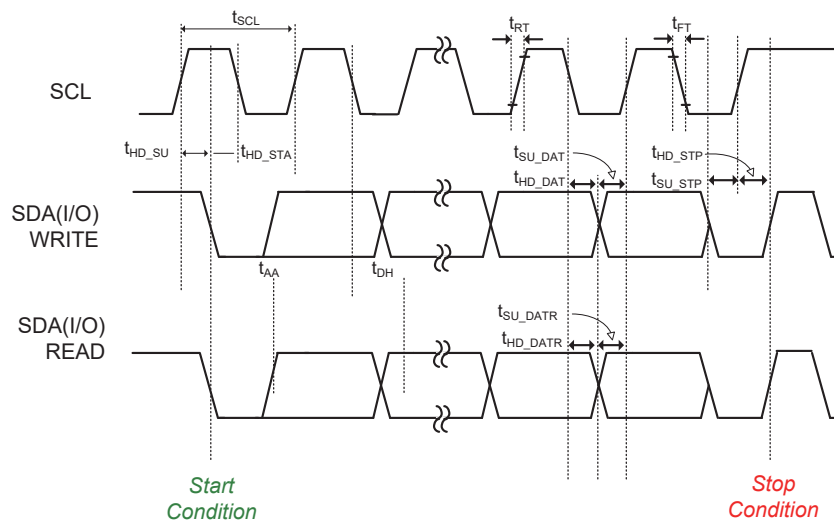


Figure 10.1: 2-wire serial interface timing diagram

10.6 Parallel interface timing characteristics

Conditions: $T_A = 25^\circ\text{C}$, $C_L = 5\text{pF}$, $F_{\text{PCLKO}} = 12\text{MHz}$

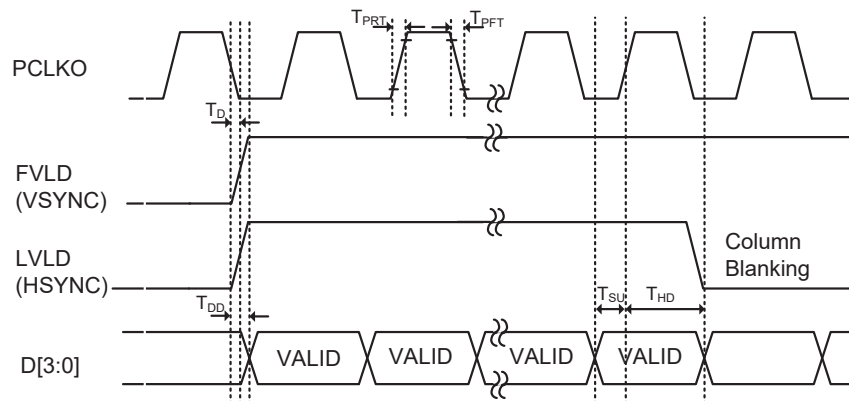


Figure 10.2: 4-bit parallel video interface timing diagram

Symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
T_{PCLKO}	PCLKO period	-	83.29	-	ns
T_{PRT}	PCLKO rise time	-	14.35	-	ns
T_{PFT}	PCLKO fall time	-	10.53	-	ns
T_D	PCLKO falling edge to HSYNC, VSYNC rising edge delay	-	69.6	-	ns
T_{DD}	PCLKO falling edge to DATA transition delay	-	88	-	ns
T_{SU}	Data bus setup time	-	37.2	-	ns
T_{HD}	Data bus hold time	-	43.6	-	ns

Table 10.6: 4-bit parallel video interface timing

10.7 Serial interface timing characteristics

Conditions: $T_A = 25^\circ\text{C}$, $C_L = 5\text{pF}$, $F_{\text{PCLKO}} = 36\text{MHz}$

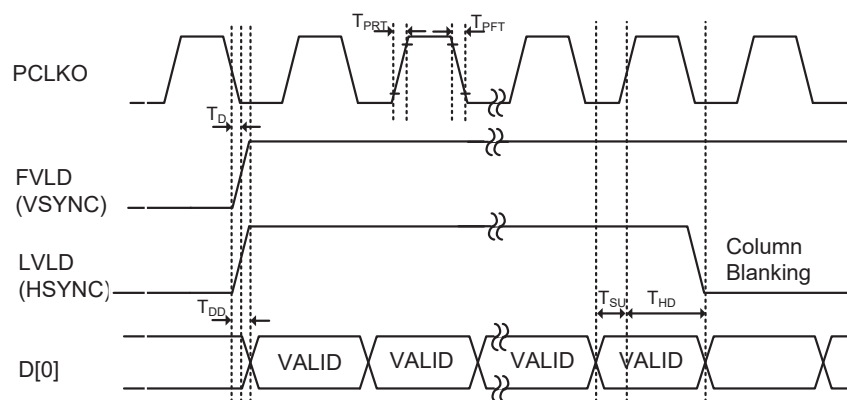


Figure 10.3: Serial video interface timing diagram

Symbol	Parameter Name	Spec.			Unit
		Min.	Typ.	Max.	
T_{PCLKO}	PCLKO period	-	27.78	-	ns
T_{PRT}	PCLKO rise time	-	6.19	-	ns
T_{PFT}	PCLKO fall time	-	5.72	-	ns
T_D	PCLKO falling edge to HSYNC, VSYNC rising edge delay	-	23.4	-	ns
T_{DD}	PCLKO falling edge to DATA transition delay	-	31.2	-	ns
T_{SU}	Data bus setup time	-	11.5	-	ns
T_{HD}	Data bus hold time	-	15.2	-	ns

Table 10.7: Serial video interface timing

11. Chief Ray Angle

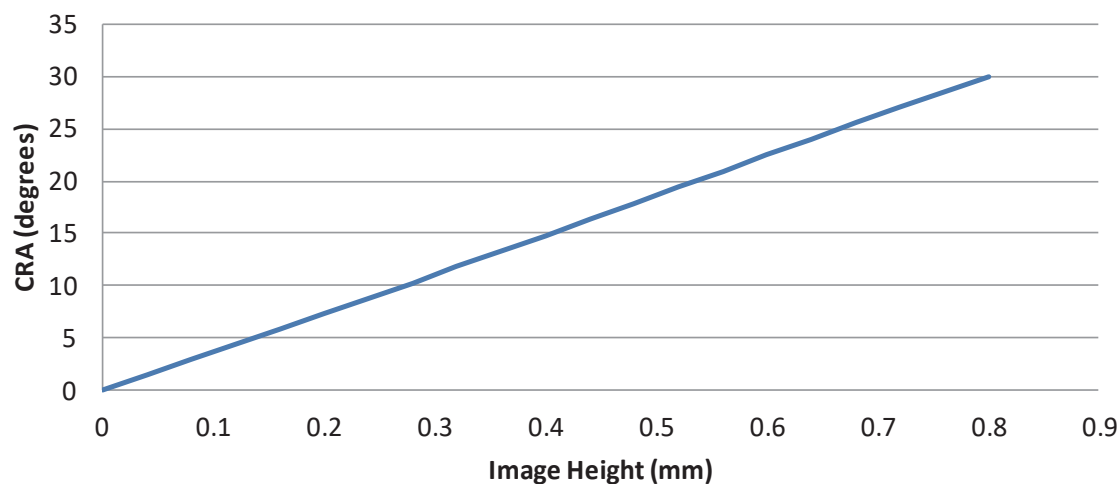


Figure 11.1: Chief ray angle

Field (%)	Image Height (mm)	CRA (degree)
0.00	0	0.00
0.10	0.08	2.87
0.20	0.16	5.77
0.30	0.24	8.74
0.40	0.32	11.75
0.50	0.4	14.80
0.60	0.48	17.86
0.70	0.56	20.93
0.80	0.64	23.99
0.90	0.72	27.04
1.00	0.8	30.05

Table 11.1: Chief ray angle