

150V N-Channel Enhancement Mode MOSFET

Description

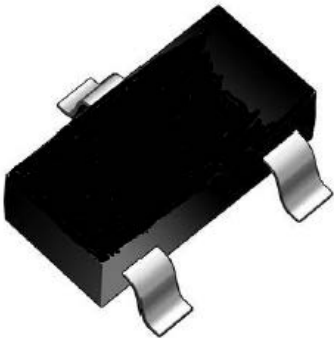
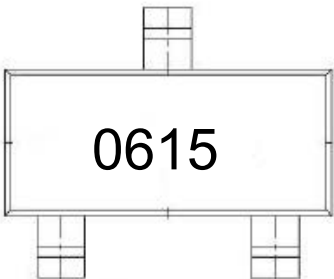
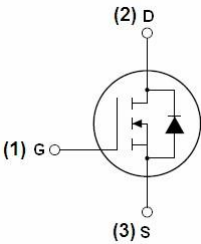
The HM06N15MR uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 150V, I_D = 0.6A$
- $R_{DS(ON)} < 880m\Omega @ V_{GS}=10V$ (Typ:700m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HM06N15MR	SOT23-3	0615	3000

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	0.6	A
Drain Current-Pulsed (Note 1)	I_{DM}	1.8	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	41.7	$^{\circ}C/W$



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Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.6A	-	700	880	mΩ
Forward Transconductance	g _{FS}	V _{DS} =15V, I _D =0.6A	-	8	-	S
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	580	-	PF
Output Capacitance	C _{oss}		-	90	-	PF
Reverse Transfer Capacitance	C _{rss}		-	3	-	PF
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	15	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =100V, I _D =0.6A, V _{GS} =10V	-	12	-	nC
Gate-Source Charge	Q _{gs}		-	2.5	-	nC
Gate-Drain Charge	Q _{gd}		-	3.8	-	nC
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =0.6A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	0.6	A

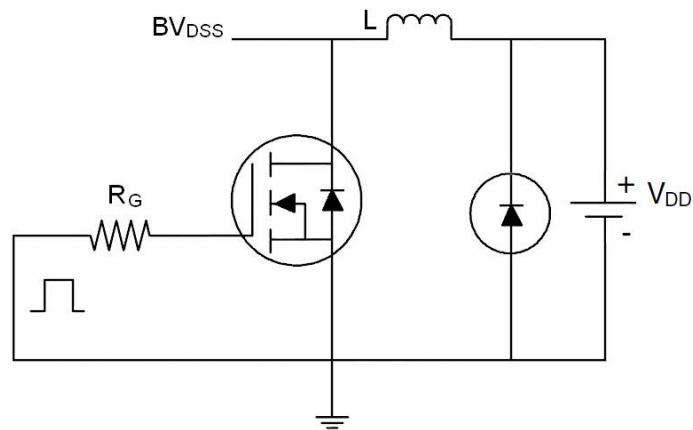
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

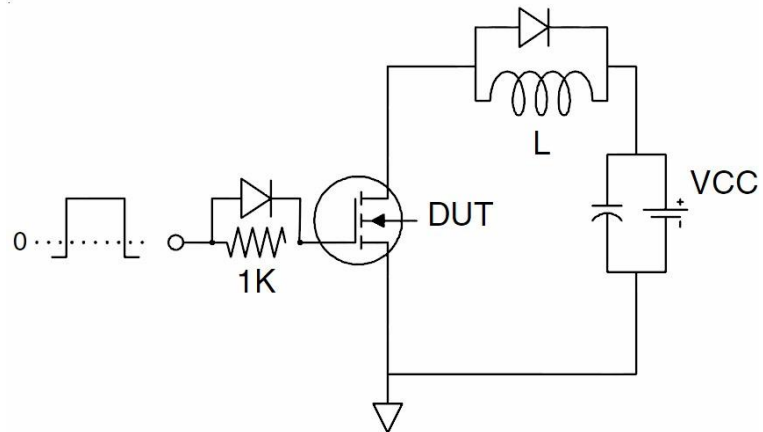
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Test Circuit

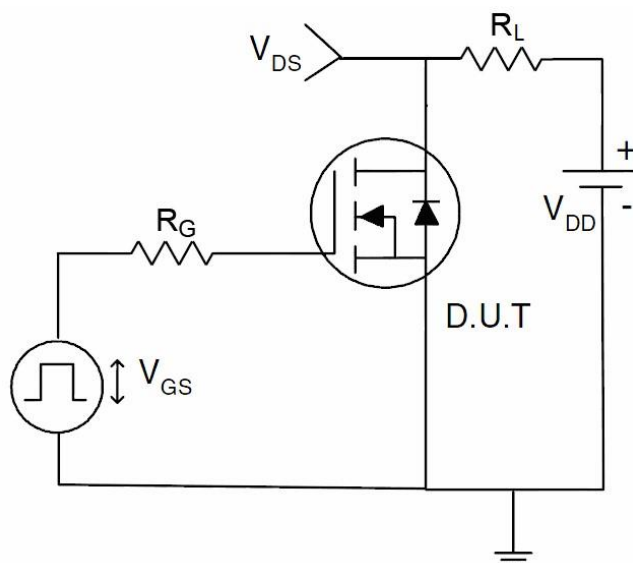
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

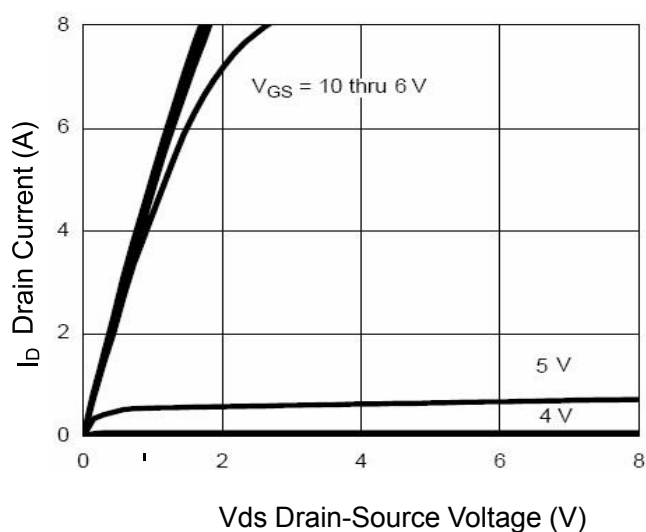


Figure 1 Output Characteristics

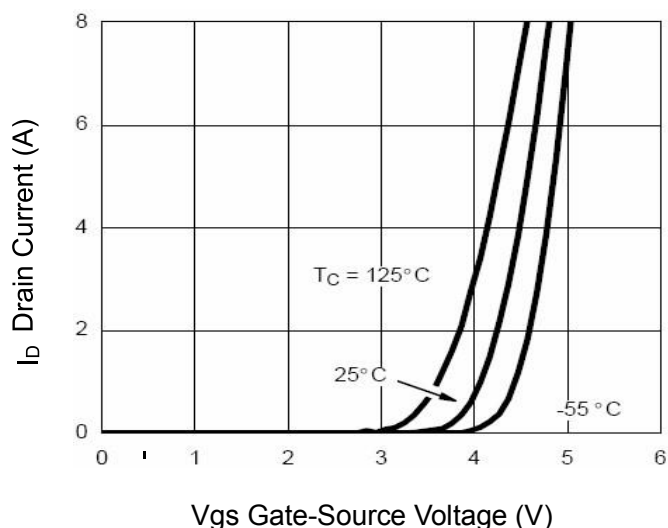


Figure 2 Transfer Characteristics

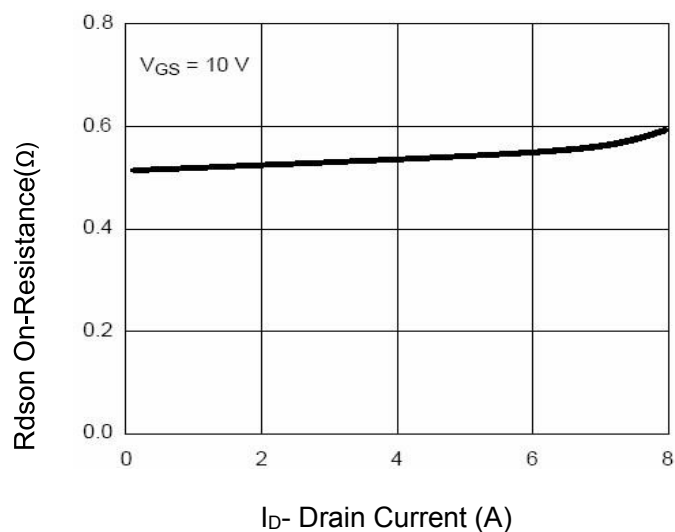


Figure 3 $R_{DS(on)}$ - Drain Current

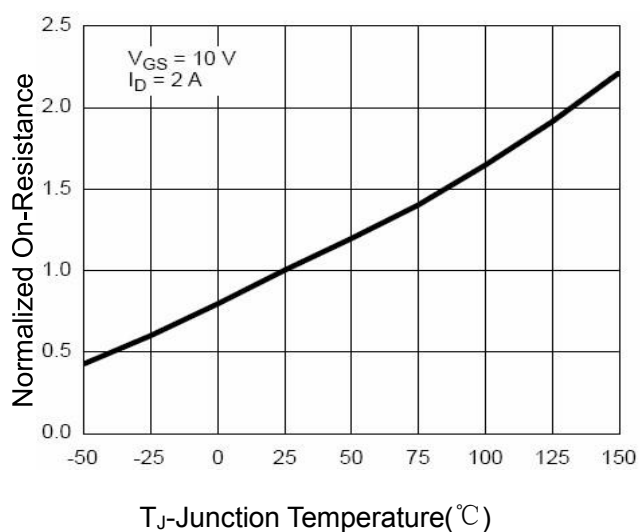


Figure 4 $R_{DS(on)}$ -Junction Temperature

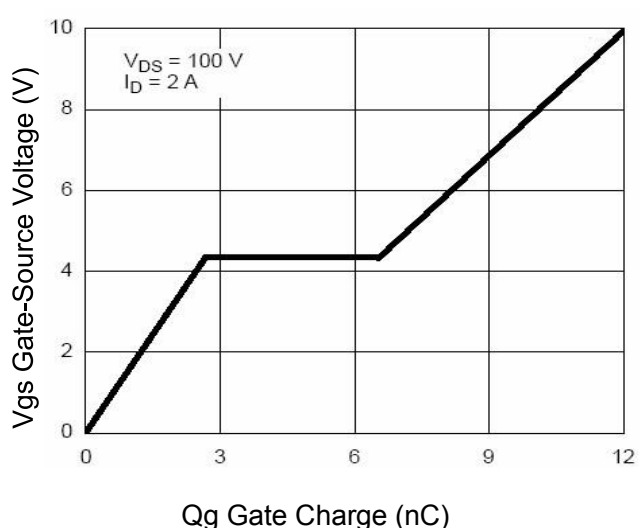


Figure 5 Gate Charge

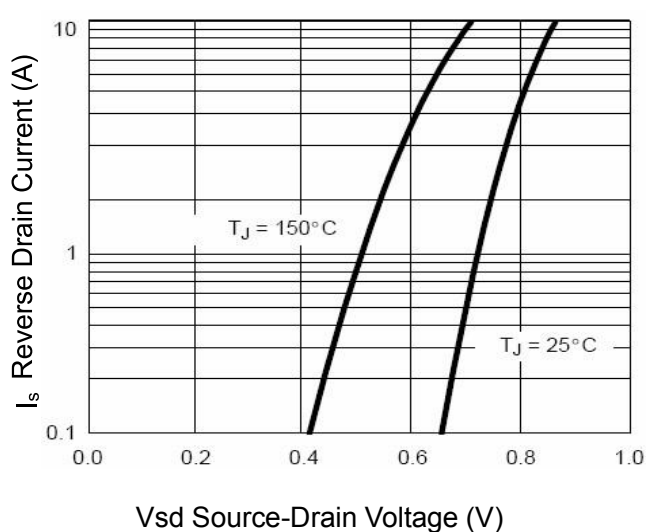
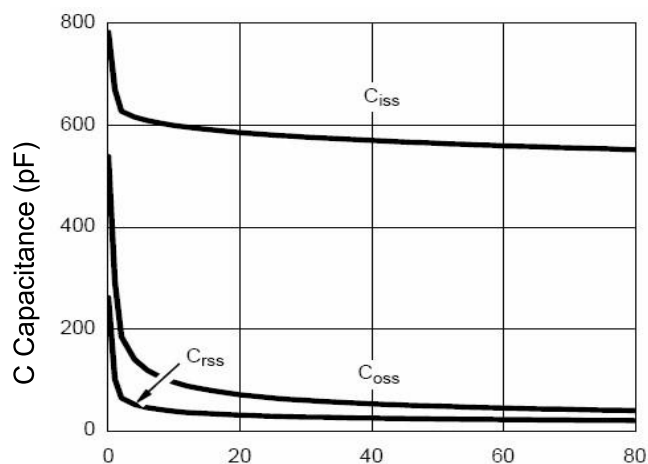
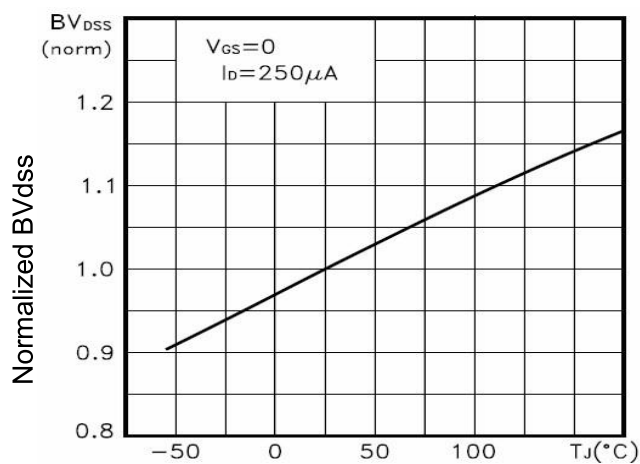


Figure 6 Source- Drain Diode Forward



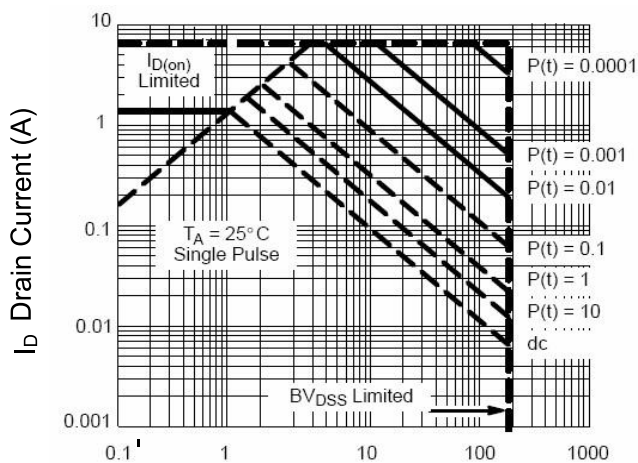
V_{DS} Drain-Source Voltage (V)

Figure 7 Capacitance vs V_{DS}



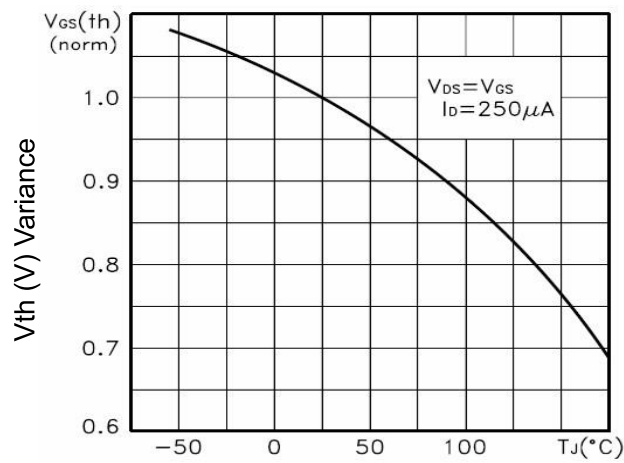
T_J -Junction Temperature($^{\circ}C$)

Figure 9 BV_{DSS} vs Junction Temperature



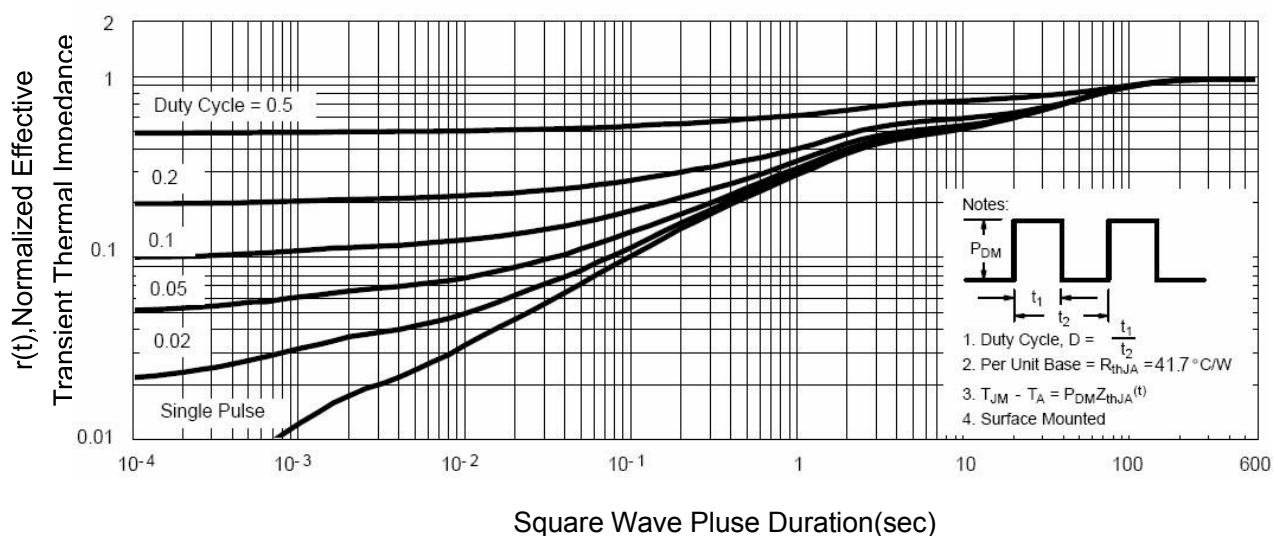
V_{DS} Drain-Source Voltage (V)

Figure 8 Safe Operation Area



T_J -Junction Temperature($^{\circ}C$)

Figure 10 $V_{GS(th)}$ vs Junction Temperature



Square Wave Pulse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

SOT23-3L Package outline

