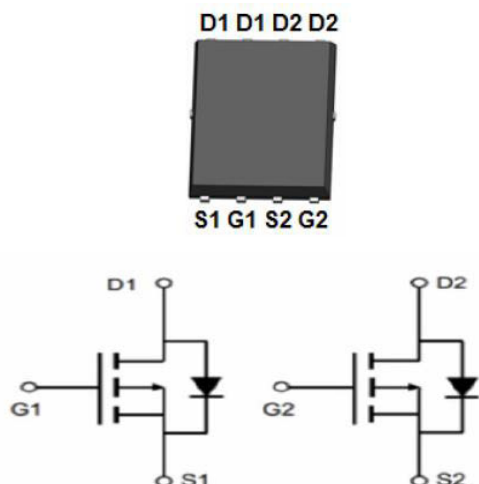


P-Channel Enhancement Mode Field Effect Transistor

DFN5X6-8L



Product Summary

- V_{DS} -100V
- I_D -7A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) <225mohm
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) <210mohm
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) <30mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current ^B	$T_A=25^\circ\text{C}$ @ Steady State	I_D	-7	A
	$T_A=100^\circ\text{C}$ @ Steady State		-4.9	
Drain Current ^B	$T_A=25^\circ\text{C}$ @ Steady State	I_D	-10	A
	$T_A=70^\circ\text{C}$ @ Steady State		-8	
Pulsed Drain Current ^A		I_{DM}	21	A
Single Pulse Avalanche Energy ^B		E_{AS}	31	mJ
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$ @ Steady State	P_D	32	W
	$T_A=100^\circ\text{C}$ @ Steady State		12.8	
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$ @ Steady State	P_D	3	W
	$T_A=70^\circ\text{C}$ @ Steady State		1.9	
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JC}$	3.9	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case @ Steady State ^C		$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
HM07DP10D	F1	HM07DP10D XXXX	5000	10000	100000	13" reel

■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V, T_C=25^{\circ}C$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}= \pm 10V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}= V_{GS}, I_D=-250\mu A$	-1.2		-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}= -4.5V, I_D=-2A$			225	m Ω
		$V_{GS}= -10V, I_D=-5A$			210	
Diode Forward Voltage	V_{SD}	$I_S=-7A, V_{GS}=0V$		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		2992		pF
Output Capacitance	C_{oss}			330		
Reverse Transfer Capacitance	C_{rss}			272		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-15V, I_D=-9.1A$		72.8		nC
Gate Source Charge	Q_{gs}			6.6		
Gate Drain Charge	Q_{gd}			10.1		
Reverse Recovery Charge	Q_{rr}	$I_F=-6A, di/dt=100A/us$		34		
Reverse Recovery Time	t_{rr}			67		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, I_D=-6A, R_{GEN}=2.5\Omega$		7		ns
Turn-on Rise Time	t_r			33		
Turn-off Delay Time	$t_{D(off)}$			130		
Turn-off Fall Time	t_f			132		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

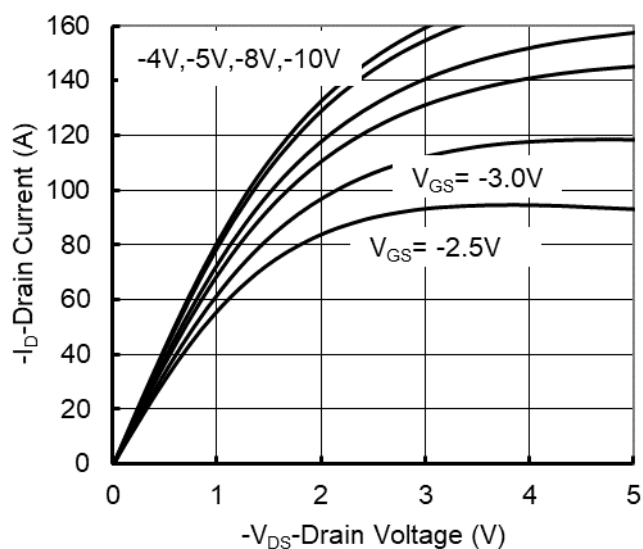


Figure 1. Output Characteristics

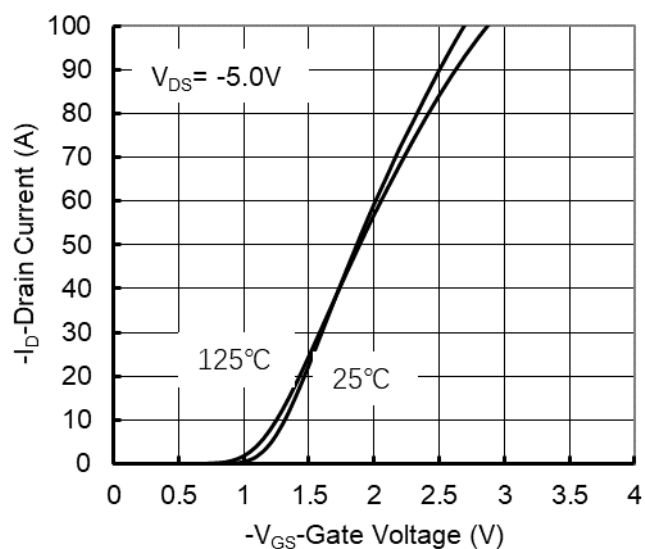


Figure 2. Transfer Characteristics

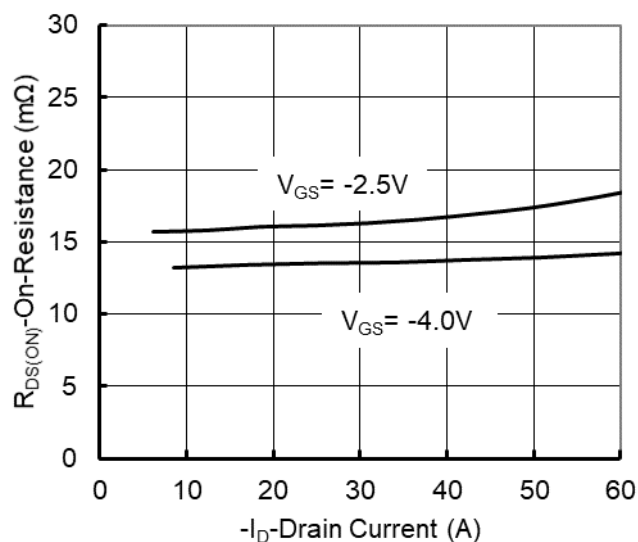


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

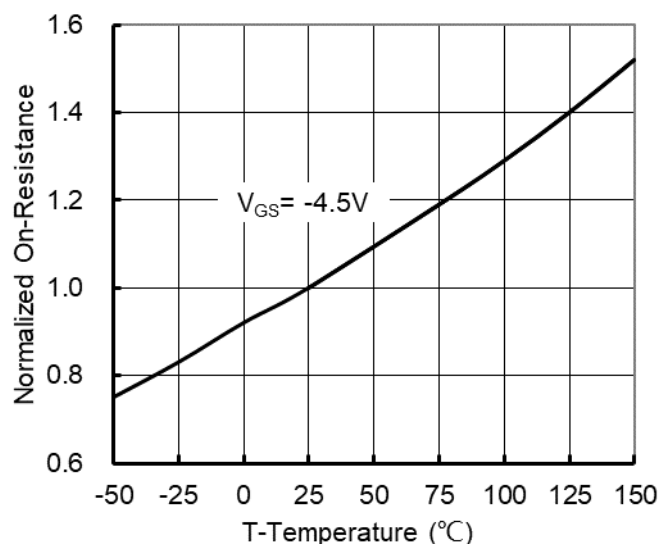


Figure 4. On-Resistance vs. Junction Temperature

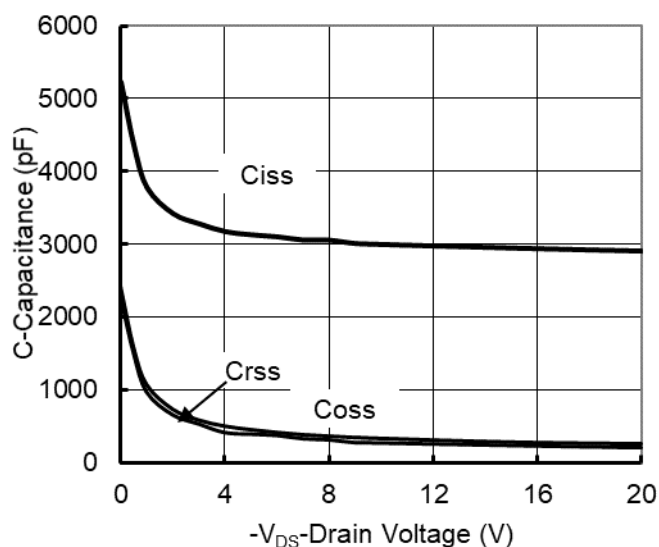


Figure 5. Capacitance Characteristics

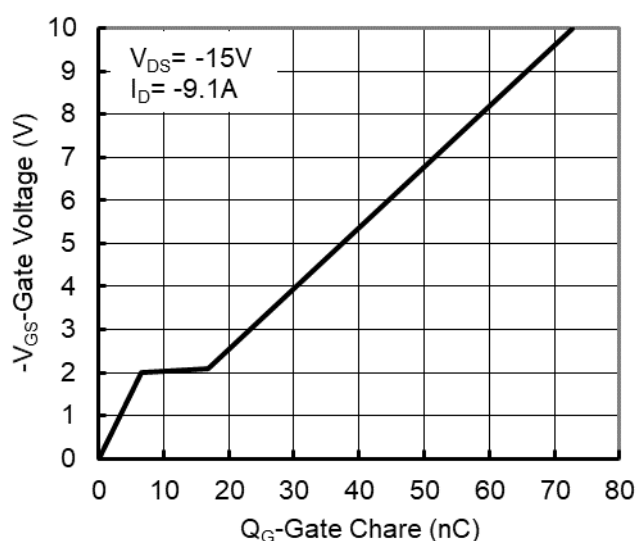


Figure 6. Gate Charge

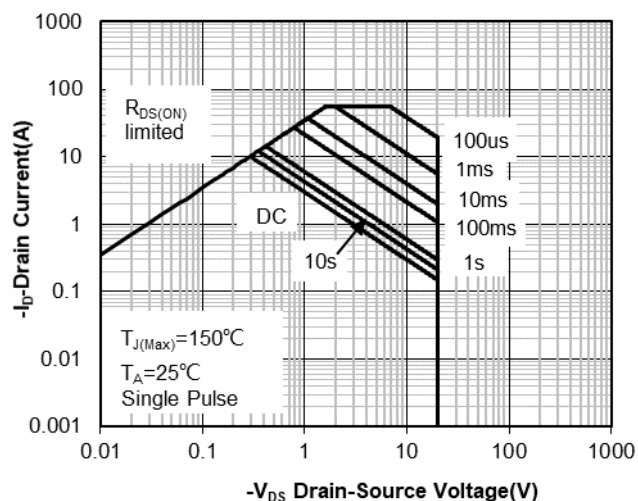


Figure 7. Safe Operation Area

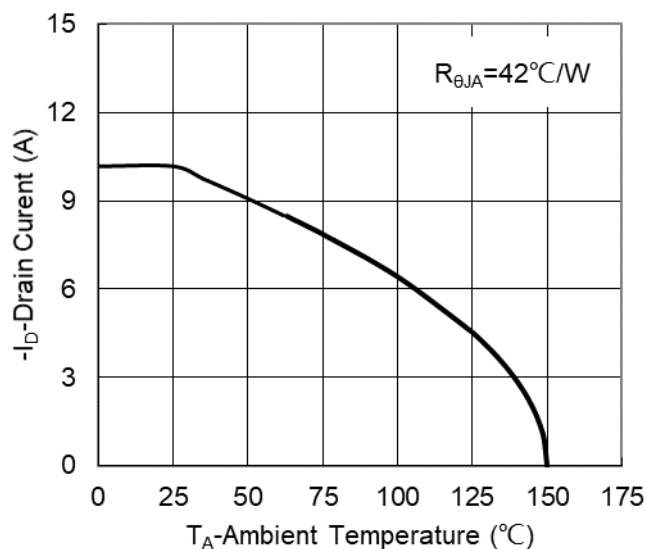


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

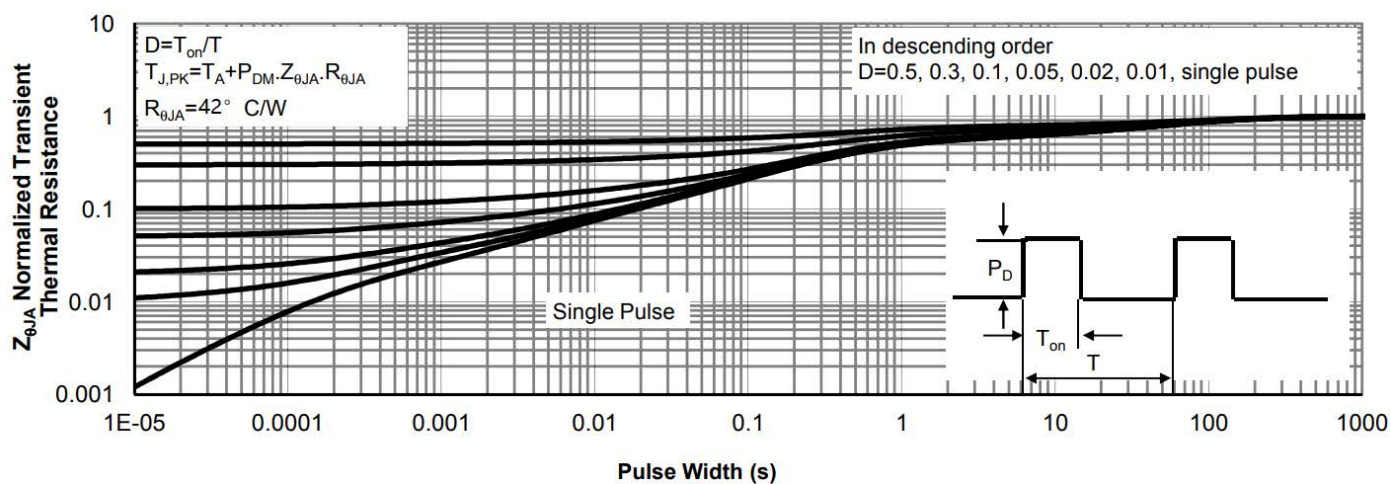
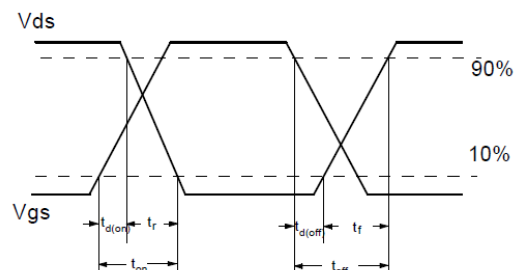
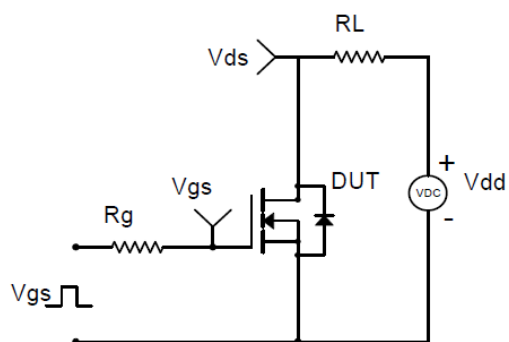
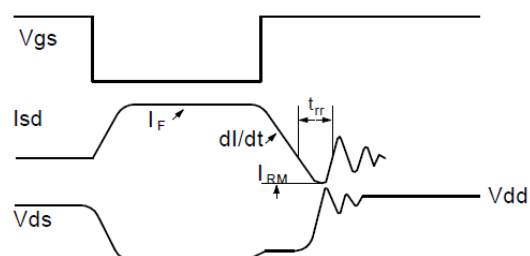
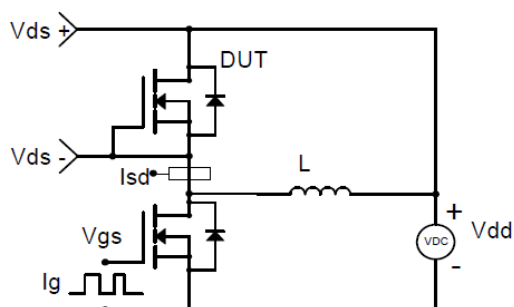


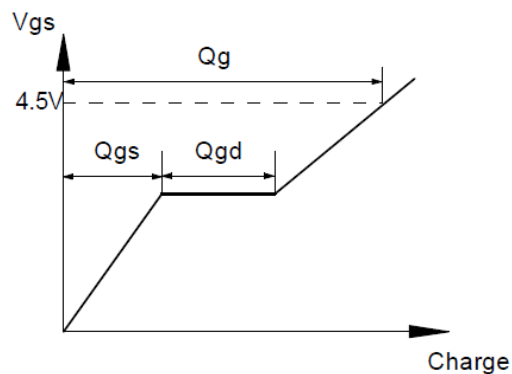
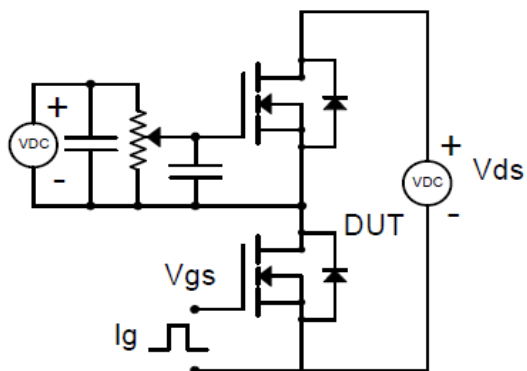
Figure 9. Normalized Maximum Transient Thermal Impedance



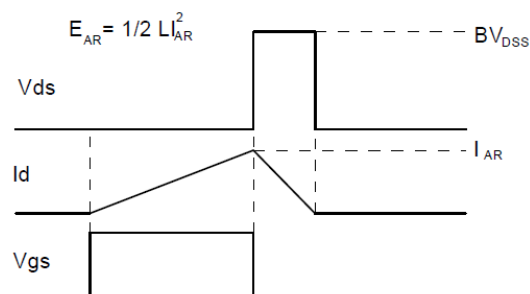
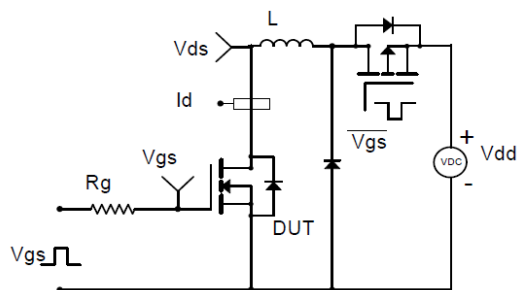
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

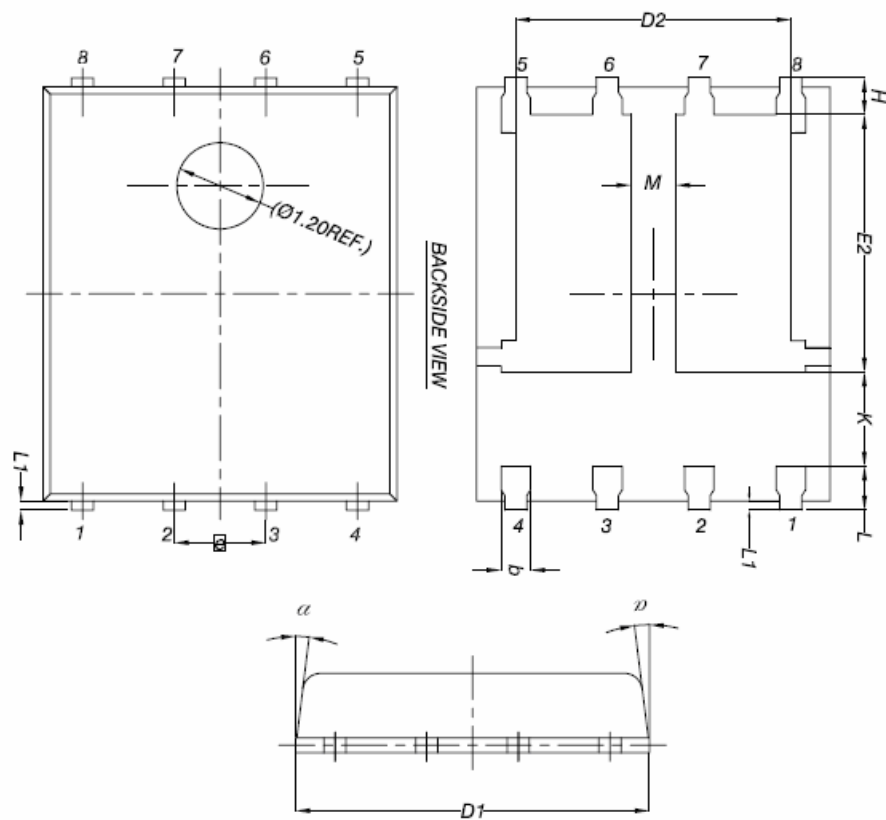


Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°

