

N-Channel Enhancement Mode Power MOSFET

DESCRIPTION

The HM12N20D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

GENERAL FEATURES

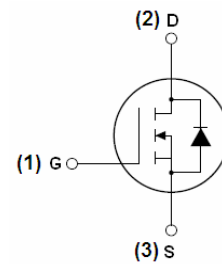
- $V_{DS} = 200V, I_D = 12A$
 $R_{DS(ON)} < 80m\Omega @ V_{GS} = 10V$ (Typ: 63mΩ)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

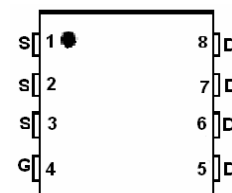
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM12N20D	HM12N20D	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	12	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	8	A
Pulsed Drain Current	I_{DM}	36	A
Maximum Power Dissipation	P_D	150	W
Single pulse avalanche energy (Note 5)	E_{AS}	250	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	1	$^{\circ}\text{C/W}$
--	-----------------	---	----------------------

Electrical Characteristics (TC=25 $^{\circ}\text{C}$ unless otherwise noted)

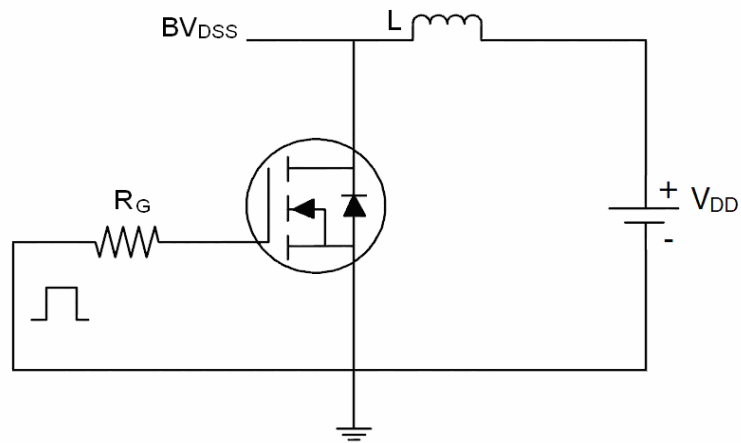
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	220	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	3.2	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =15A	-	63	80	mΩ
Forward Transconductance	g _{FS}	V _{DS} =50V, I _D =15A	30	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz		4200		PF
Output Capacitance	C _{OSS}			163		PF
Reverse Transfer Capacitance	C _{RSS}			75		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V, I _D =15A V _{GS} =10V, R _{GEN} =2.5Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}		-	22	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =100V, I _D =15A, V _{GS} =10V		60		nC
Gate-Source Charge	Q _{gs}			19		nC
Gate-Drain Charge	Q _{gd}			17		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =11A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S	-	-	-	12	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 15A	-	90	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs(Note3)	-	300	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

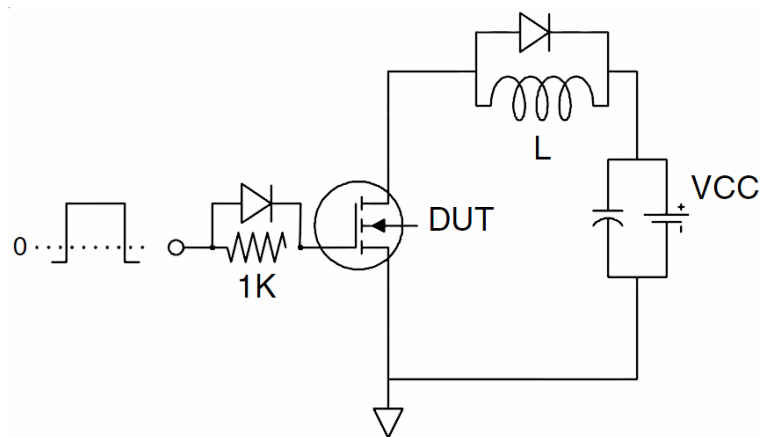
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=100V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

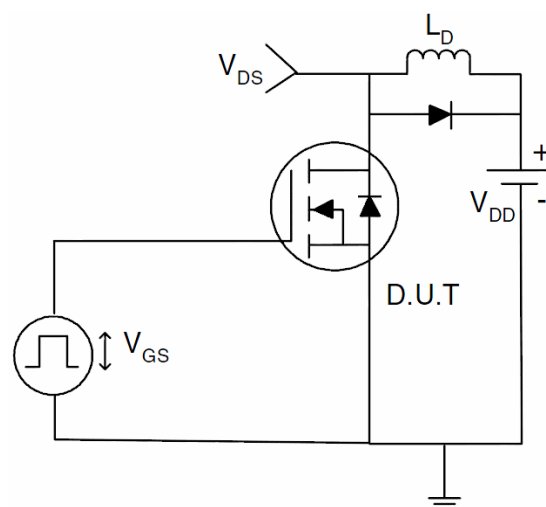
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

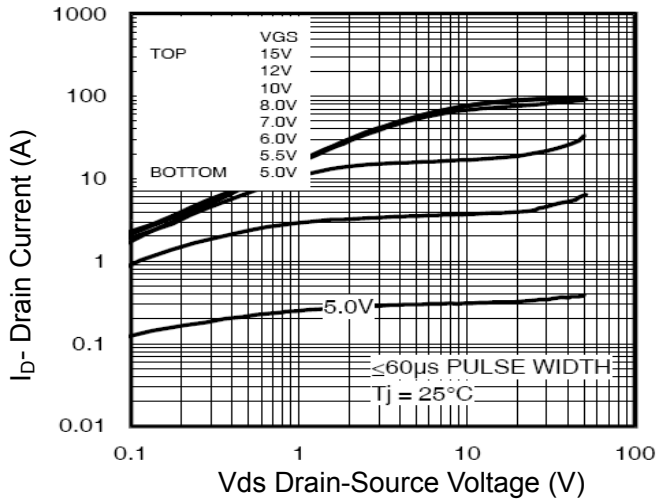


Figure 1 Output Characteristics

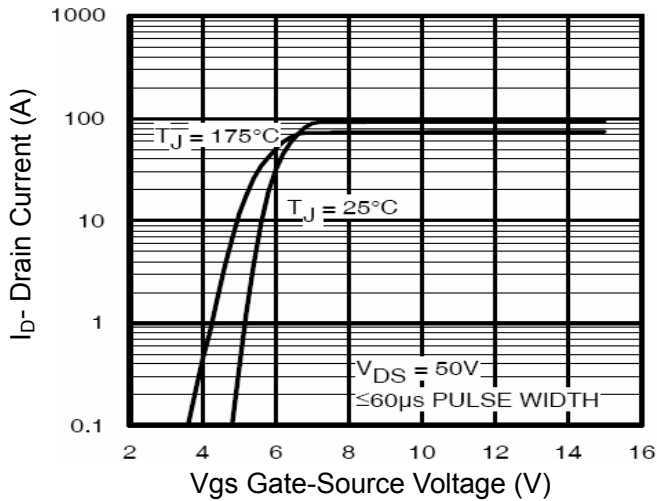


Figure 2 Transfer Characteristics

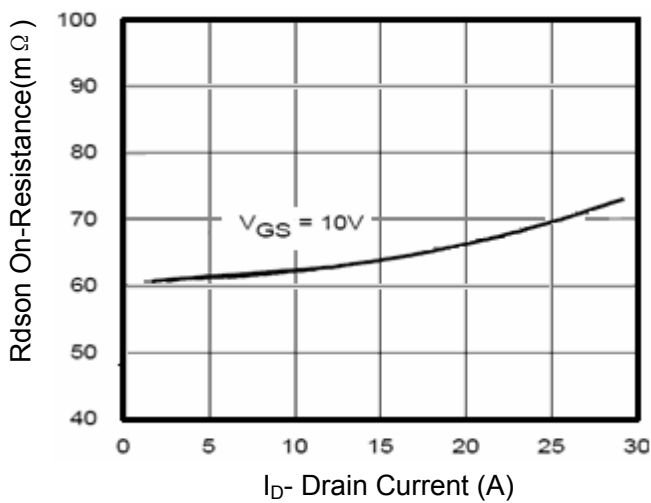


Figure 3 Rdson- Drain Current

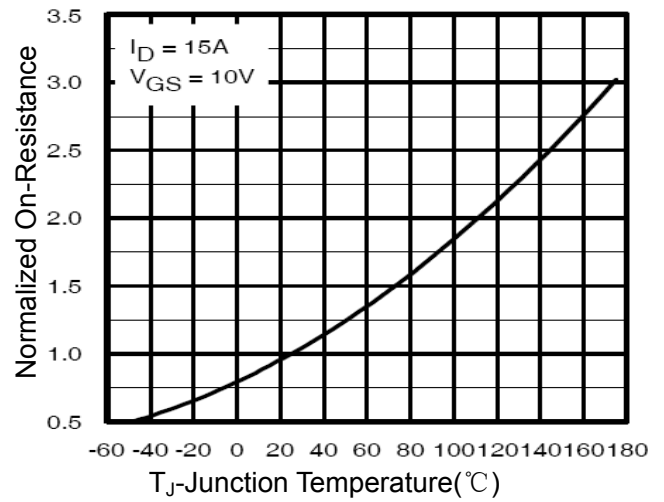


Figure 4 Rdson-Junction Temperature

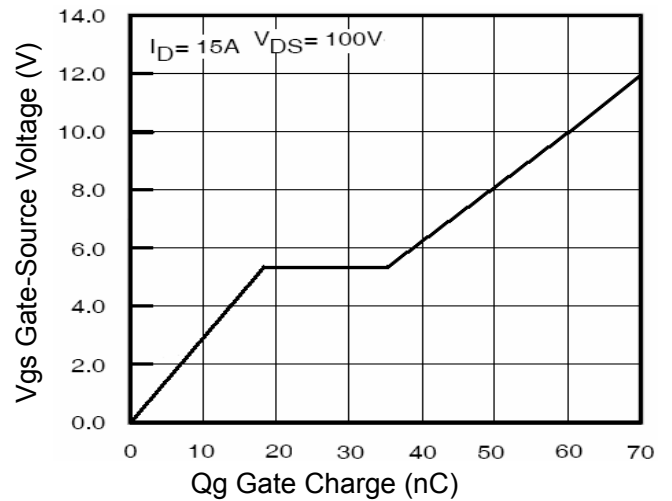


Figure 5 Gate Charge

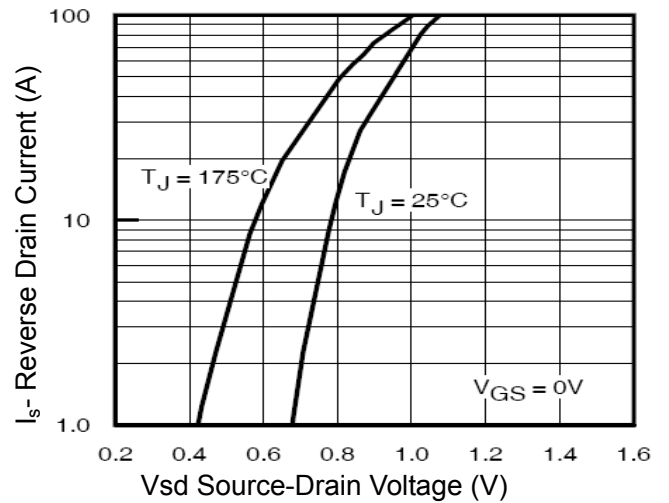


Figure 6 Source- Drain Diode Forward

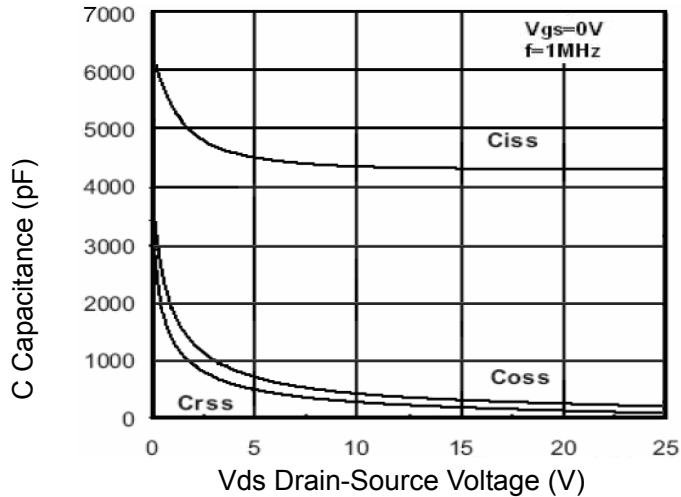


Figure 7 Capacitance vs Vds

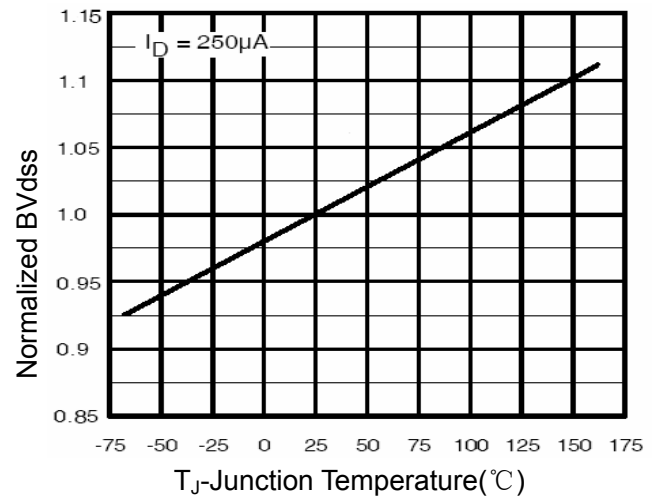


Figure 9 BV_{DSS} vs Junction Temperature

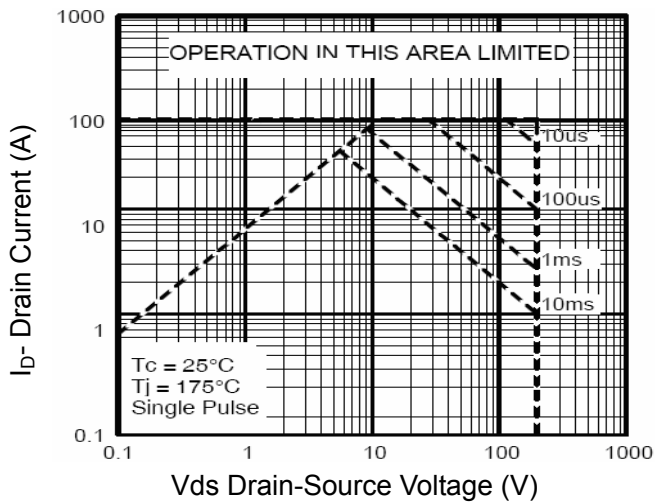


Figure 8 Safe Operation Area

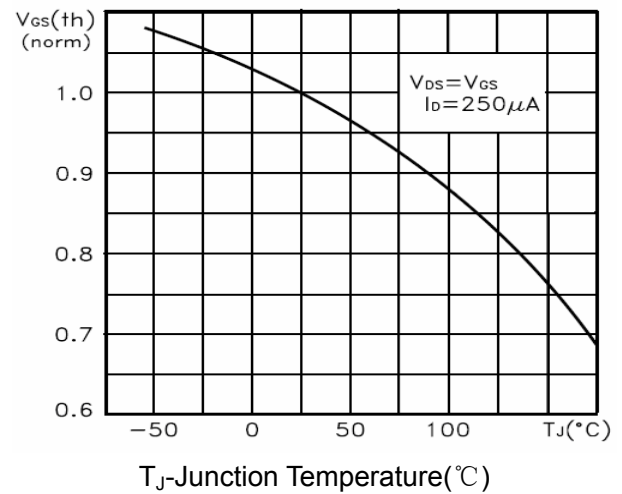


Figure 10 $V_{GS(th)}$ vs Junction Temperature

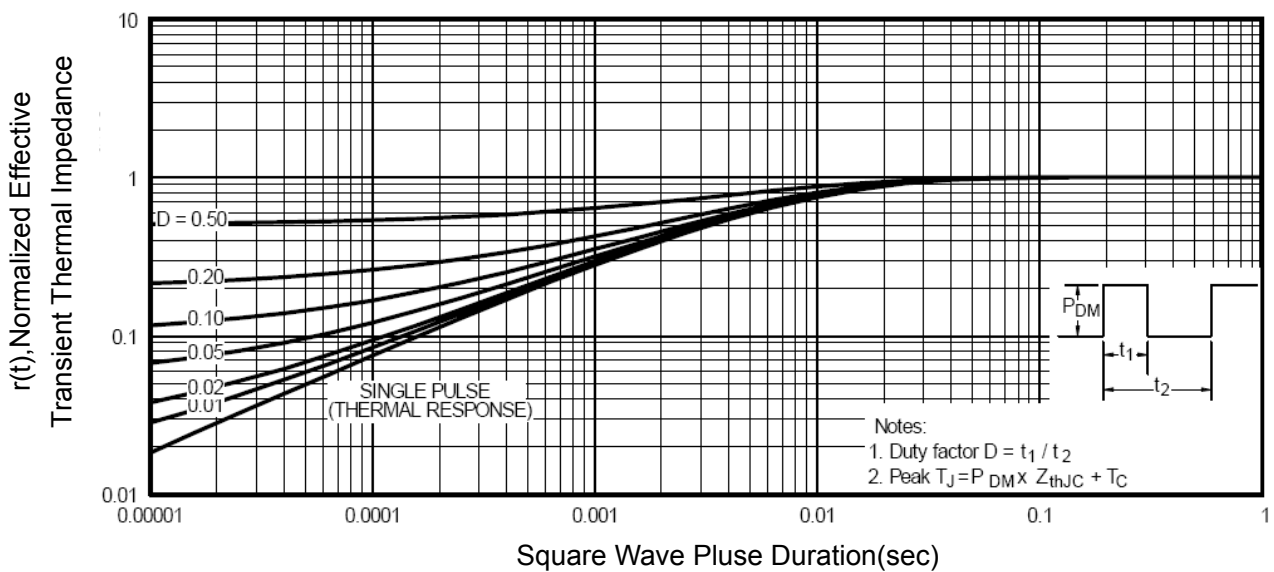
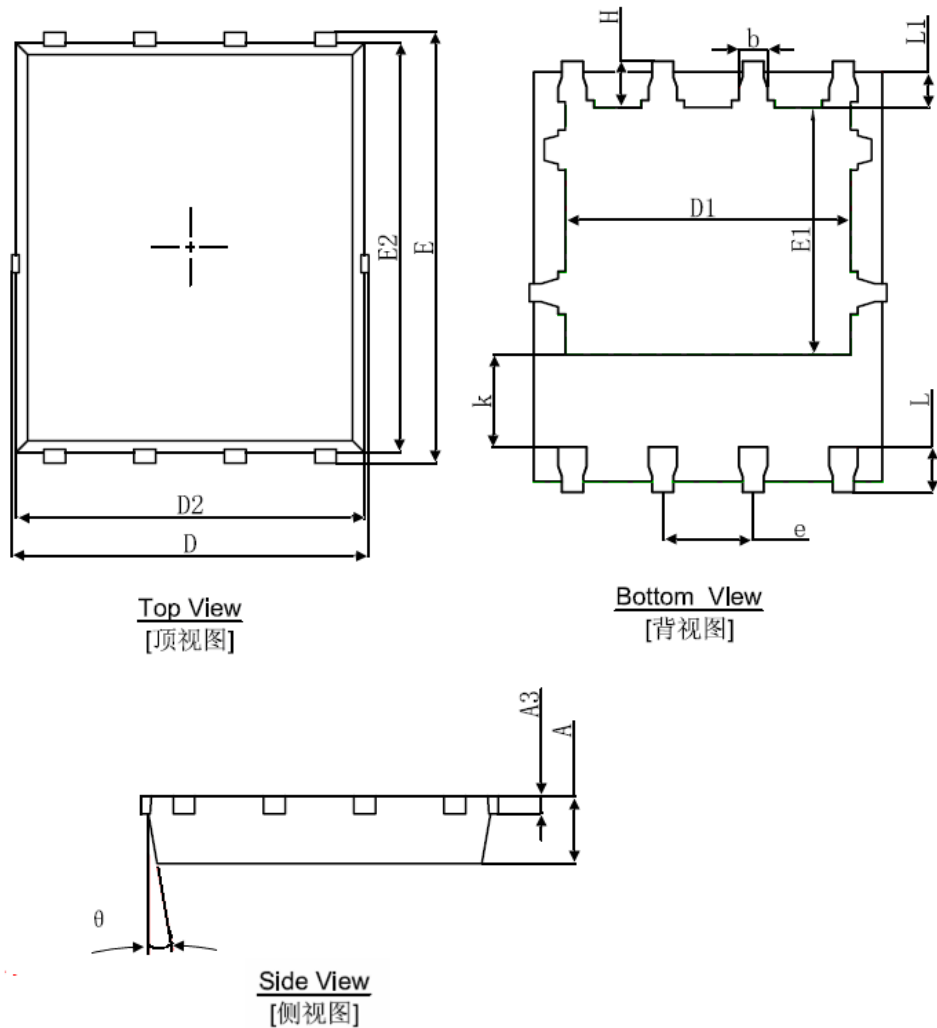


Figure 11 Normalized Maximum Transient Thermal Impedance



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°