

## Wide Range Synchronous Buck Controller

### Feature

- Wide Input Voltage Range: 8V to 30V
- Up to 93% Efficiency
- Programmable Switching Frequency up to up to 500kHz
- No Loop Compensation Required
- Programmable current limit
- Thermal Shutdown
- Available in SOP-8L Package

### Application

- Car Charger / Adaptor
- Pre-Regulator for Linear Regulators
- Distributed Power Systems
- Battery Charger

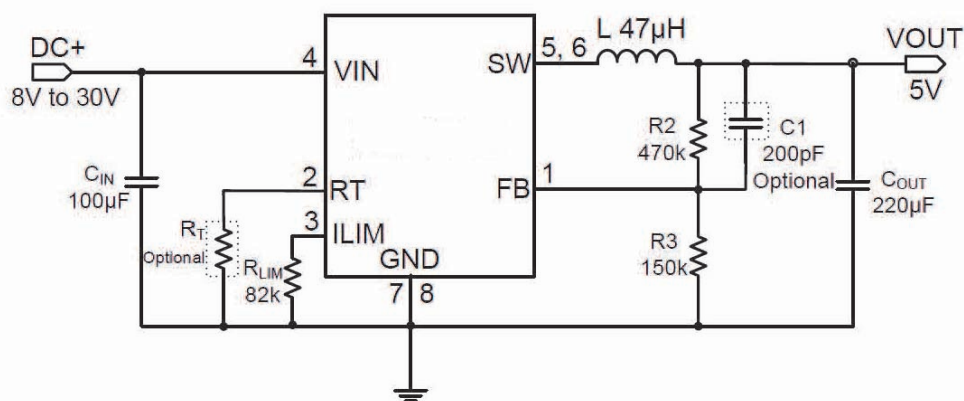
### Description

The PT FI Ì HÔ is a synchronous step down regulator from a high voltage input supply. Operating with an input voltage range from 8V to 30V, the PT FI Ì HÔ achieves 2.8A continuous output current with excellent load and line regulation. The switching frequency is programmable from 130 kHz to 500 kHz and the synchronous architecture provides for highly efficient designs. Current mode operation provides fast transient response and eases loop stabilization.

The PT FI Ì HÔ requires a minimum number of readily available standard external components. Other features include cable compensation, programmable current limit and thermal shutdown.

The PT FI Ì HÔ converters are available in the industry standard SOP-8L packages.

### Typical Application Circuit

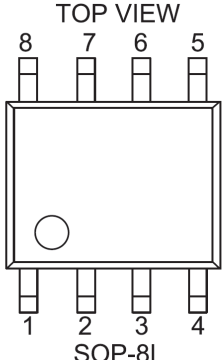


\* The output voltage is set by R2 and R3:  $V_{OUT} = 1.21V \cdot [1 + (R2/R3)]$ .

\* RT: RT is optional. The resistor range is from 130KΩ to 1.5 MΩ. PT FI Ì HÔ can work when keeping RT pin floating. The default frequency is 130KHZ.

\* ILIM: PT FI Ì HÔ can work when keeping ILIM pin floating, with 3A limit current in this situation.

## Pin Assignment and Description

TOP VIEW	PIN	NAME	DESCRIPTION
	 <p>TOP VIEW</p> <p>8 7 6 5</p> <p>1 2 3 4</p> <p>SOP-8L</p>	1	FB
	2	RT	Frequency Setting
	3	ILIM	Current Limit
	4	VIN	Input Supply Voltage
	5, 6	SW	Switch Node
	7, 8	GND	Ground

## Absolute Maximum Ratings (Note 1)

- Input Supply Voltage .....-0.3V ~ 35V
- FB, ILIM, RT Voltages..... -0.3V ~ 6V
- SW Voltage .....-0.3V ~ (VIN + 1V)
- Operating Temperature Range (Note 2).....-40°C ~ +85°C
- Storage Temperature Range..... -65°C ~ +150°C
- Junction Temperature Range.....+150°C
- Lead Temperature (Soldering, 10 sec.)..... +265°C

**Note 1:** Stresses beyond those listed Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The PT FI Ì HÔ is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

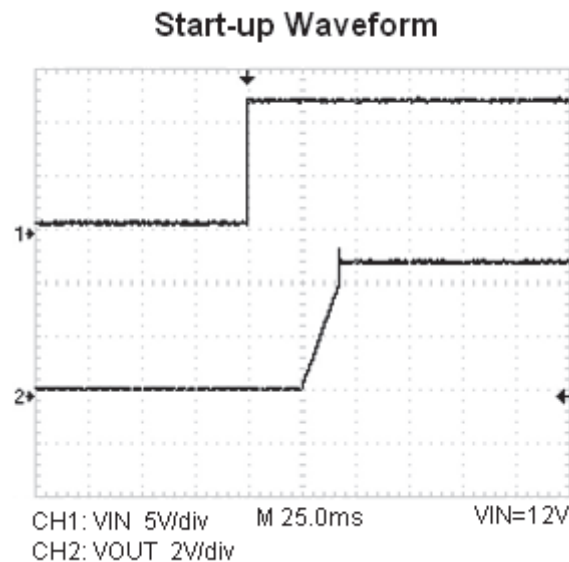
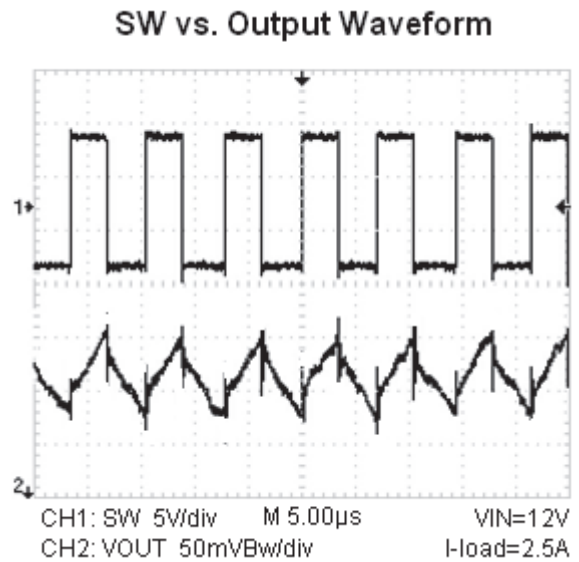
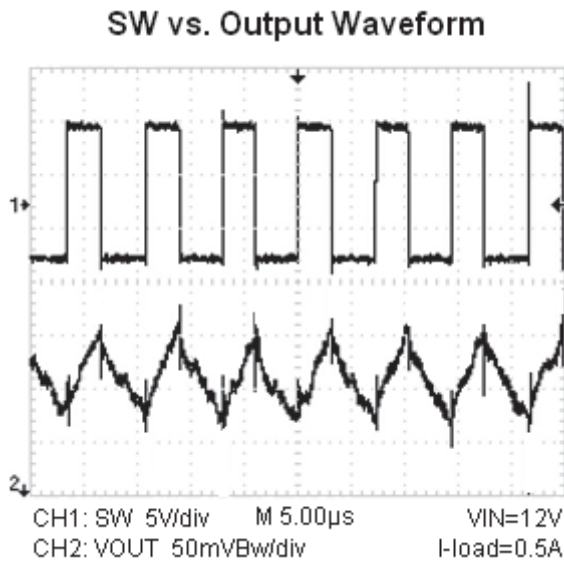
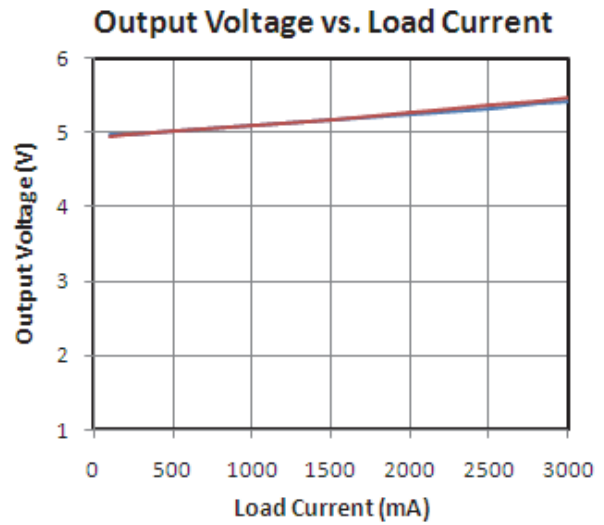
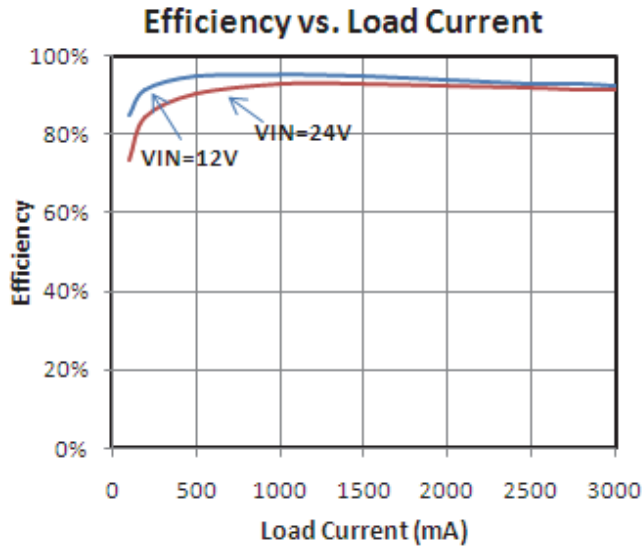
## Electrical Characteristics

Operating Conditions:  $T_A=25^{\circ}\text{C}$ ,  $V_{IN}=12\text{V}$ ,  $R_2=470\text{k}$ ,  $R_3=150\text{k}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Operating Voltage Range		8		30	V
$I_Q$	Quiescent Current	$I_{LOAD}=0\text{A}$	10	15	20	mA
$V_{UVLO}$	Input UVLO Threshold			4.25	4.5	V
$\Delta V_{UVLO}$	UVLO Hysteresis			50	100	mV
$V_{FB}$	Regulated Voltage		1.188	1.21	1.236	V
$I_{FB}$	Feedback Pin Input Current				0.05	$\mu\text{A}$
$f_{OSC}$	Oscillator Frequency Range	Float RT Pin		130		kHz
$f_{OSC\_MAX}$	Maximum Oscillator Frequency			500		kHz
DC	Max Duty Cycle				90	%
$I_{LIM\_def}$	Default Limit Current	Float ILIM Pin		3.0		A
$I_{LIM-TH}$	Current Limit Sense Pin Source Current		7	8.5	10	$\mu\text{A}$
$R_{PFET}$	$R_{DS(ON)}$ of P-Channel FET			40		$\text{m}\Omega$
$R_{NFET}$	$R_{DS(ON)}$ of N-Channel FET			30		$\text{m}\Omega$
$T_{SD}$	Thermal Shutdown	Temperature Rising		145		$^{\circ}\text{C}$
$\Delta T_{SD}$	Thermal Shutdown Hysteresis			30		$^{\circ}\text{C}$

## Typical Performance Characteristics

Operating Conditions:  $T_A=25^{\circ}\text{C}$ ,  $C_{IN}=100\mu\text{F}$ ,  $C_{OUT}=220\mu\text{F}$ ,  $L=47\mu\text{H}$ , unless otherwise specified.



## Pin Functions

**FB (Pin 1):** Feedback Pin. Receive the feedback voltage from an external resistive divider across the output. In the adjustable version, the output voltage is fixed. The Output voltage is set by R2 and R3:

$$V_{OUT} = 1.21V \cdot [1 + (R2/R3)].$$

**RT (Pin 2):** The internal oscillator is set with a single resistor between this pin and the GND pin.

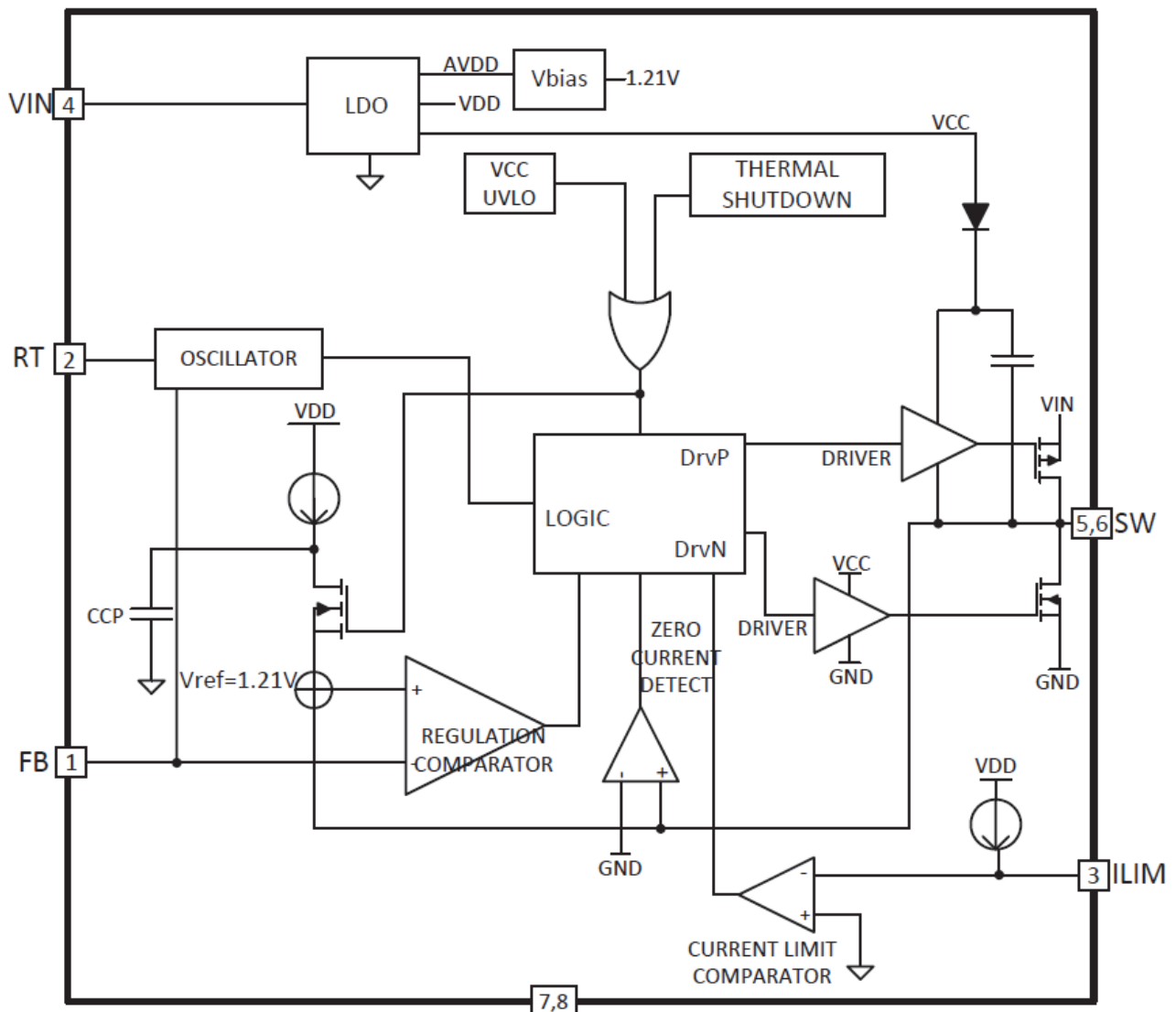
**ILIM (Pin 3):** Monitors current through the low-side switch and triggers current limit operation if the inductor valley current exceeds a user defined value that is set by  $R_{LIM}$  and the Sense current sourced out of this pin during operation.

**VIN (Pin 4):** Main Supply Pin. The PTFI  $\hat{H}\hat{O}$  operates from 8V to 30V unregulated input. It must be closely decoupled to GND, with a 100 $\mu$ F or greater ceramic capacitor to prevent large voltage spikes from appearing at the input.

**SW (Pin 5, 6):** Switch Node Connection to Inductor.

**GND (Pin 7, 8):** Ground Pin.

## Block Diagram



## Application Information

The PTFI Ĥ operates by a constant frequency, current mode architecture. The output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 1.21V and adjusts the peak inductor current accordingly.

During normal operation, the internal P-channel MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, resets the RS latch. While the P-channel MOSFET is off, the N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator or the beginning of the next clock cycle.

### Thermal Protection

The total power dissipation in ĤPTFI Ĥ is limited by a thermal protection circuit. When the device temperature rises to approximately 145°C, this circuit turns off the output, allowing the IC to cool. The thermal protection circuit can protect the device from being damaged by overheating in the event of fault conditions. Continuously running the HTFI Ĥ into thermal shutdown degrades device reliability.

### Current Limit

Current limit detection occurs during the off-time by monitoring the current through the low-side switch using an external resistor,  $R_{LIM}$ . The current limit value is defined by  $R_{LIM}$ . If during the off-time the current in the low-side switch exceeds the user defined current limit value, the next on-time cycle is immediately terminated. Current sensing is achieved by comparing the voltage across the low side FET with the voltage across the current limit set resistor  $R_{LIM}$ . For example, the current limit value is 3.0A by the  $R_{LIM} = 68k$ . The current limit value rises when the set resistor  $R_{LIM}$  rises. The maximum output current is set by  $R_{LIM}$ :  $R_{LIM} (k\Omega) = 22 \cdot I_{MAX} (A)$ .

### Oscillator Frequency

The PTFI Ĥ oscillator frequency is set by a single external resistor connected between the RT pin and the GND pin. The resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND). An internal amplifier holds the RT pin at a fixed voltage typically 0.6V. The oscillator frequency rises when the re-

sistor  $R_T$  falls. To determine the timing resistance for a given switching frequency, use the equation below:

$$R_T(k\Omega) = [6500/f_{osc}(kHz)]^2$$

### Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. For most applications, a resistor in the 10kΩ to 1MΩ range is suggested for R3. R2 is then given by:

$$R2 = R3 \cdot [(V_{OUT} / V_{REF}) - 1]$$

where  $V_{REF}$  is 1.21V.

### Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the PTFI Ĥ integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Choose the proper feedback resistance values for cable compensation refer to the curve in Figure 1. The delta  $V_{OUT}$  voltage rises when the feedback resistance R3 value rises. The delta  $V_{OUT}$  voltage rises when the feedback resistance R3 value rises, use the equation below:

$$\Delta V_{OUT}(V) = R3(k\Omega) \cdot I_{OUT}(A)/1100$$

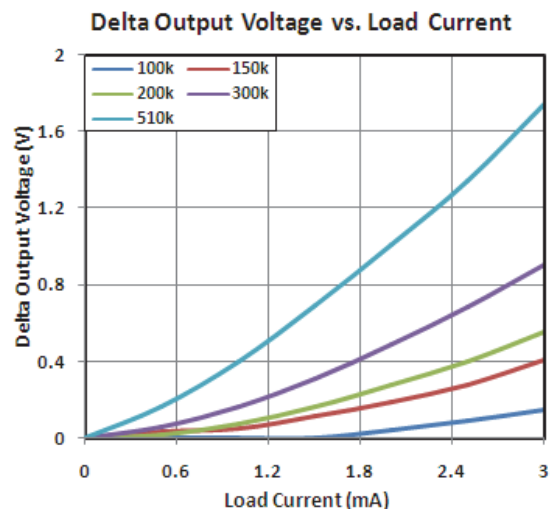


Figure 1. Delta Output Voltage vs. Load Current

## Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7µH to 47µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current and value inductors result in higher ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is  $\Delta I_L = 1120\text{mA}$  (40% of 2.8A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 3.92A rated inductor should be enough for most applications (2.8A + 1120mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the PT FI Ì HÔ requires to operate.

## Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN \text{ required}} I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature

than required. Always consult the manufacturer if there is any question.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume.

## Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses:  $V_{IN}$  quiescent current and  $I^2R$  losses. The  $V_{IN}$  quiescent current loss dominates the efficiency loss at very low load currents whereas the  $I^2R$  loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The  $V_{IN}$  quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET



Each time the gate is switched from high to low to high again, a packet of charge  $\Delta Q$  moves from  $V_{IN}$  to ground. The resulting  $\Delta Q/\Delta t$  is the current out of  $V_{IN}$  that is typically larger than the DC bias current. In continuous mode,  $I_{GATECHG} = f(Q_T + Q_B)$  where  $Q_T$  and  $Q_B$  are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to  $V_{IN}$  and thus their effects will be more pronounced at higher supply voltages.

2.  $I^2R$  losses are calculated from the resistances of the internal switches,  $R_{SW}$  and external inductor  $R_L$ . In continuous mode the average output current flowing through inductor  $L$  is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET  $R_{DS(ON)}$  and the duty cycle (DC) as follows:  $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ . The  $R_{DS(ON)}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses, simply add  $R_{SW}$  to  $R_L$  and multiply the result by the square of the average output current.

Other losses including  $C_{IN}$  and  $C_{OUT}$  ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

### Board Layout Suggestions

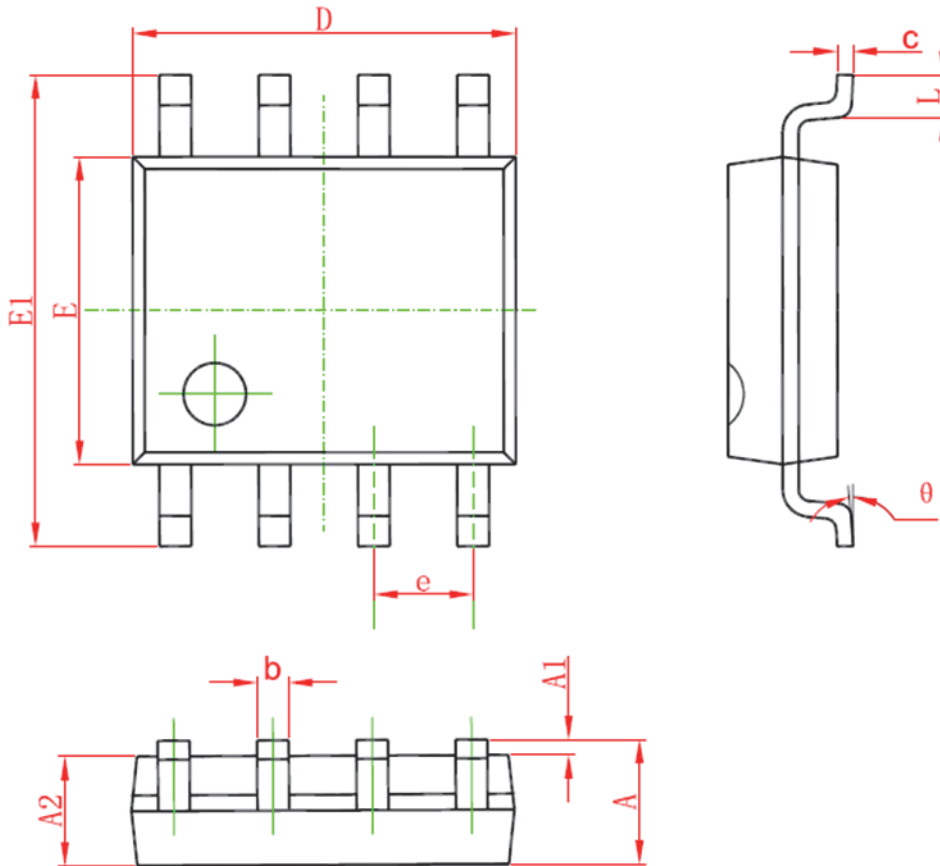
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the PT FI Ĩ HŌ. Check the following in your layout.

1. The power traces, consisting of the GND trace, the SW trace and the  $V_{IN}$  trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins ( $V_{IN}$  and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.



## Packaging Information

### SOP-8L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

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