GENERAL DESCRIPTION

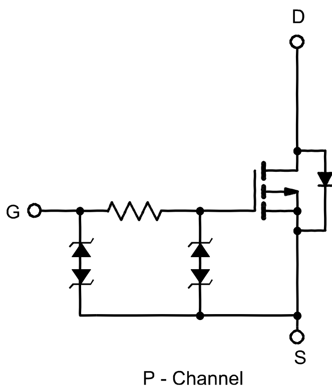
The PT GH€FÖ is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

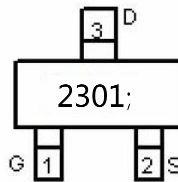
- $R_{DS(ON)}$= 0.48Ω @V_{GS}=-4.5V
- $R_{DS(ON)}$= 0.67Ω @V_{GS}=-2.5V
- $R_{DS(ON)}$= 0.95Ω @V_{GS}=-1.8V
- $R_{DS(ON)}$= 2.20Ω @V_{GS}=-1.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System



P - Channel



Marking and pin Assignment

SOT-23 top view

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±6	V

Electrical Characteristics (T_J =25℃ Unless Otherwise Specified)

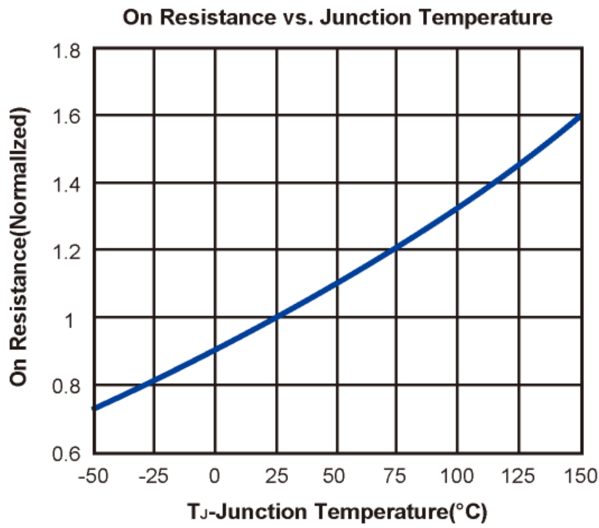
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.45		-1.2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±4.5V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=-4.5V, I_D=-780mA		0.35	0.48	Ω
		V_{GS}=-2.5V, I_D=-660mA		0.44	0.67	
		V_{GS}=-1.8V, I_D=-100mA		0.55	0.95	
		V_{GS}=-1.5V, I_D=-100mA		0.78	2.20	
V_{SD}	Diode Forward Voltage	I_S=-350mA, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
C_{iss}	Input Capacitance	V_{DS}=-16V, V_{GS}=0V, f=1MHZ		152		pF
C_{oss}	Output Capacitance			18.5		
C_{rss}	Reverse Transfer Capacitance			6		
Q_g	Total Gate Charge	V_{DS}=-16V, V_{GS}=-4.5V, I_D=-200mA		2.8		nC
Q_{gs}	Gate-Source Charge			2.1		
Q_{gd}	Gate-Drain Charge			0.5		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V, R_L =50Ω V_{GEN}=-5V,R_G=10Ω I_D=-200mA		51.3		ns
t_r	Turn-On Rise Time			24.2		
$t_{d(off)}$	Turn-Off Delay Time			246		
t_f	Turn-Off Fall Time			81.2		

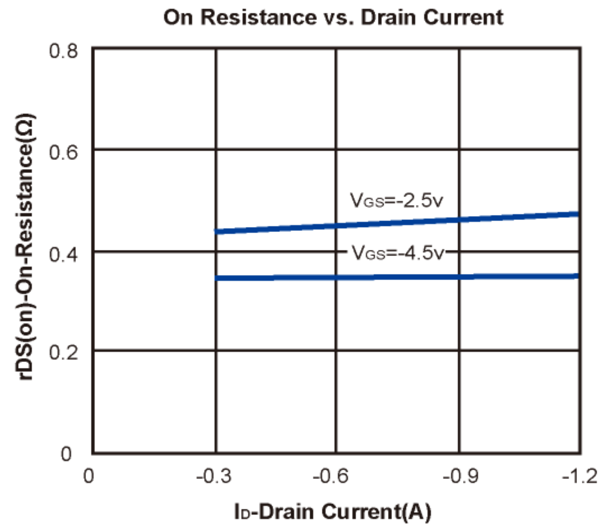
Notes: a. Based on Eutectic paste and bond wire Cu wire 1mil×1(S), Cu wire 1mil×1(G) on each die of SOT-523 package.

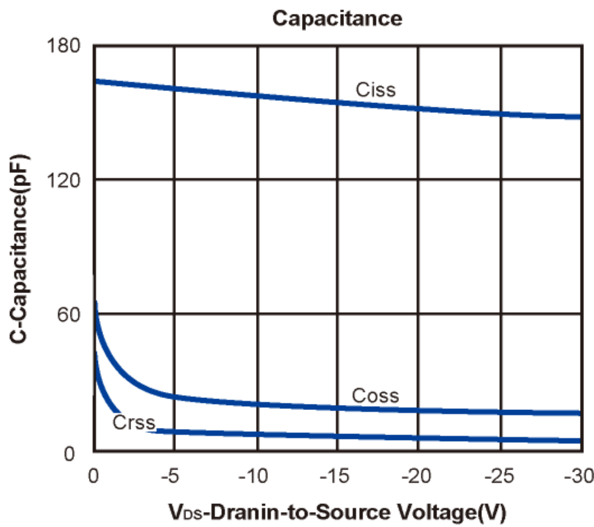
b. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%.

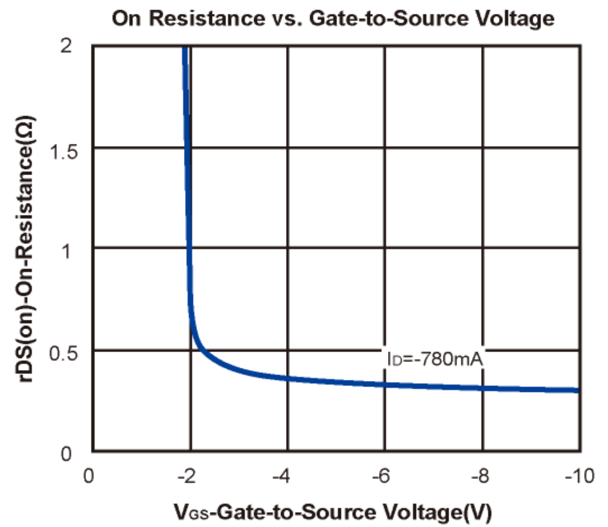
c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

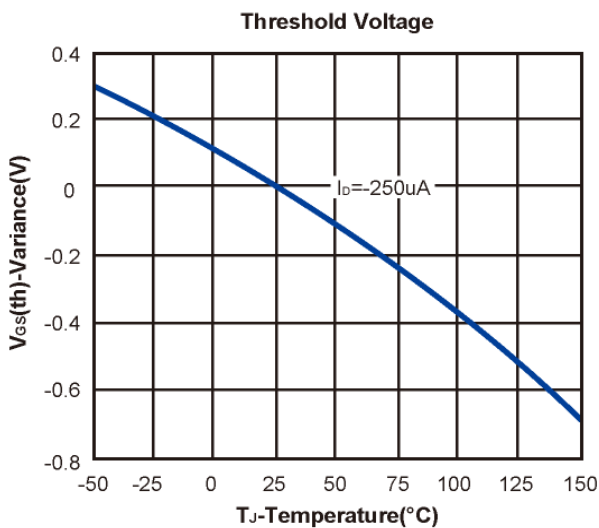
Typical Characteristics (TJ =25℃ Noted)

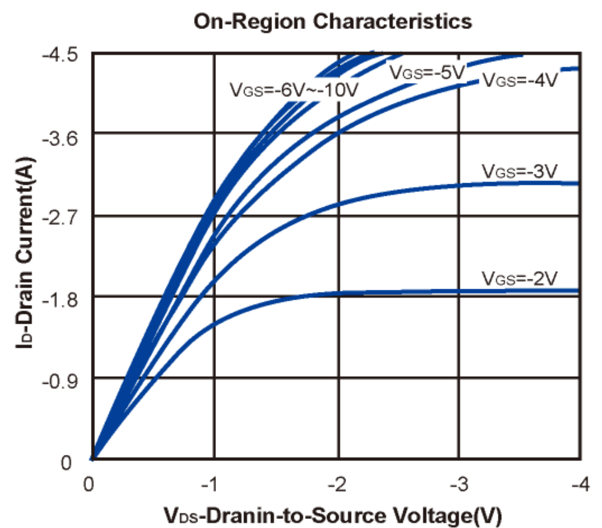




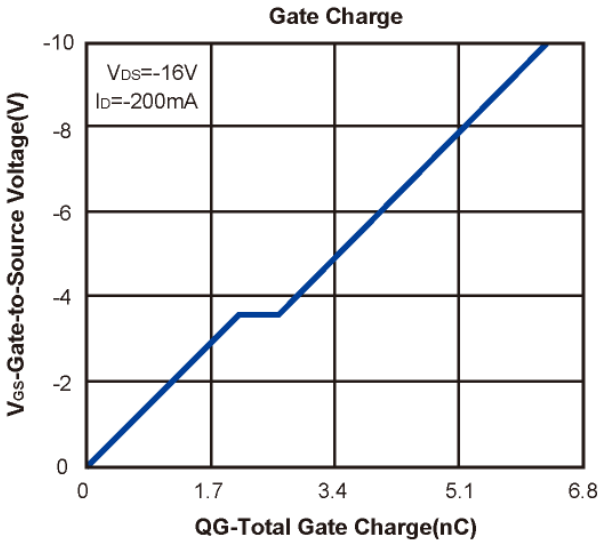


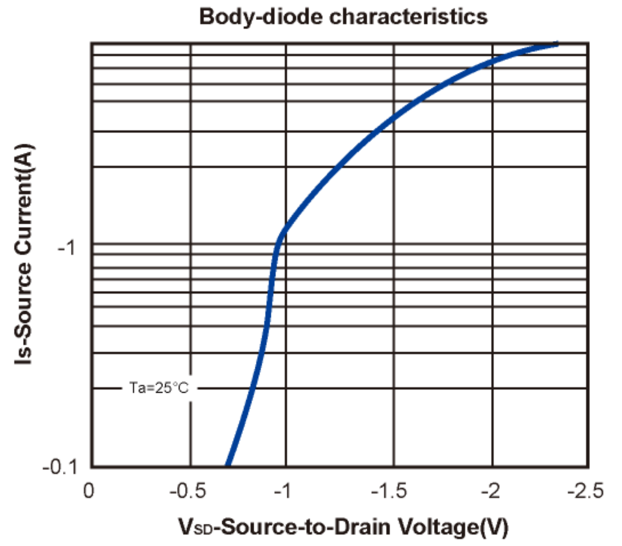






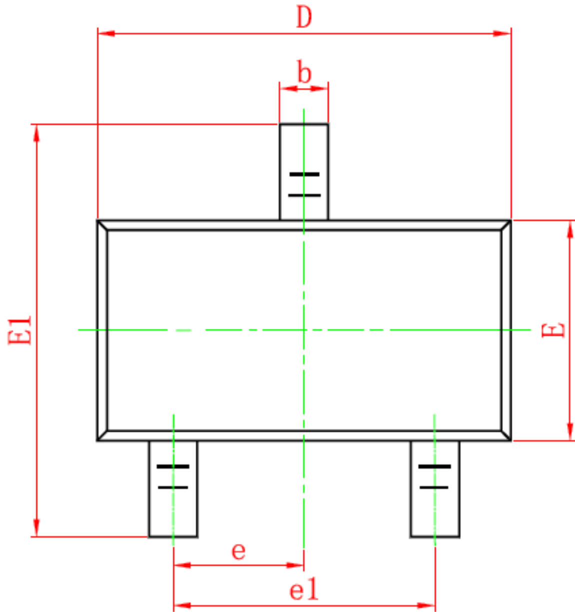
Typical Characteristics (TJ =25℃ Noted)

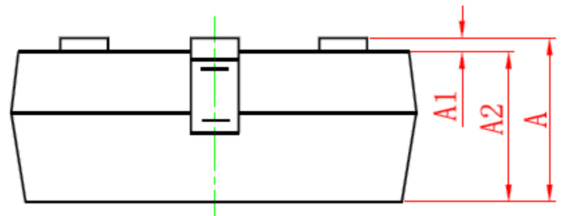


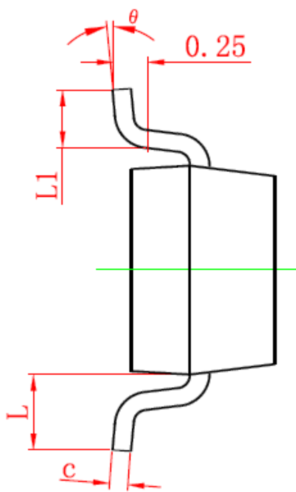


SOT-23 PACKAGE INFORMATION

Dimensions in Millimeters (UNIT:mm)







Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.