

GENERAL DESCRIPTION

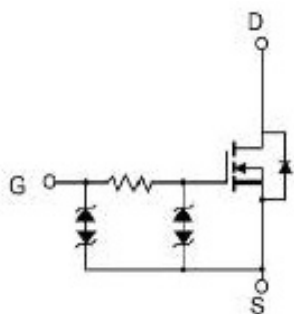
The HM2302D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

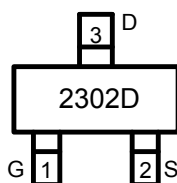
- $R_{DS(ON)} = 270 \text{ m}\Omega @ V_{GS}=4.5\text{V}$
- $R_{DS(ON)} = 330 \text{ m}\Omega @ V_{GS}=2.5\text{V}$
- $R_{DS(ON)} = 450 \text{ m}\Omega @ V_{GS}=1.8\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch



N-Channel



Marking and pin Assignment



SOT-23 top view

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V

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Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	V

Electrical Characteristics (T_j=25°C Unless Otherwise Specified)

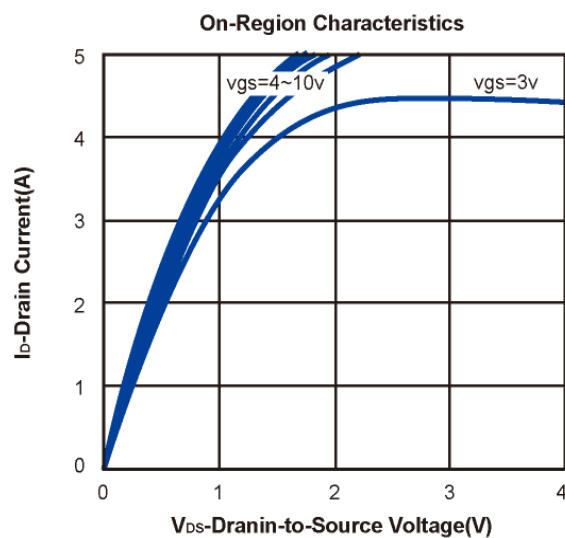
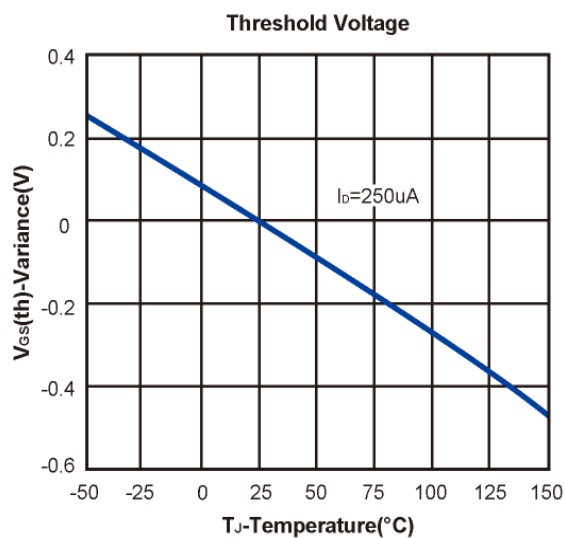
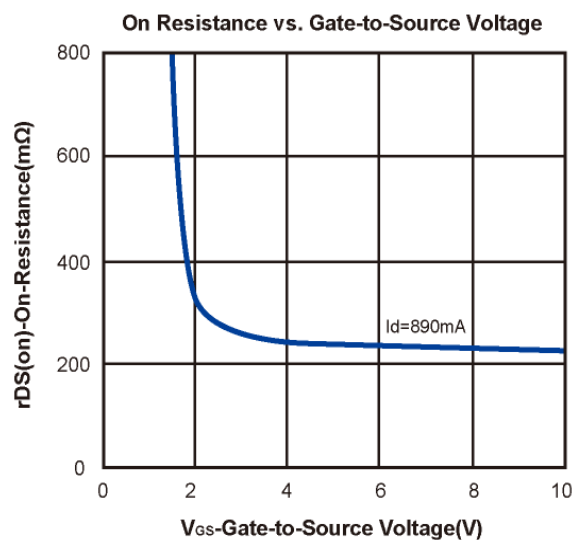
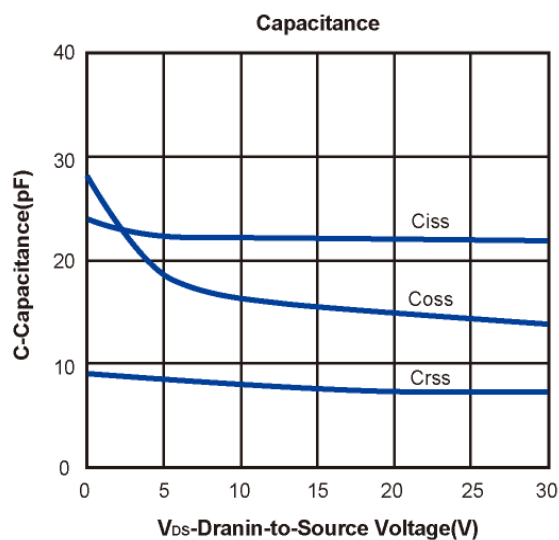
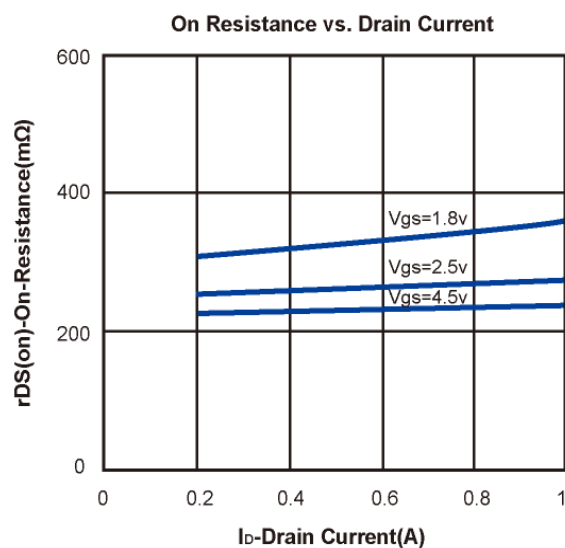
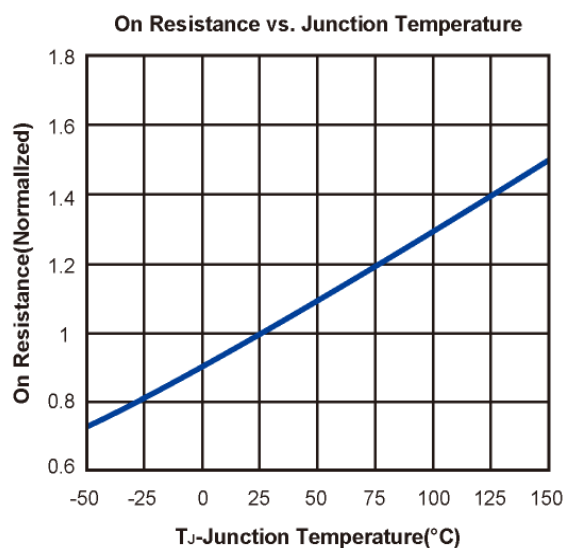
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.45		1.2	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±8V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =4.5V, I _D =890mA		220	270	mΩ
		V _{GS} =2.5V, I _D =780mA		260	330	
		V _{GS} =1.8V, I _D =700mA		330	450	
V _{SD}	Diode Forward Voltage	I _S =350mA, V _{GS} =0V		0.75	1.2	V
DYNAMIC						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHZ		21		pF
C _{oss}	Output Capacitance			15		
C _{rss}	Reverse Transfer Capacitance			8		
Q _g	Total Gate Charge	V _{DS} =25V, V _{GS} =10V, I _D =0.22A		6.7		nC
Q _{gs}	Gate-Source Charge			1.2		
Q _{gd}	Gate-Drain Charge			0.9		
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, R _L =3Ω V _{GEN} =10V, R _G =10Ω		120		ns
t _r	Turn-On Rise Time			317		
t _{d(off)}	Turn-Off Delay Time			748		
t _f	Turn-Off Fall Time			716		

Notes: a. Based on epoxy or solder paste and bond wire Cu wire 1mil×1(S), Cu wire 1mil×1(G) on each die of SOT-523 package.

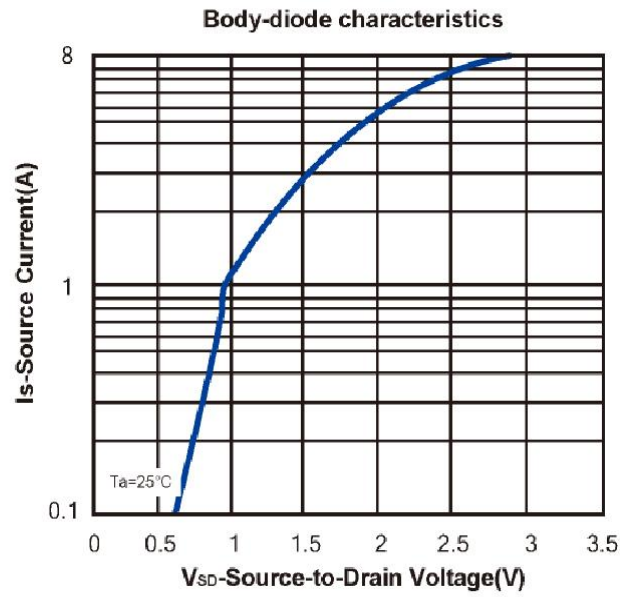
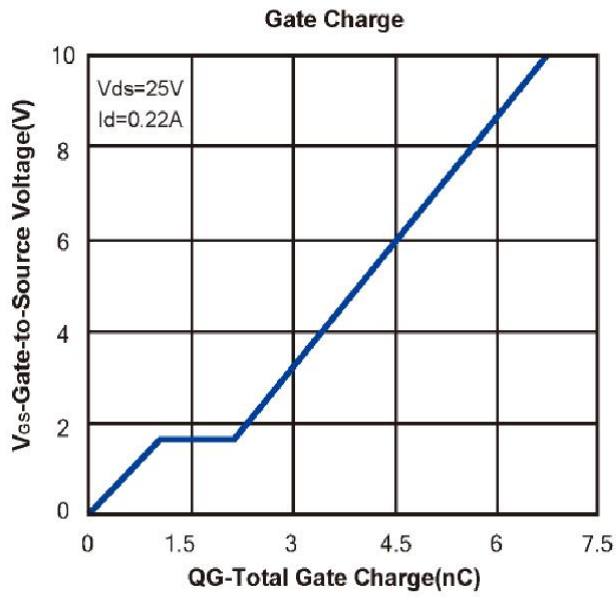
b. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%.

c. Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J =25°C Noted)

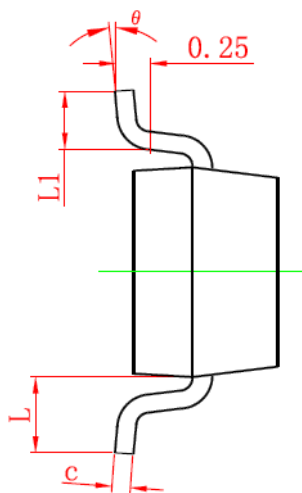
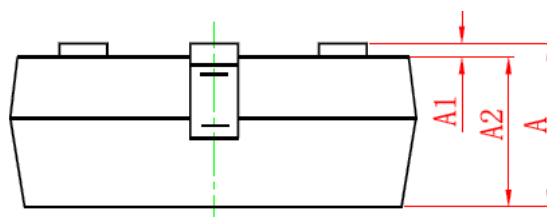
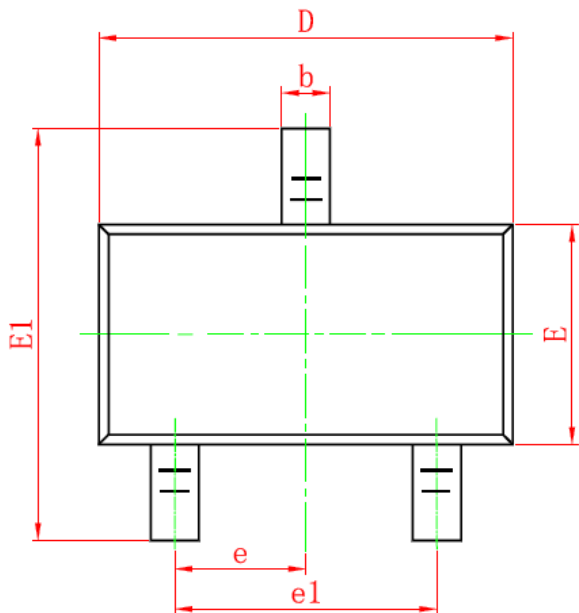


Typical Characteristics (T_J =25°C Noted)



SOT-23 PACKAGE INFORMATION

Dimensions in Millimeters (UNIT:mm)



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.