虹美功率半导体
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HM2318D

N-Channel 40V(D-S) MOSFET

GENERAL DESCRIPTION

The HM2318D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

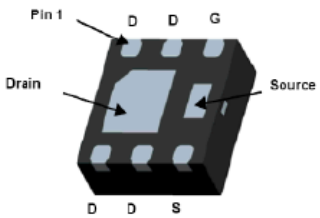
- $R_{DS(ON)}$ ≦40mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦65mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

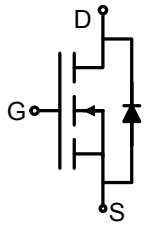
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V



DFN2X2-6L bottom view



Schematic diagram

N-Channel 40V(D-S) MOSFET

Electrical Characteristics (T_j =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D= 6.0A		32	40	mΩ
		V_{GS}=4.5V, I_D= 3.5A		50	65	
V_{SD}	Diode Forward Voltage	I_S=1A		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_D=6A		16		nC
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_D=6A		8.2		
Qgs	Gate-Source Charge			3.6		
Qgd	Gate-Drain Charge			3.9		
Ciss	Input capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz		560		pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			22		
Rg	Gate Resistance	f =1MHz		0.7		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=20V, R_L =20Ω I_D=1A, V_{GEN}=10V R_G=1Ω		12		ns
t_r	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			37		
t_f	Turn-Off Fall Time			4		

Notes: a. Based on epoxy or solder paste and bond wire Cu 2mil×3(S), Au 1mil ×1(G) on each die of SOT-23 package.

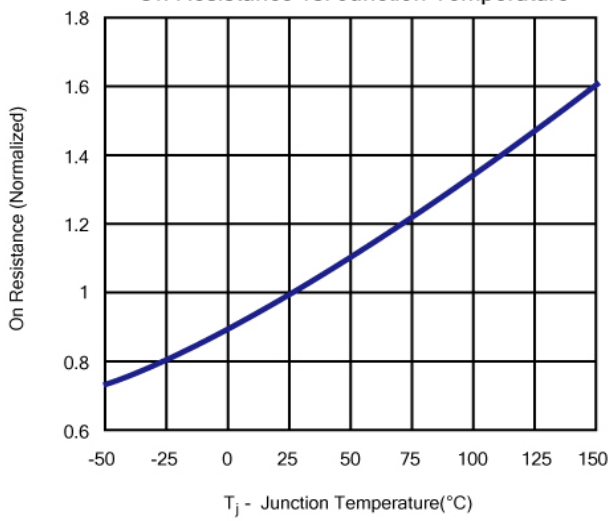
b. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%.

c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

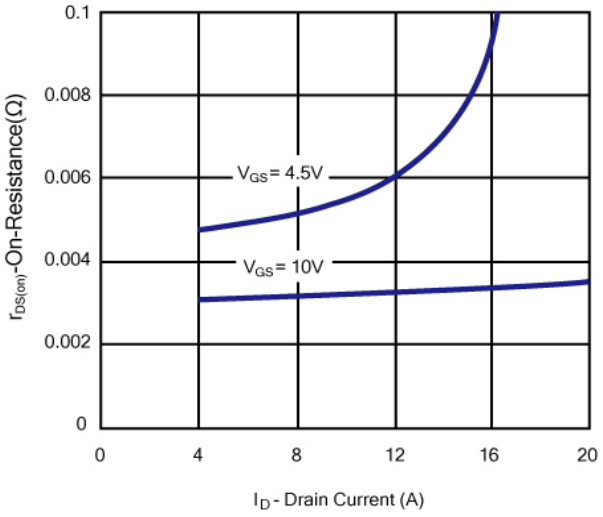
Typical Characteristics (T_J =25℃ Noted)

N-Channel 40V(D-S) MOSFET

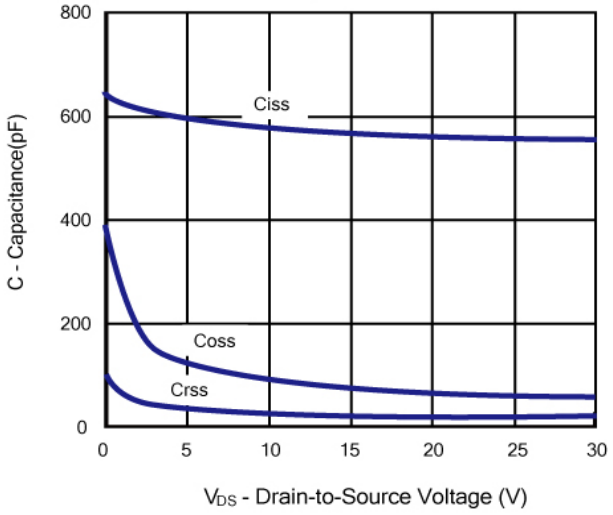
On Resistance vs. Junction Temperature



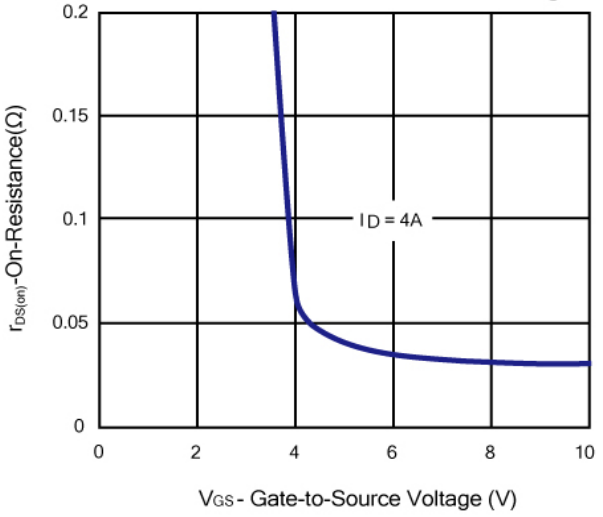
On-Resistance vs. Drain Current



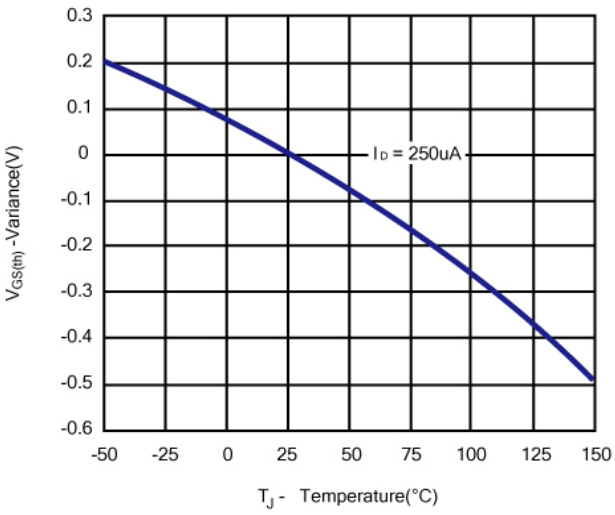
Capacitance



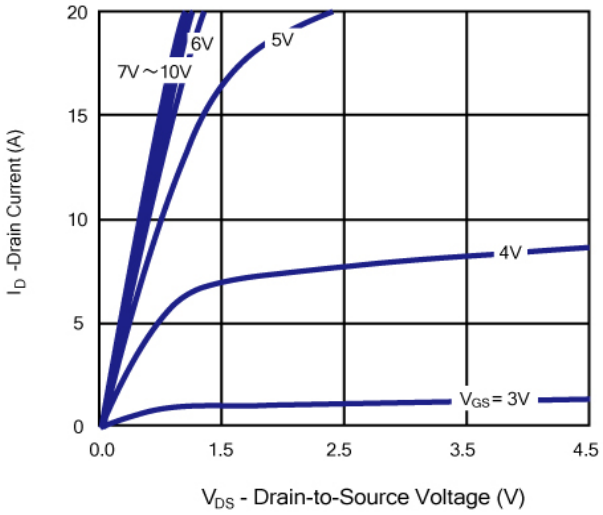
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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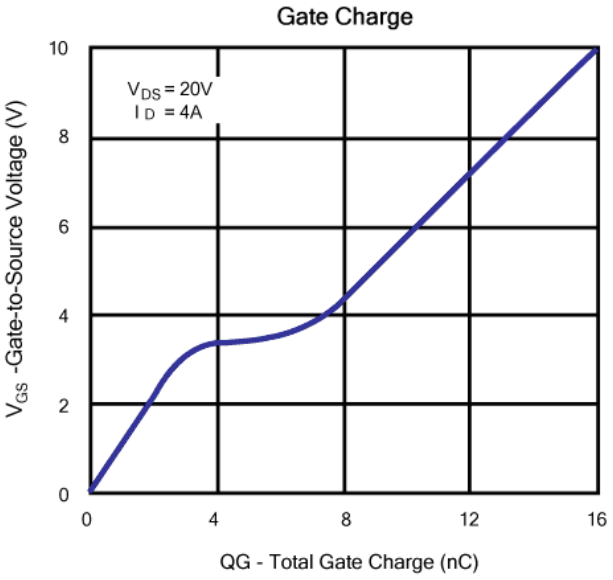
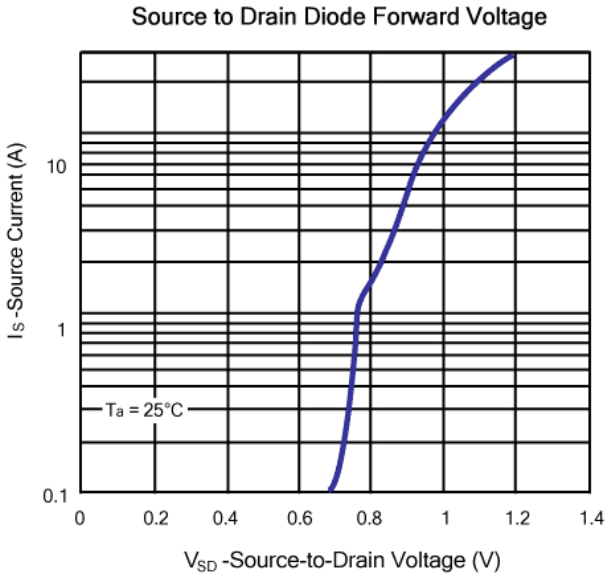
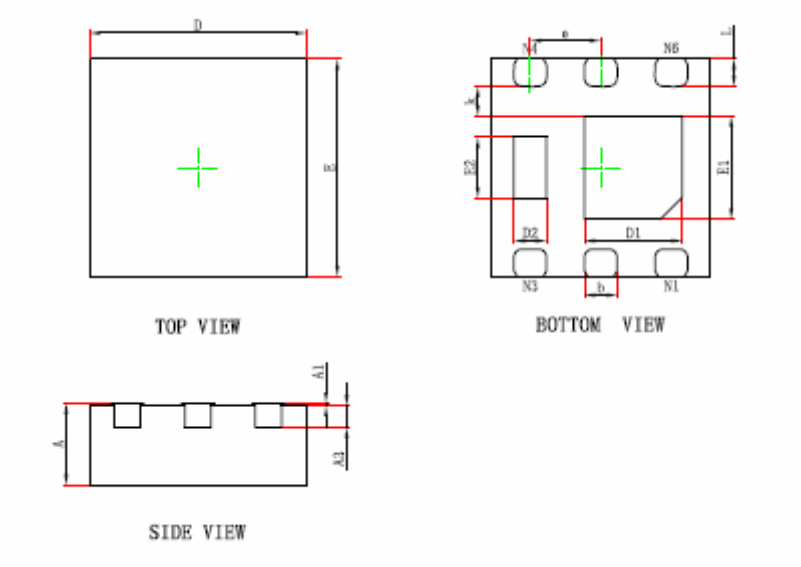




DFN2X2-6L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	0.800	1.000	0.031	0.039
E1	0.850	1.050	0.033	0.041
D2	0.200	0.400	0.008	0.016
E2	0.460	0.660	0.018	0.026
k	0.200MIN.		0.008MIN.	
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
L	0.174	0.326	0.007	0.013

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.