

250V N-Channel Enhancement Mode MOSFET

Description

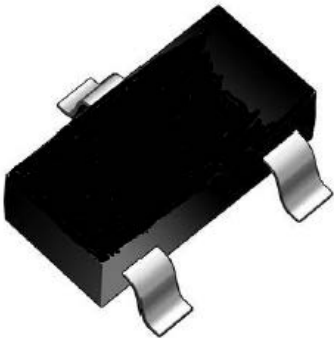
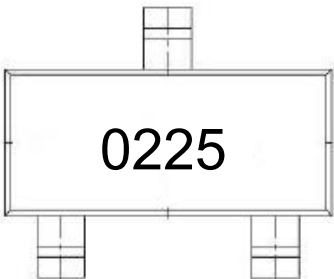
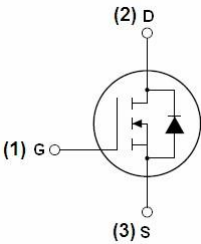
The HM2N25MR uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 250V, I_D = 2A$
- $R_{DS(ON)} < 1500m\Omega @ V_{GS}=10V$ (Typ:1300m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HM2N25MR	SOT23-3	0225	3000

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	2	A
Drain Current-Pulsed (Note 1)	I_{DM}	10	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	41.7	$^{\circ}C/W$



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	250	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=250V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5		3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=2A$	-	1300	1500	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=2A$	-	8	-	S
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	580	-	PF
Output Capacitance	C_{oss}		-	90	-	PF
Reverse Transfer Capacitance	C_{rss}		-	3	-	PF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	10	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$V_{DS}=100V, I_D=2A,$ $V_{GS}=10V$	-	12		nC
Gate-Source Charge	Q_{gs}		-	2.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3.8	-	nC
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=2A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	2	A

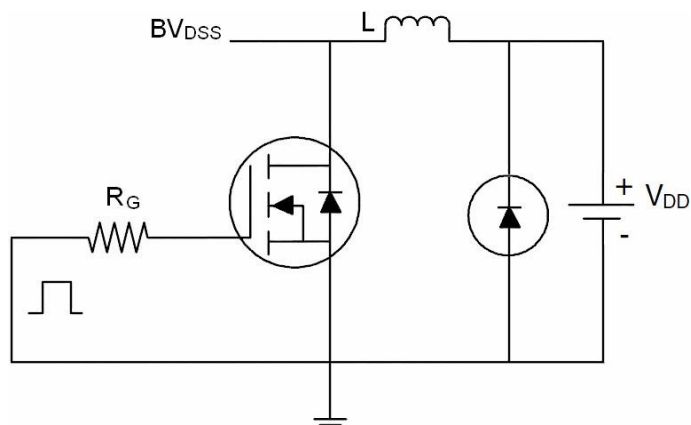
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

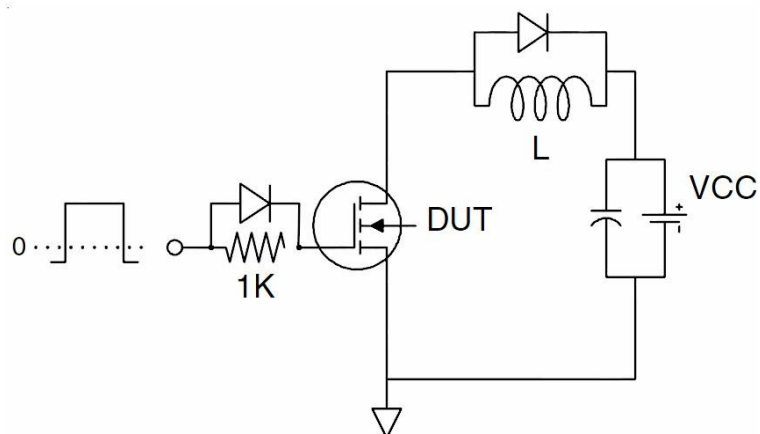
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Test Circuit

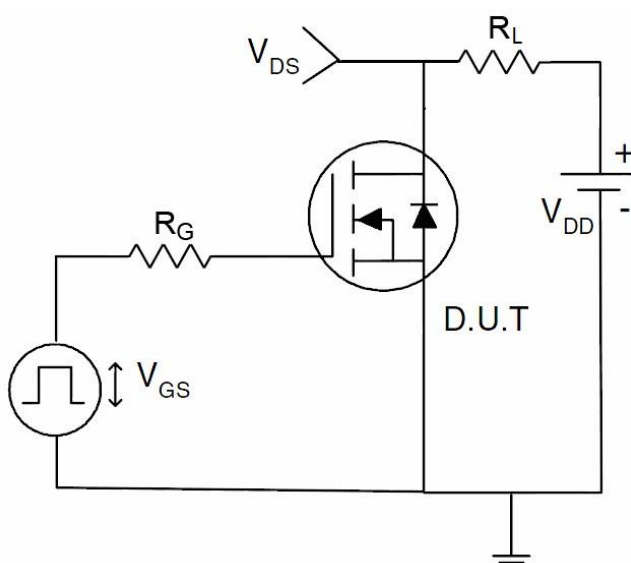
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

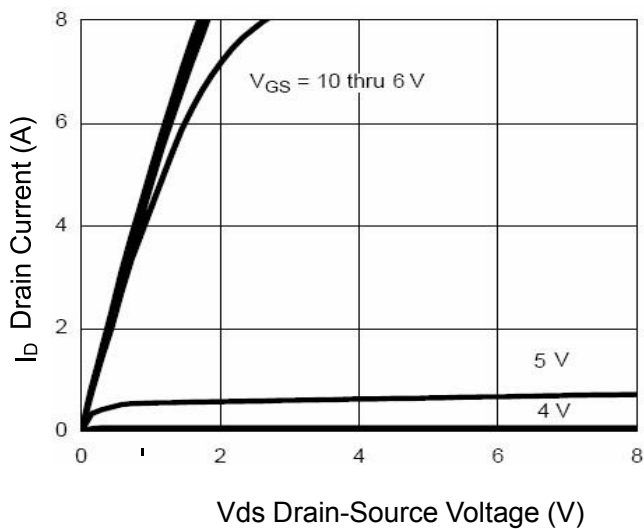


Figure 1 Output Characteristics

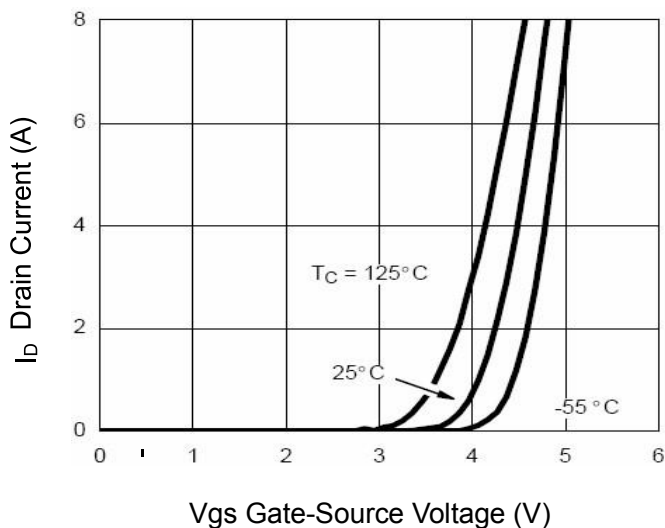


Figure 2 Transfer Characteristics

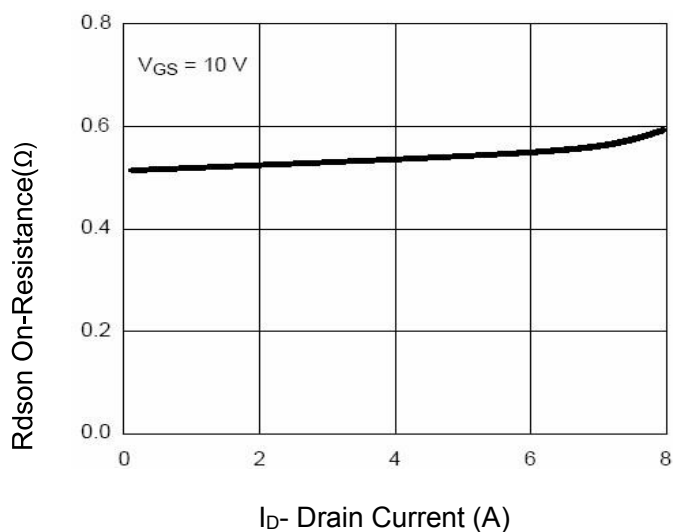


Figure 3 $R_{DS(on)}$ - Drain Current

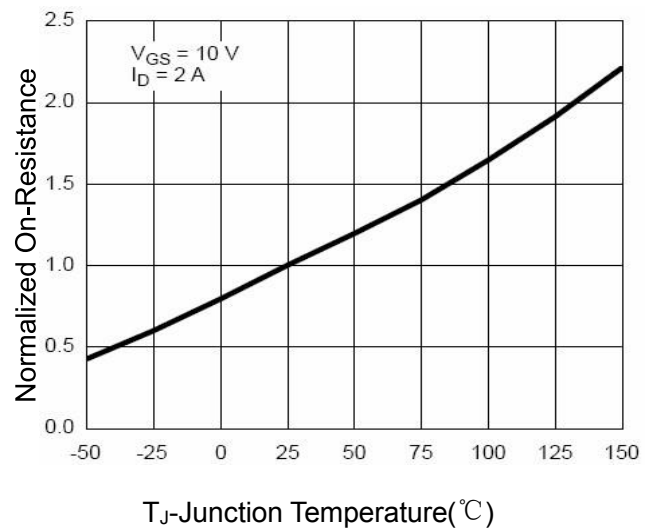


Figure 4 $R_{DS(on)}$ -Junction Temperature

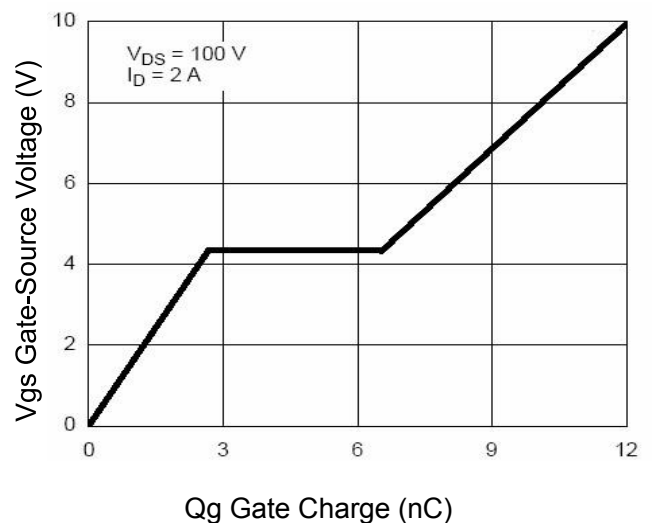


Figure 5 Gate Charge

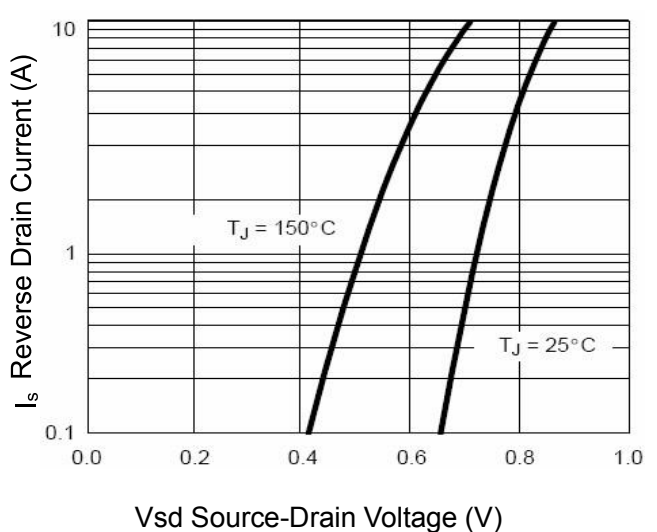
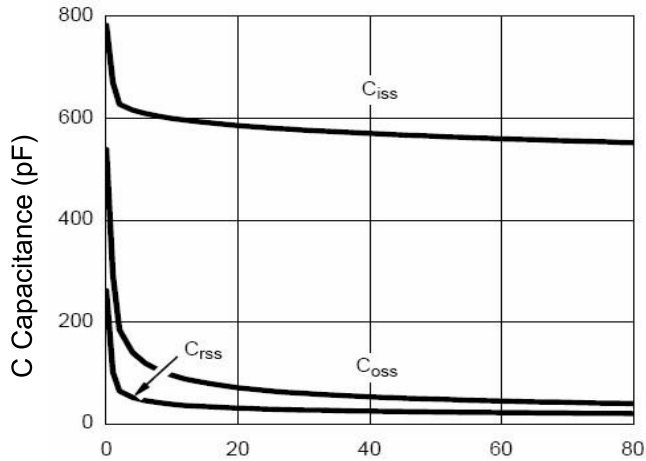
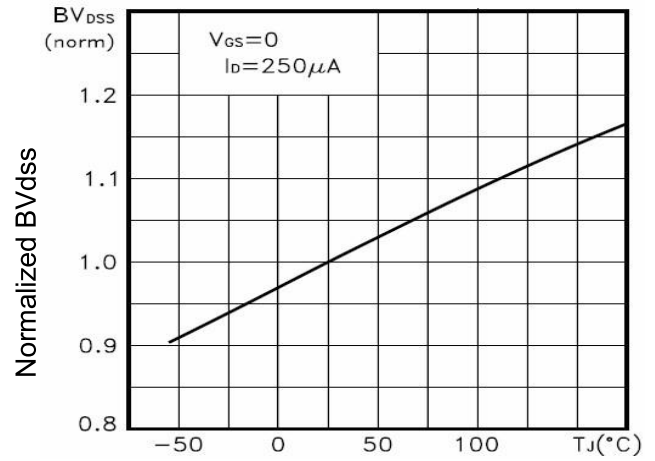


Figure 6 Source- Drain Diode Forward



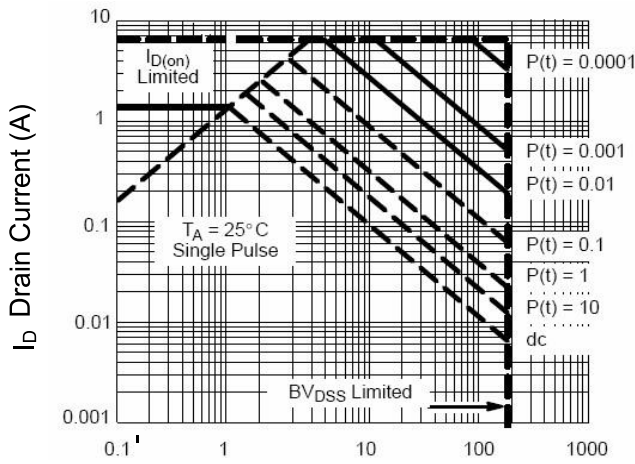
V_{DS} Drain-Source Voltage (V)

Figure 7 Capacitance vs V_{DS}



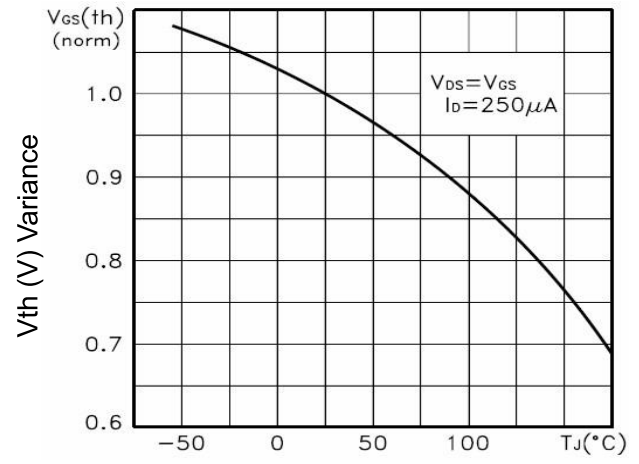
T_J -Junction Temperature($^{\circ}C$)

Figure 9 BV_{DSS} vs Junction Temperature



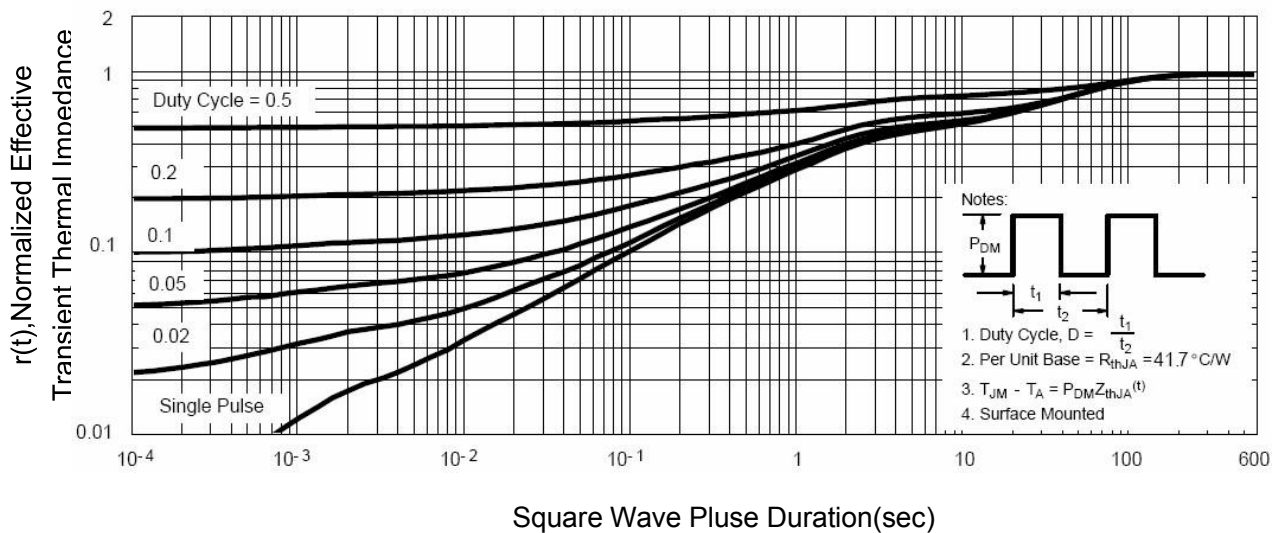
V_{DS} Drain-Source Voltage (V)

Figure 8 Safe Operation Area



T_J -Junction Temperature($^{\circ}C$)

Figure 10 $V_{GS(th)}$ vs Junction Temperature



Square Wave Pulse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

SOT23-3L Package outline

