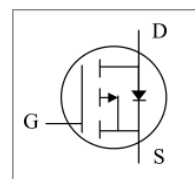


-150V P-Channel Enhancement Mode MOSFET

Description

The HM2P15PR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = -150V$ $I_D = -2.0 A$

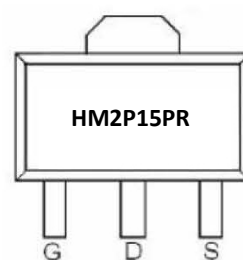
$R_{DS(ON)} < 780m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



SOT-89-3L top view

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HM2P15PR	SOT-89-3L	HM2P15PR	3000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-150	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-2.0	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-1.4	A
I_{DM}	Pulsed Drain Current ²	-6.0	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ³	1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	80	$^\circ\text{C/W}$

-150V P-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-150	---	---	V
$\Delta\text{BVDSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.0624	---	V/ $^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-10\text{V}$, $I_D=-0.8\text{A}$	---	---	780	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-0.4\text{A}$	---	---	980	
VGS(th)	Gate Threshold Voltage		-2.0	---	-4.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=-250\mu\text{A}$	---	4.5	---	mV/ $^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-80\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	10	μA
		$V_{DS}=-80\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	100	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-0.8\text{A}$	---	3	---	S
Rg	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	16	32	Ω
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-15\text{V}$, $V_{GS}=-4.5\text{V}$, $I_D=-0.5\text{A}$	---	4.5	---	nC
Qgs	Gate-Source Charge		---	1.14	---	
Qgd	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-50\text{V}$, $V_{GS}=-10\text{V}$, $R_G=3.3\Omega$, $I_D=-0.5\text{A}$	---	13.6	---	ns
Tr	Rise Time		---	6.8	---	
Td(off)	Turn-Off Delay Time		---	34	---	
Tf	Fall Time		---	3	---	
Ciss	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	553	---	pF
Coss	Output Capacitance		---	29	---	
Crss	Reverse Transfer Capacitance		---	20	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	-0.9	A
ISM	Pulsed Source Current ^{2,4}		---	---	-1.8	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=-1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

-150V P-Channel Enhancement Mode MOSFET

Typical Characteristics

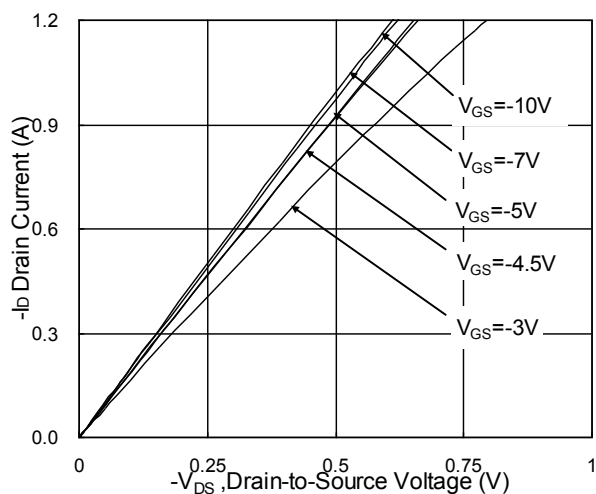


Fig.1 Typical Output Characteristics

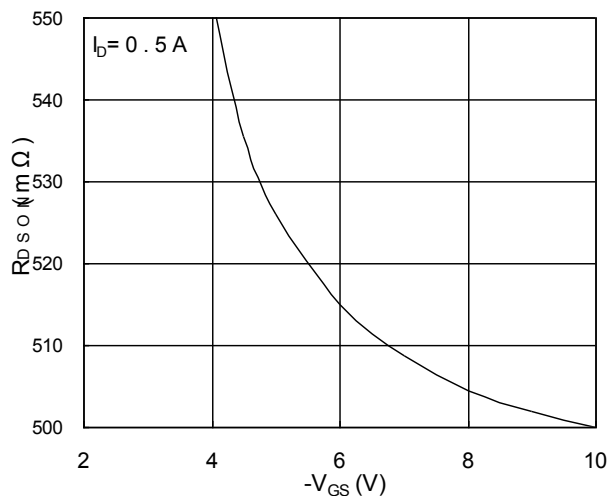


Fig.2 On-Resistance vs. Gate-Source

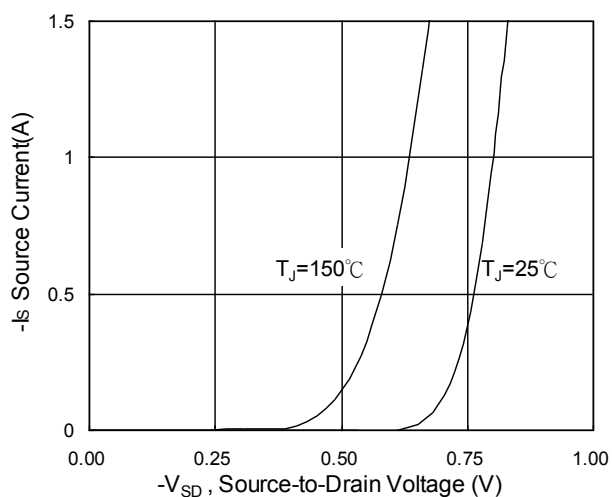


Fig.3 Forward Characteristics Of Reverse

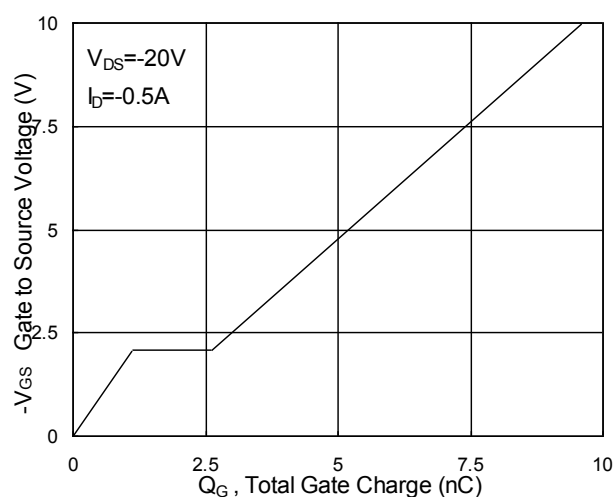


Fig.4 Gate-Charge Characteristics

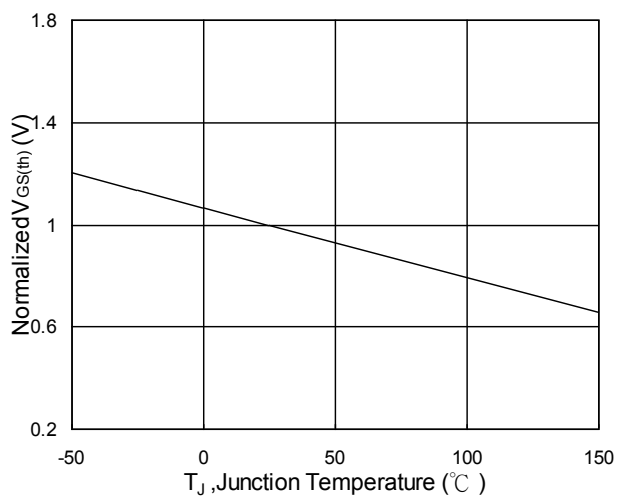


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

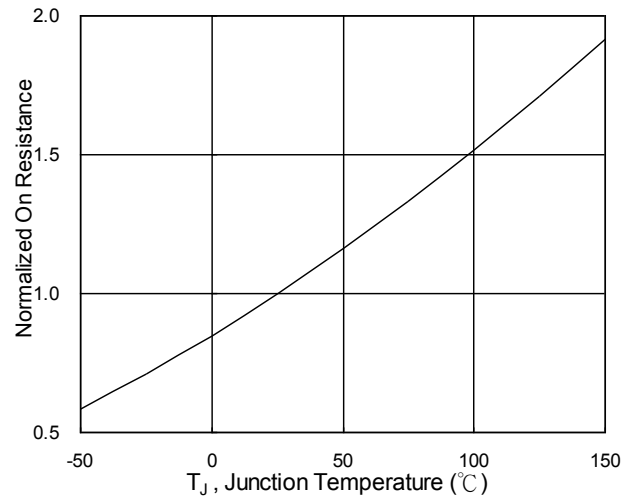


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

-150V P-Channel Enhancement Mode MOSFET

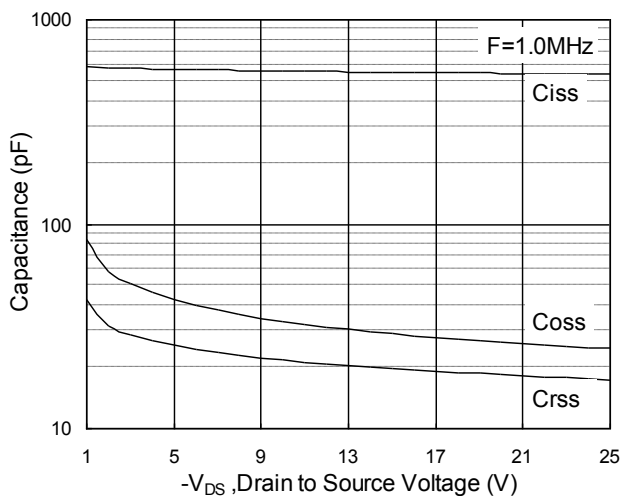


Fig.7 Capacitance

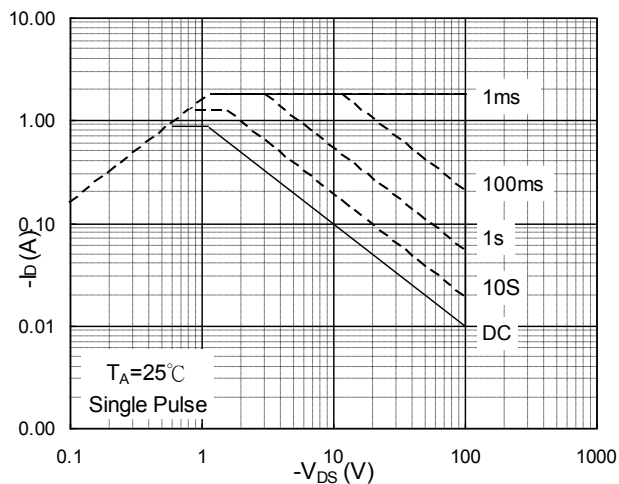


Fig.8 Safe Operating Area

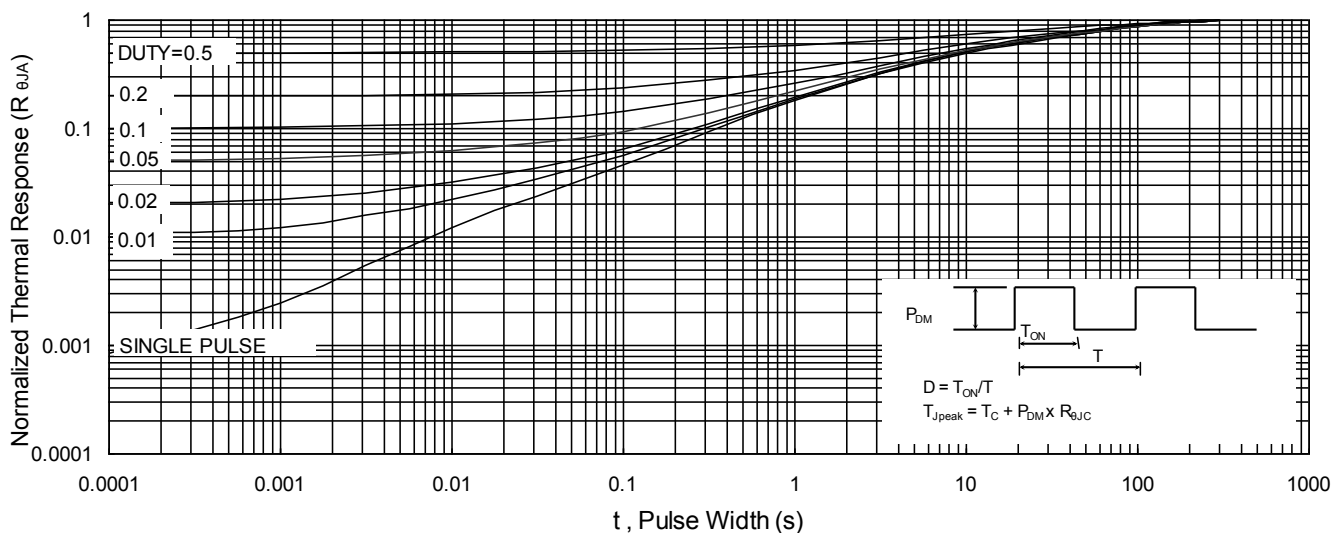


Fig.9 Normalized Maximum Transient Thermal Impedance

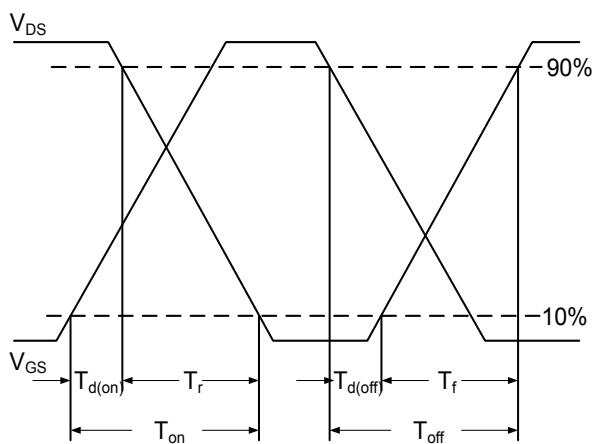


Fig.10 Switching Time Waveform

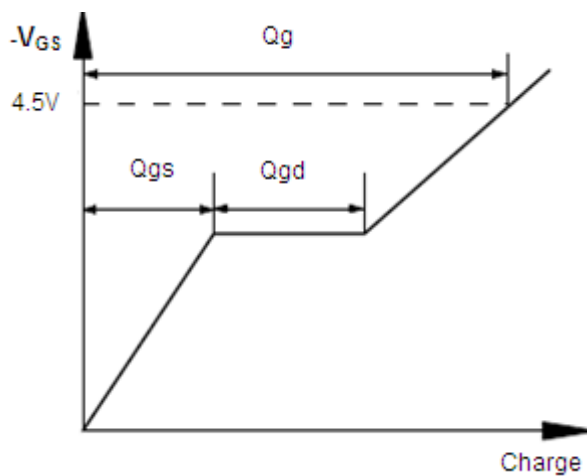
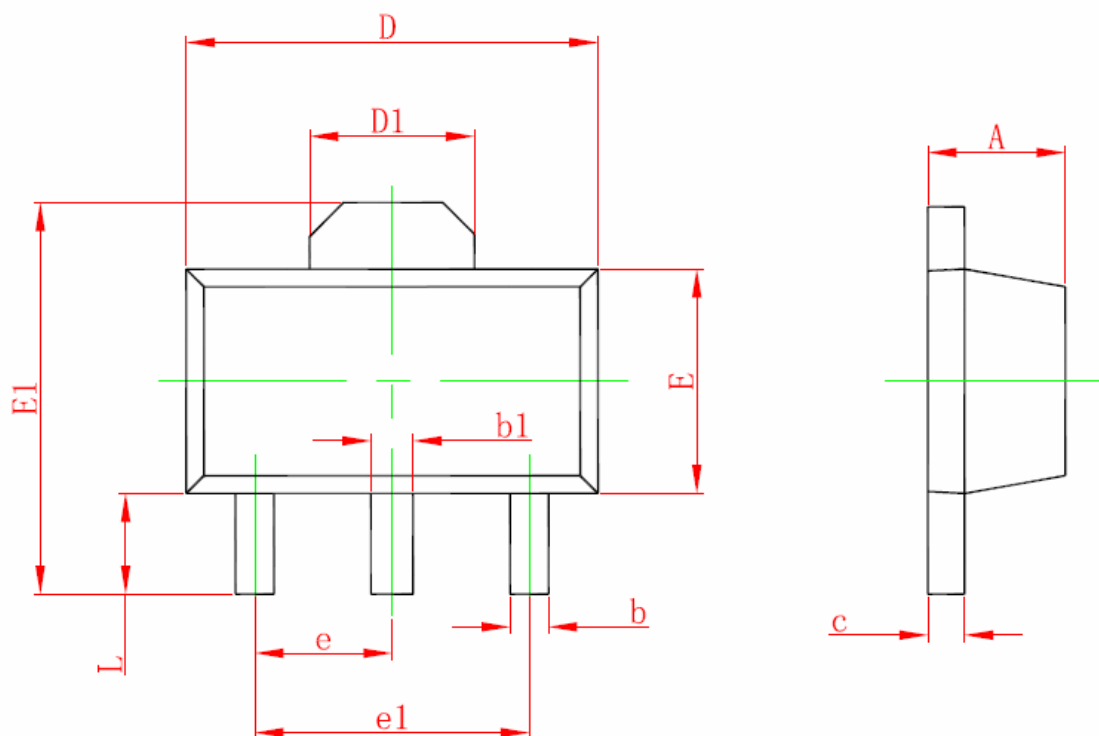


Fig.11 Gate Charge Waveform

SOT-89-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.