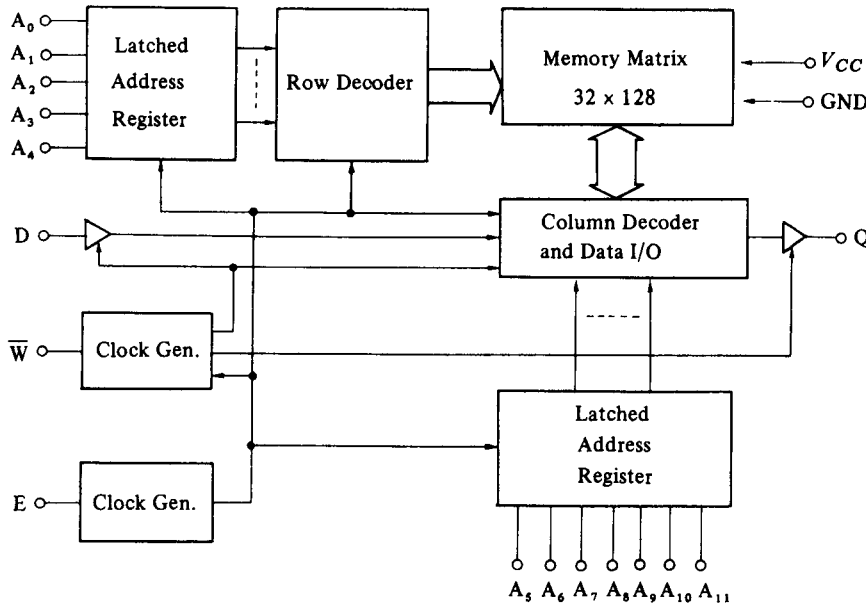
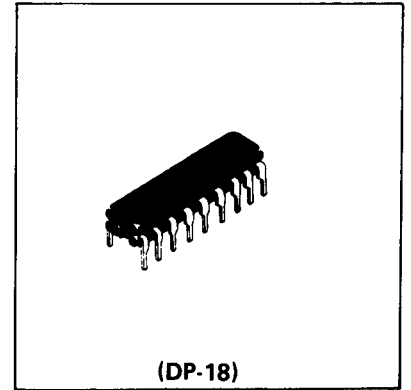


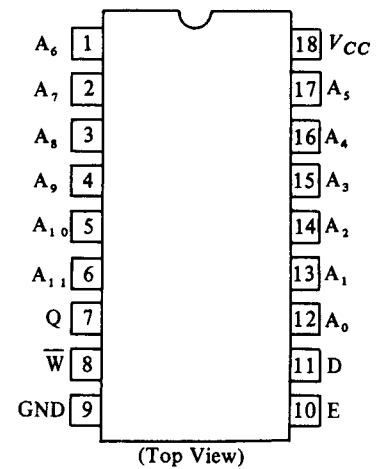
HM4315P

4096-word×1-bit Static Random Access Memory

- Low Power Standby 10μW typ.
- Low Power Operation 20mW typ.
- Data Retention 2.0V
- Fast Access Time 450ns max.
- TTL/CMOS Compatible Input/Output
- On Chip Address Register
- Si Gate CMOS Technology



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|-----------------------|-----------|----------------------|------|
| Supply Voltage* | V_{CC} | -0.3 to +7.0 | V |
| Terminal Voltage* | V_T | -0.3 to $V_{CC}+0.3$ | V |
| Power Dissipation | P_T | 1.0 | W |
| Operating Temperature | T_{opr} | 0 to +70 | °C |
| Storage Temperature | T_{stg} | -55 to +125 | °C |

* with respect to GND

■ RECOMMENDED DC OPERATING CONDITION ($T_a=0$ to +70°C)

| Item | Symbol | min. | typ. | max. | Unit |
|----------------|----------|------|------|--------------|------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | GND | 0 | 0 | 0 | V |
| Input Voltage | V_{IH} | 2.4 | — | $V_{CC}+0.3$ | V |
| | V_{IL} | -0.3 | — | 0.8 | V |

■ DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

| Item | Symbol | Test Condition | min. | typ. | max. | Unit |
|------------------------------|-----------|---|------|------|------|---------------|
| Input Leakage Current | I_{LI} | $V_{IN} = 0 \sim V_{CC}$ | -1.0 | — | 1.0 | μA |
| Output Leakage Current | I_{LO} | $E = V_{IL}$, $V_{out} = 0 \sim V_{CC}$ | -1.0 | — | 1.0 | μA |
| Operating Power | I_{CC1} | $E = V_{CC}$, $V_{IN} = V_{CC}$ or 0V , Output Open | — | — | 1.0 | mA |
| Supply Current | I_{CC2} | $E = 2.4\text{V}$, $V_{IN} = 2.4\text{V}$, Output Open | — | 2.5 | 5.0 | mA |
| Average Power Supply Current | I_{CC3} | $V_{IH} \geq V_{CC} - 0.2\text{V}$, $f = 1\text{MHz}$, duty 50% | — | 4 | 10 | mA |
| | I_{CC4} | $V_{IH} = 2.4\text{V}$, $f = 1\text{MHz}$, duty 50% | — | 6 | 15 | mA |
| Standby Power Supply Current | I_{CCL} | $E \leq 0.2\text{V}$ | — | 2 | 100 | μA |
| Output Voltage | V_{OL} | $I_{OL} = 2.0\text{mA}$ | — | — | 0.4 | V |
| | V_{OH} | $I_{OH} = -1.0\text{mA}$ | 2.4 | — | — | V |

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

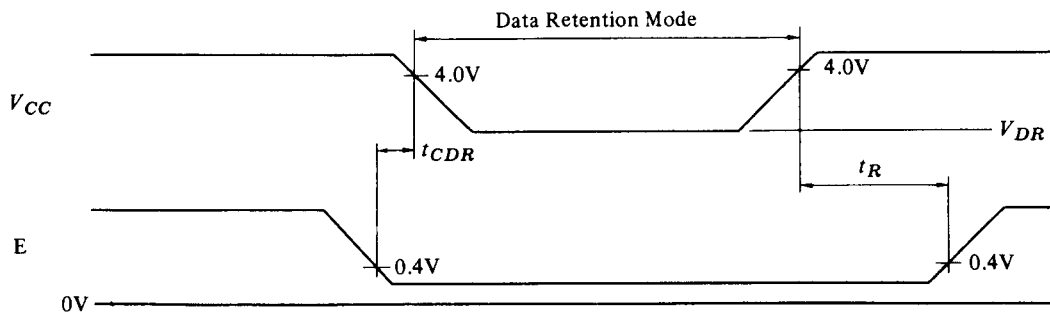
| Item | Symbol | Test Condition | min. | typ. | max. | Unit |
|--------------------|-----------|-----------------------|------|------|------|-------------|
| Input Capacitance | C_{in} | $V_{in} = 0\text{V}$ | — | 3 | 5 | pF |
| Output Capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{V}$ | — | 7 | 10 | pF |

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

| Item | Symbol | Test Condition | min. | typ. | max. | Unit |
|--------------------------------------|------------|---|---------|------|------|---------------|
| V_{CC} for Data Retention | V_{DR} | $E \leq 0.2\text{V}$ | 2.0 | — | — | V |
| Data Retention Power Supply Current | I_{CCDR} | $E \leq 0.2\text{V}$, $V_{DR} = 2.0\text{V}$ | — | 0.5 | 50 | μA |
| Chip Deselect to Data Retention Time | t_{CDR} | | 0 | — | — | ns |
| Operation Recovery Time | t_R | | t_C^* | — | — | ns |

* t_C = Cycle Time

■ LOW V_{CC} DATA RETENTION TIMING



NOTE: All inputs shall be kept below $V_{CC} + 0.3\text{V}$ under any operating conditions.

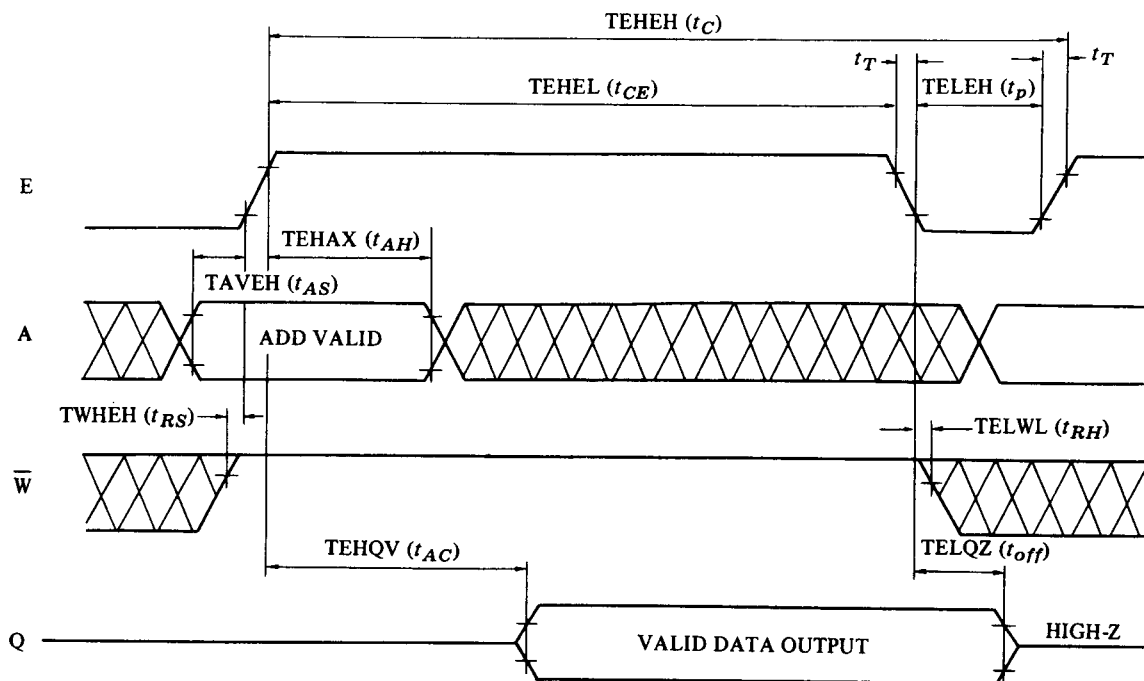
■ AC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

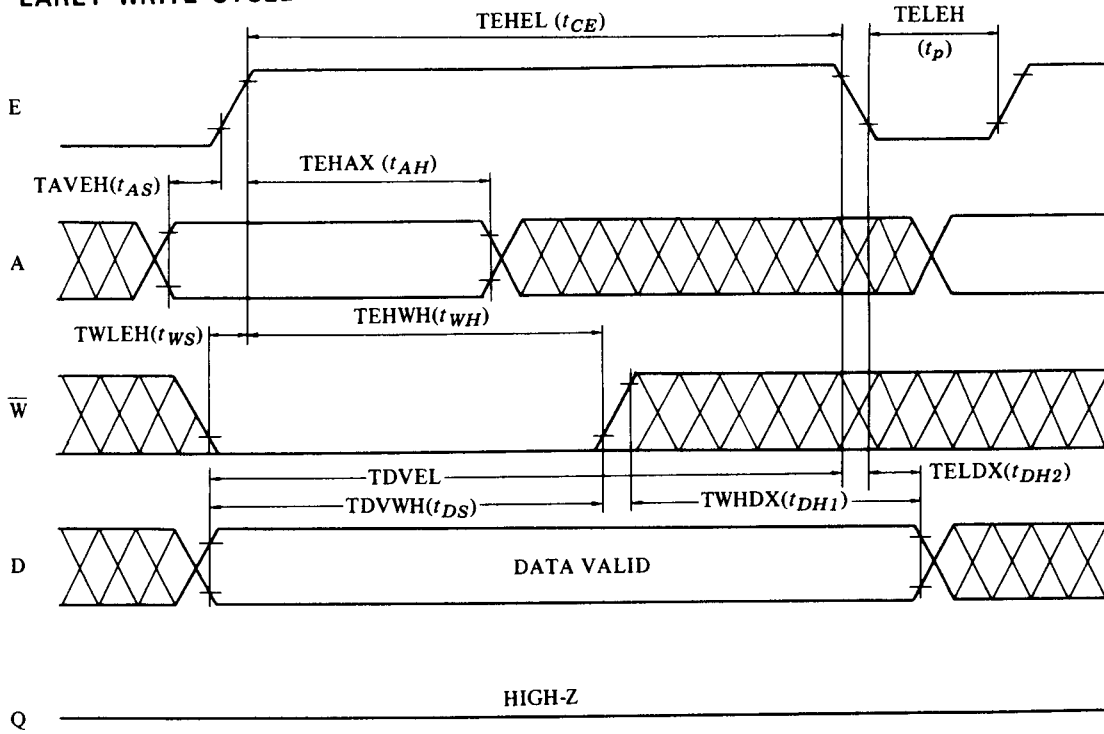
| | |
|---------------------------|-------------------------------|
| Input High Level | 2.4V |
| Input Low Level | 0.8V |
| Input Rise and Fall Times | 20ns |
| Timing Measurement Levels | 2.4V, 0.8V |
| Reference Level | $V_{OH}=2.0V$, $V_{OL}=0.8V$ |
| Output Load | $1TTL+C_L=100pF$ |

| Item | Symbol | min. | max. | Unit |
|--------------------------------------|---------------------------|------|------|------|
| Read or Write Cycle Time | TEHEH (t_C) | 640 | — | ns |
| Random Access Time | TEHQV (t_{AC}) | — | 450 | ns |
| Chip Enable Pulse Width | TEHEL (t_{CE}) | 450 | — | ns |
| Chip Enable Precharge Time | TELEH (t_P) | 150 | — | ns |
| Address Hold Time | TEHAX (t_{AH}) | 200 | — | ns |
| Address Setup Time | TAVEH (t_{AS}) | 20 | — | ns |
| Output Buffer Turn-off Delay | TELQZ (t_{off}) | 0 | 100 | ns |
| Write Enable Setup Time | TEHWL (t_{WS}) | -20 | — | ns |
| Data Input Hold Time | TWHDX (t_{DH1}) | 60 | — | ns |
| Data Input Hold Time referenced to E | TELDX (t_{DH2}) | 40 | — | ns |
| Write Enable Pulse Width | TWLWH (t_{WW}) | 120 | — | ns |
| Chip Enable to Write Enable Delay* | TEHWL (t_{CWD}) | 350 | — | ns |
| \bar{W} to E Precharge Lead Time | TWLEL (t_{WPL}) | 150 | — | ns |
| Data Input Setup Time | TDVWH, TDVEL (t_{DS}) | 100 | — | ns |
| Write Enable Hold Time | TEHWH (t_{WH}) | 300 | — | ns |
| Read Setup Time | TWHEH (t_{RS}) | 0 | — | ns |
| Read Hold Time | TELWL (t_{RH}) | 0 | — | ns |
| Chip Enable Rise/Fall Time | TT (t_T) | — | 300 | ns |

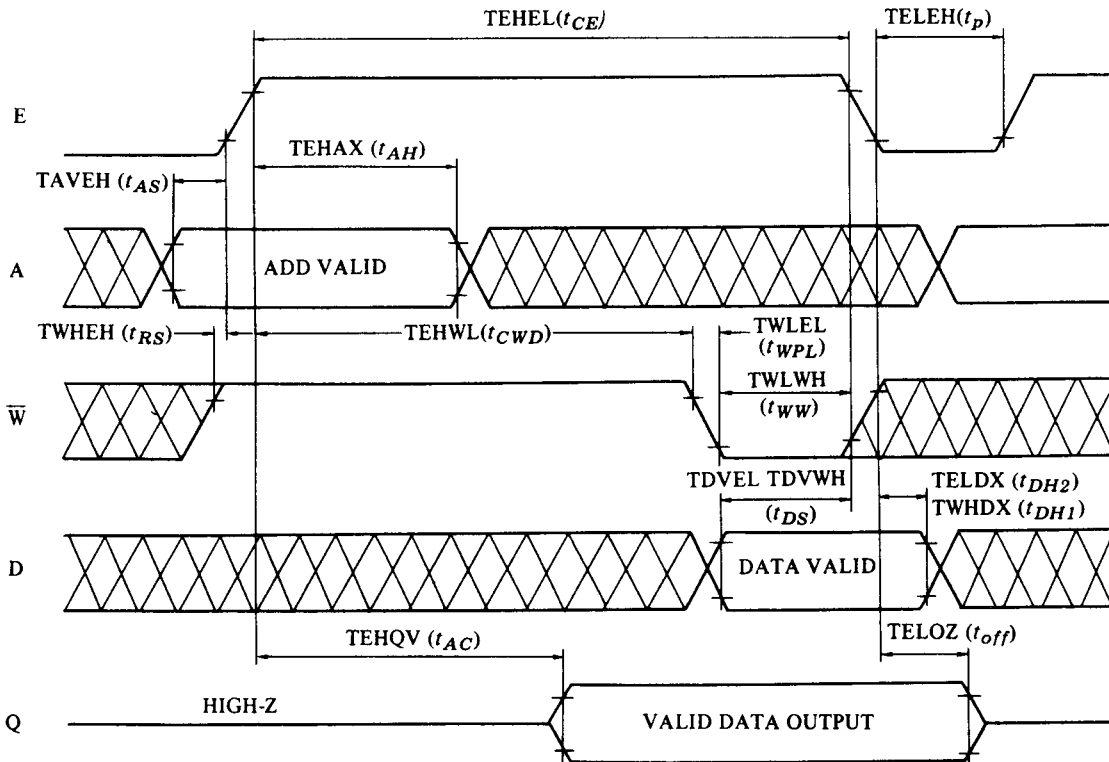
● READ CYCLE



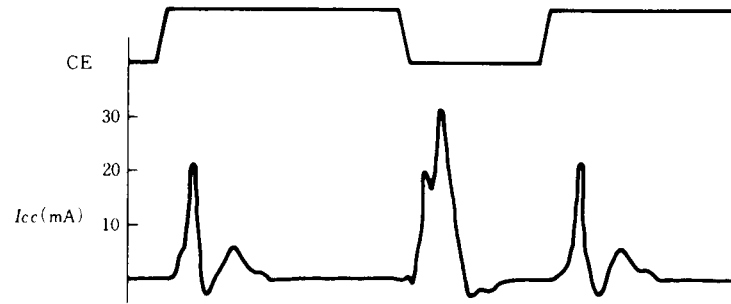
● EARLY WRITE CYCLE



● READ MODIFY WRITE CYCLE AND READ WRITE CYCLE

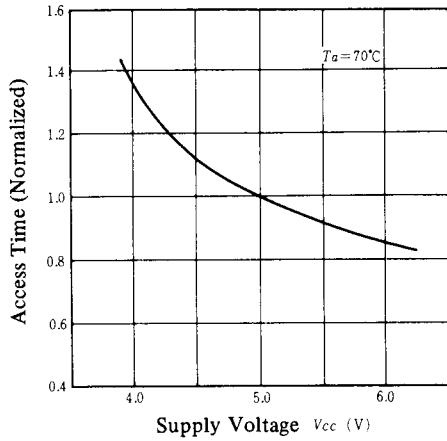


*For R-M-W Cycle (VALID DATA OUTPUT) $t_{CWD} \geq 350$ ns, $t_{CE} \geq 550$ ns
 For R-W Cycle (INVALID DATA OUTPUT) 20 ns $< t_{CWD} < 350$ ns, $t_{CE} \geq 450$ ns

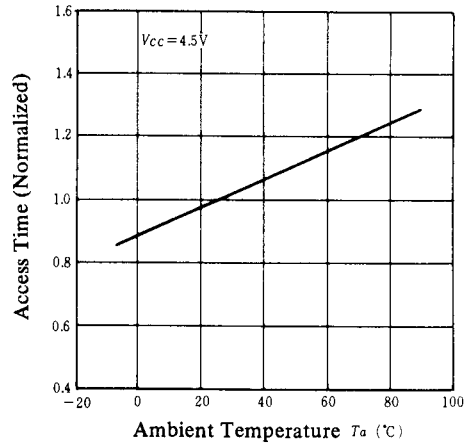


Notes: $V_{CC}=5.0V$, $T_a=25^{\circ}C$

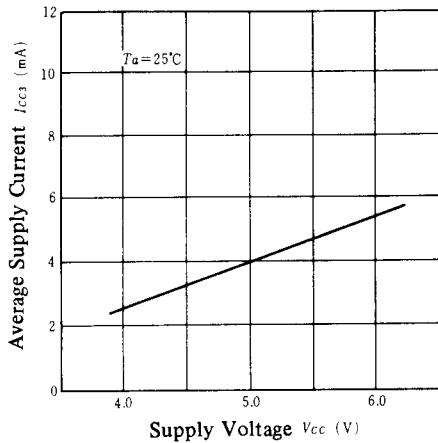
ACCESS TIME vs. SUPPLY VOLTAGE



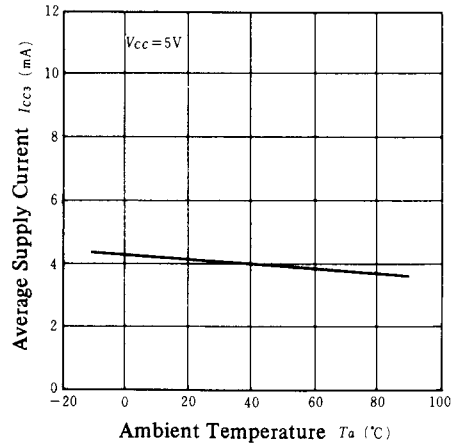
ACCESS TIME vs. AMBIENT TEMPERATURE



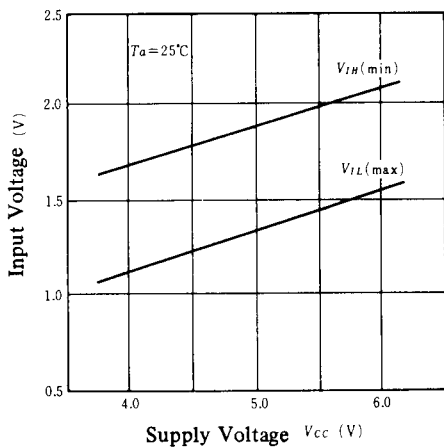
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE

