

N and P-Channel Enhancement Mode Power MOSFET

Description

The HM4640D uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

● N-Channel

$$V_{DS} = 40V, I_D = 5A$$

$$R_{DS(ON)} < 41m\Omega @ V_{GS}=4.5V$$

$$R_{DS(ON)} < 68m\Omega @ V_{GS}=2.5V$$

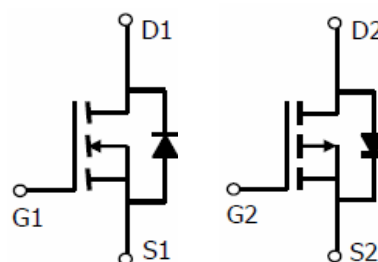
● P-Channel

$$V_{DS} = -40V, I_D = -5A$$

$$R_{DS(ON)} < 80m\Omega @ V_{GS}=-4.5V$$

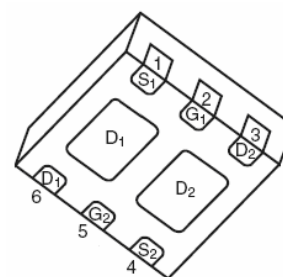
$$R_{DS(ON)} < 135m\Omega @ V_{GS}=-2.5V$$

- High power and current handing capability
- Lead free product is acquired
- Surface mount package



N-channel

P-channel



Pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
20**	HM4640D	DFN2X2-6L	Ø180mm	8mm	3000 units

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current	I_D	5	-5	A
		3.5	-3.5	
Pulsed Drain Current ^(Note 1)	I_{DM}	15	-15	A
Maximum Power Dissipation	P_D	0.8	0.8	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	N-Ch	156	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	P-Ch	156	$^\circ\text{C/W}$

N-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	22	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =2.5V, I _D =2.8A	-	33	41	mΩ
		V _{GS} =4.5V, I _D =5A	-	46	68	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =5A	-	8	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	260	-	PF
Output Capacitance	C _{OSS}		-	48	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	27	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, R _L =3.3Ω V _{GS} =4.5V, R _{GEN} =6Ω	-	2.5	-	nS
Turn-on Rise Time	t _r		-	3.2	-	nS
Turn-Off Delay Time	t _{d(off)}		-	21	-	nS
Turn-Off Fall Time	t _f		-	3	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =5A, V _{GS} =4.5V	-	2.9	5	nC
Gate-Source Charge	Q _{gs}		-	0.4	-	nC
Gate-Drain Charge	Q _{gd}		-	0.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =5A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	5	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

P-CH Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-2.0	-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-2.5 A$	-	72	80	m Ω
		$V_{GS}=-2.5V, I_D=-2A$	-	110	135	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-2.5A$	-	9.5	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $F=1.0MHz$	-	325	-	PF
Output Capacitance	C_{oss}		-	63	-	PF
Reverse Transfer Capacitance	C_{rss}		-	37	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=5\Omega$ $V_{GS}=-4.5V, R_{GEN}=3\Omega$	-	11	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-2A,$ $V_{GS}=-4.5V$	-	3.2	-	nC
Gate-Source Charge	Q_{gs}		-	0.6	-	nC
Gate-Drain Charge	Q_{gd}		-	0.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-5A$	-	-	-1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	-5	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

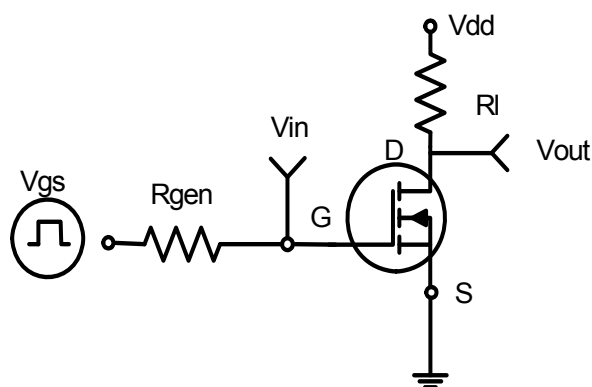


Figure 1: Switching Test Circuit

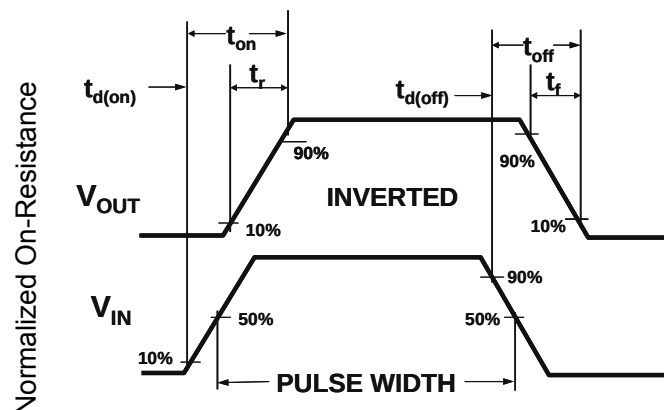


Figure 2: Switching Waveforms

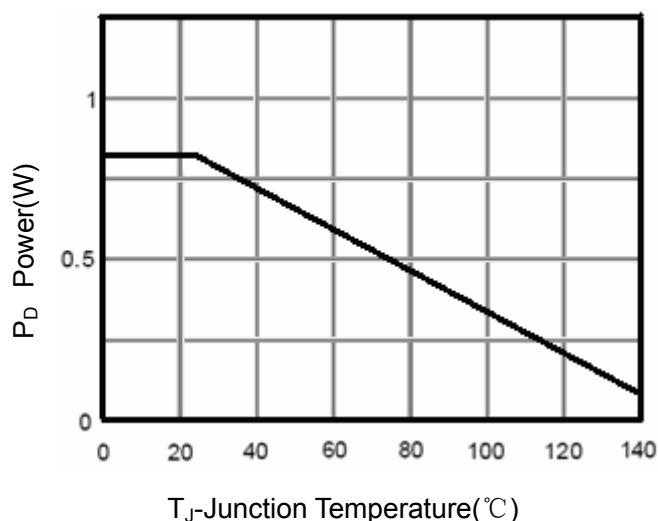


Figure 3 Power Dissipation

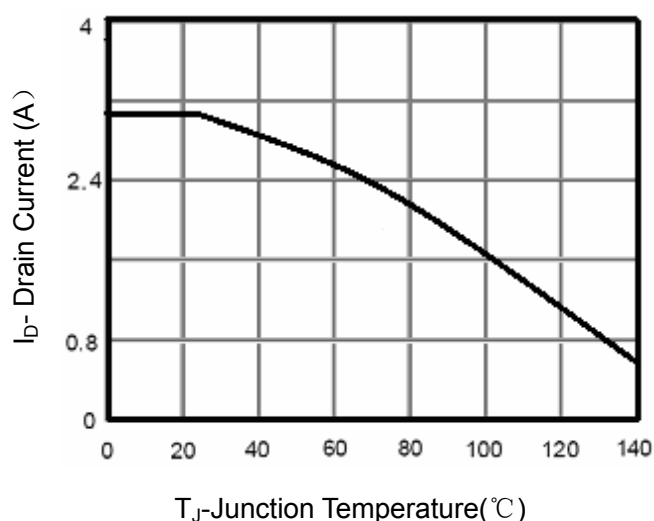


Figure 4 Drain Current

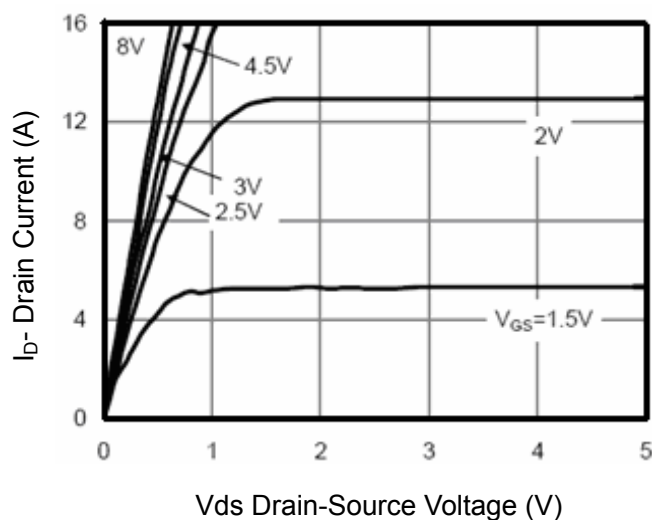


Figure 5 Output Characteristics

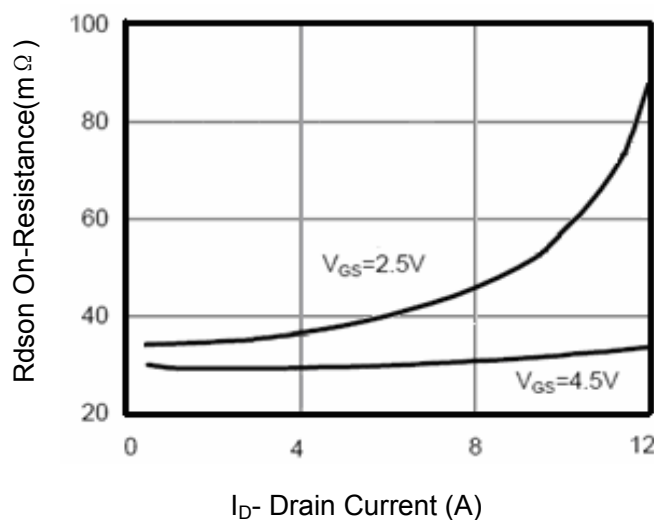


Figure 6 Drain-Source On-Resistance

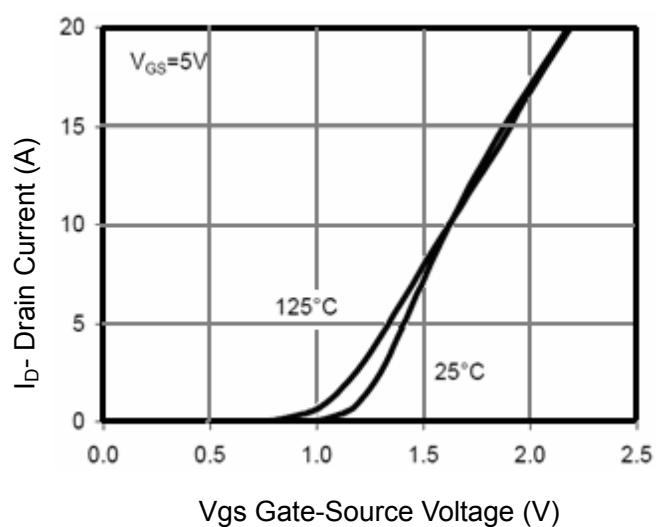


Figure 7 Transfer Characteristics

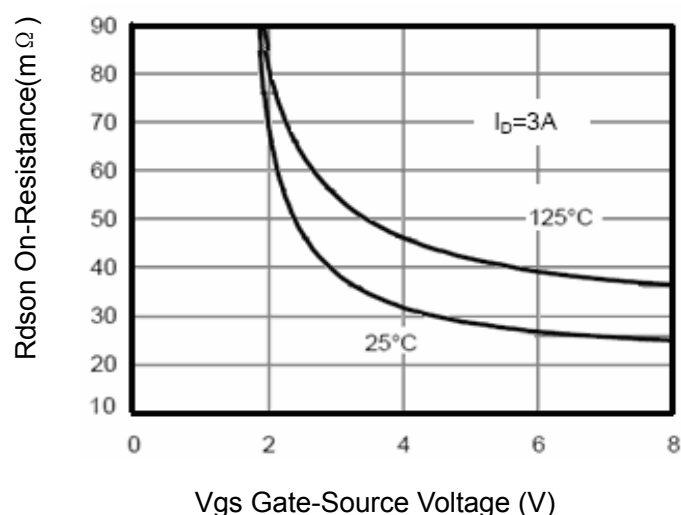


Figure 9 $R_{DS(on)}$ vs V_{GS}

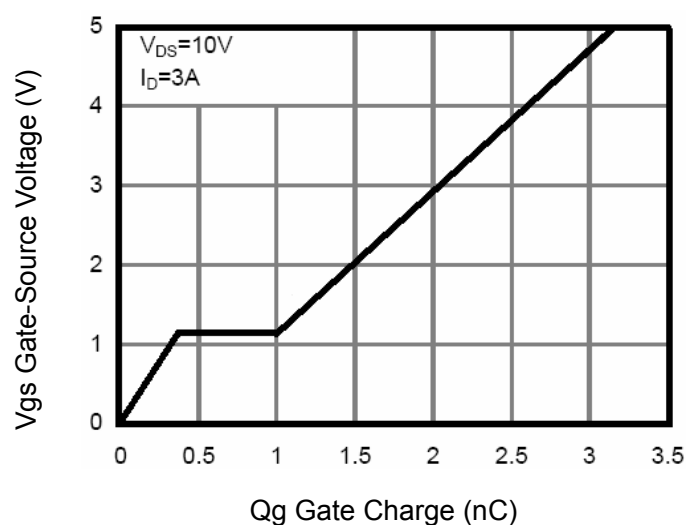


Figure 11 Gate Charge

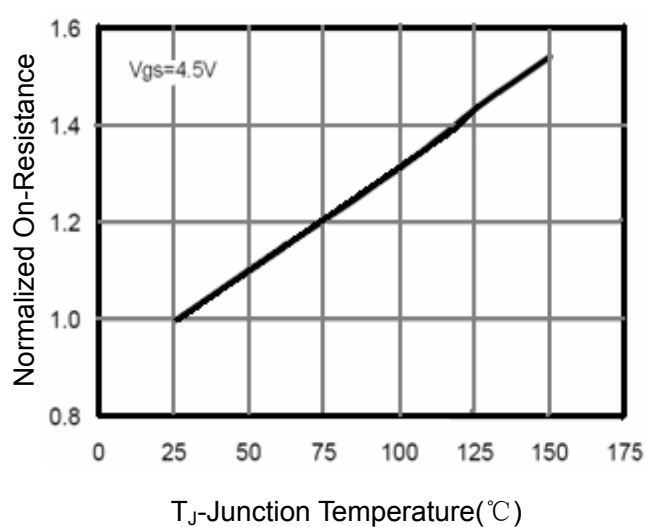


Figure 8 Drain-Source On-Resistance

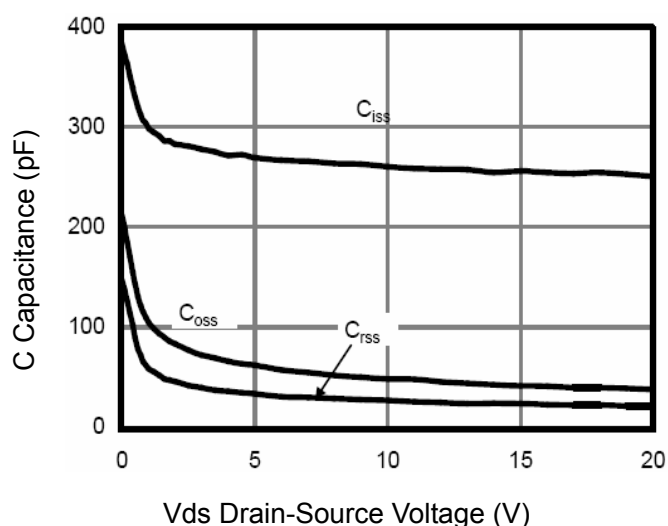


Figure 10 Capacitance vs V_{DS}

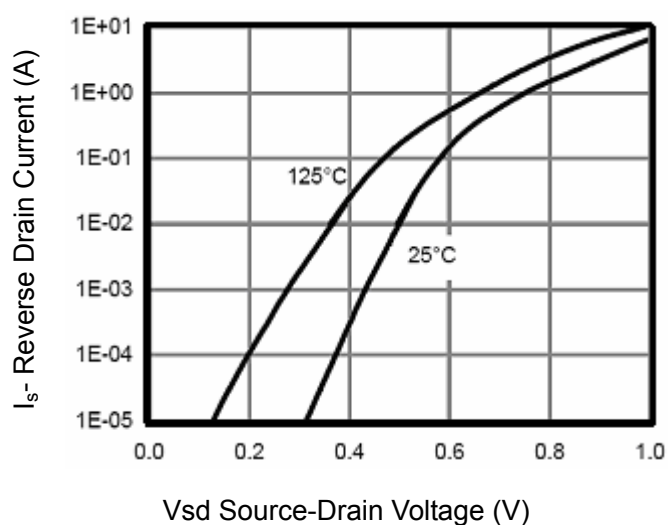


Figure 12 Source- Drain Diode Forward

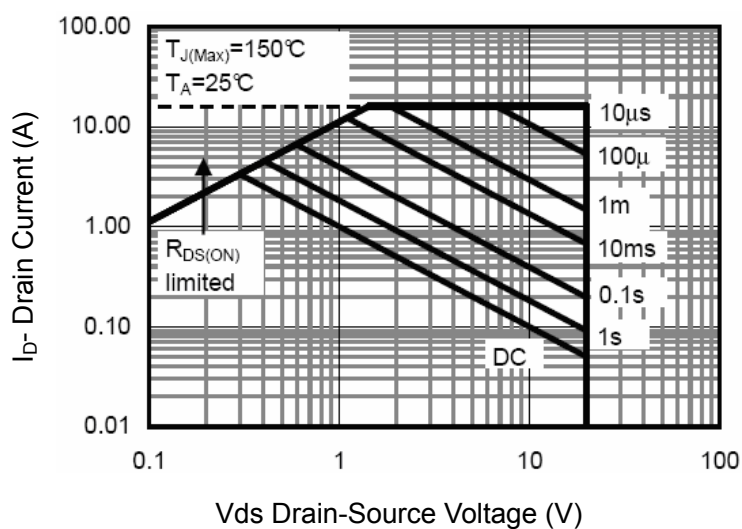


Figure 13 Safe Operation Area

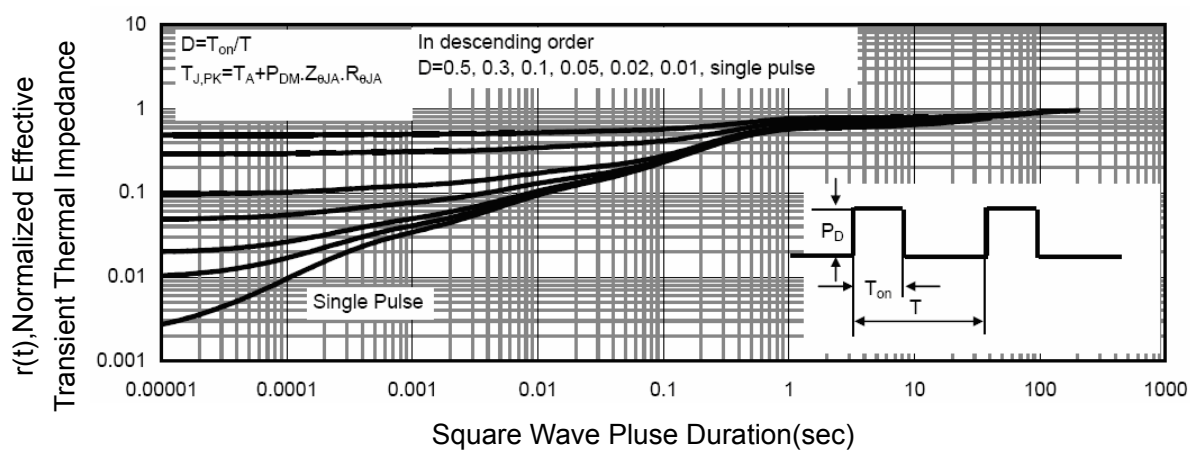


Figure 14 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

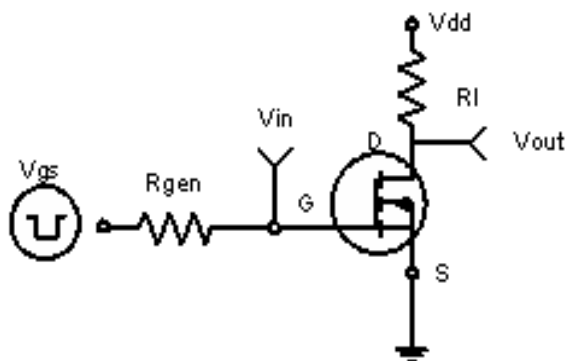


Figure 1: Switching Test Circuit

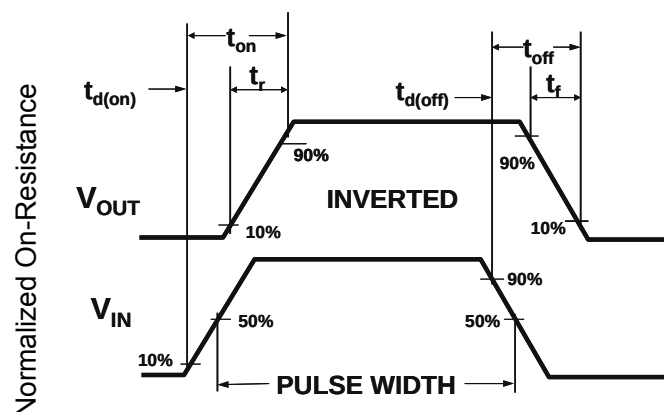


Figure 2: Switching Waveforms

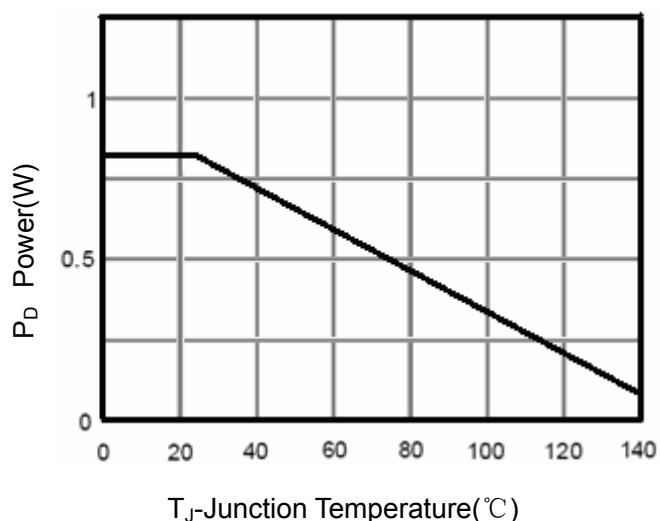


Figure 3 Power Dissipation

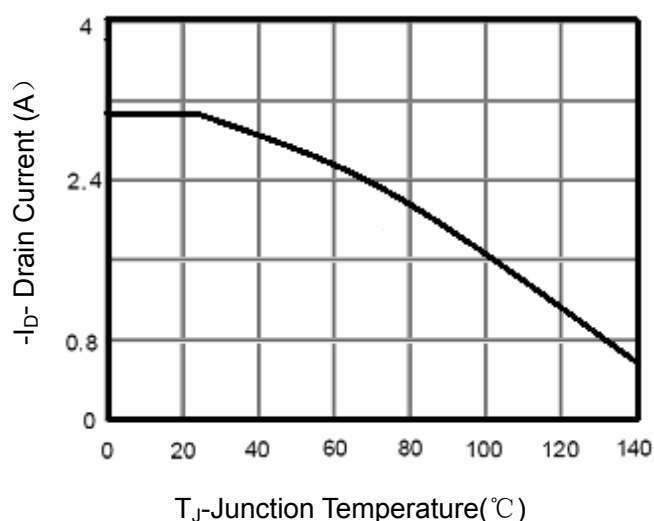


Figure 4 Drain Current

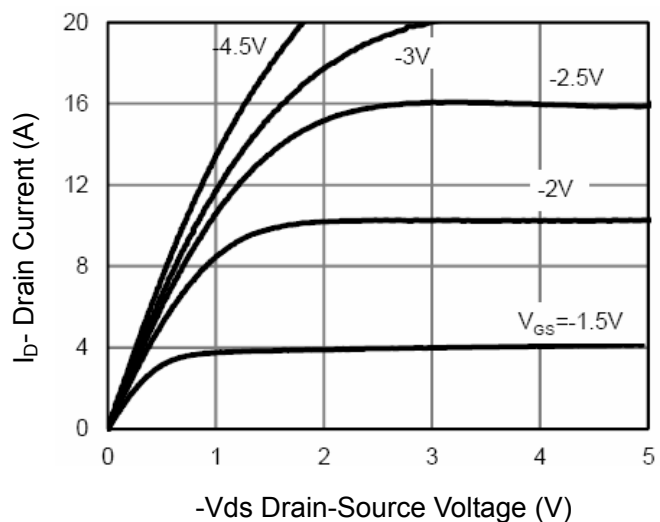


Figure 5 Output Characteristics

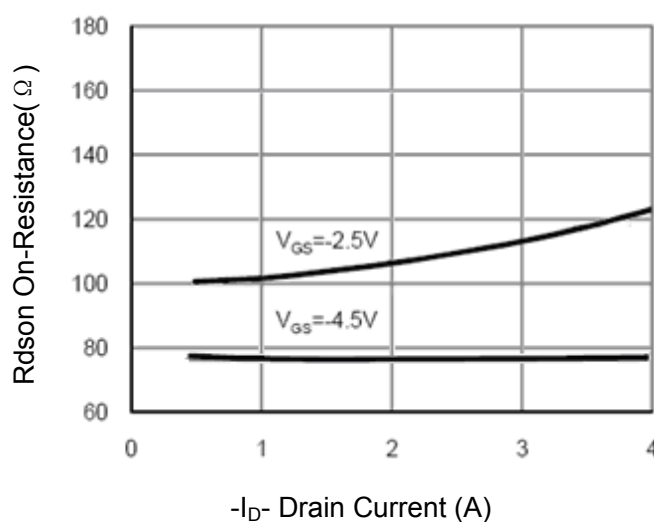


Figure 6 Drain-Source On-Resistance

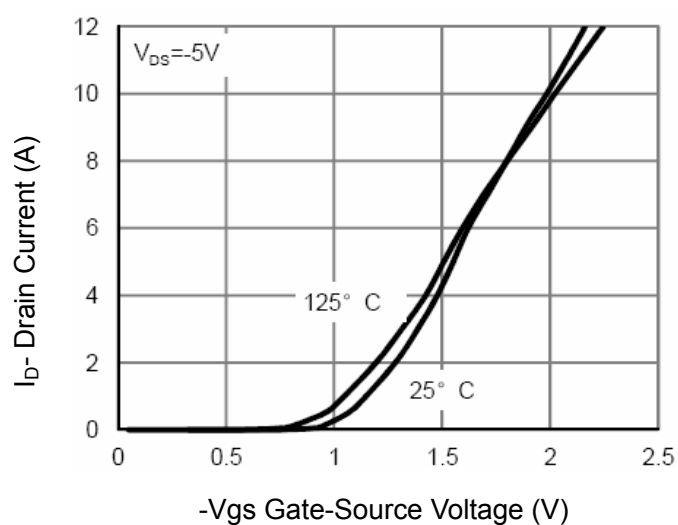


Figure 7 Transfer Characteristics

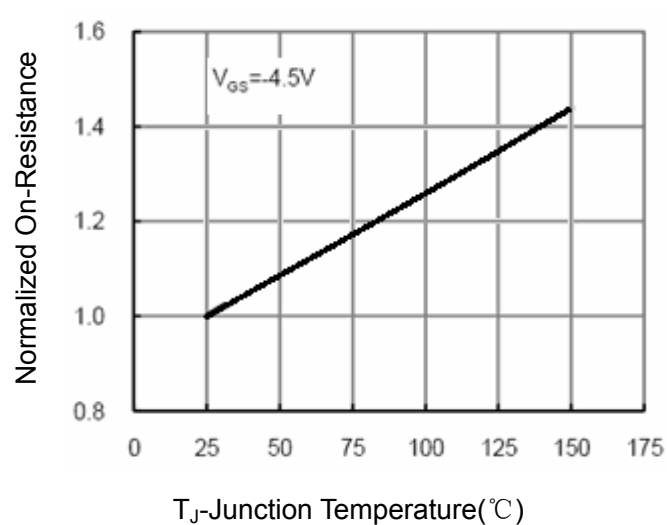


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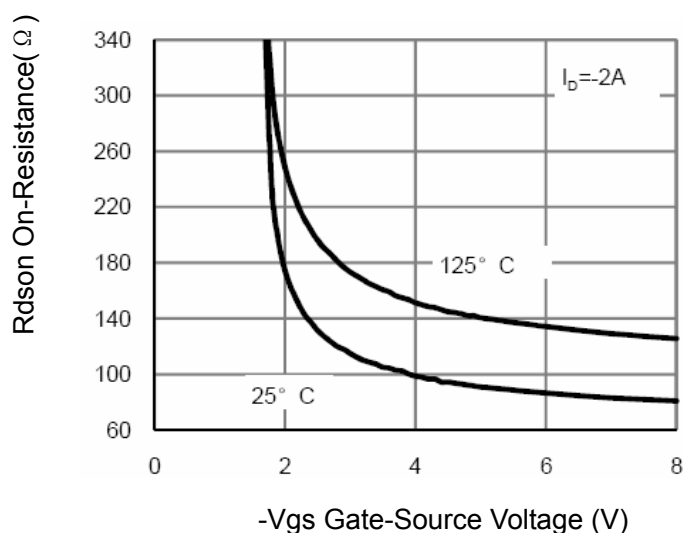


Figure 9 Rdson vs Vgs

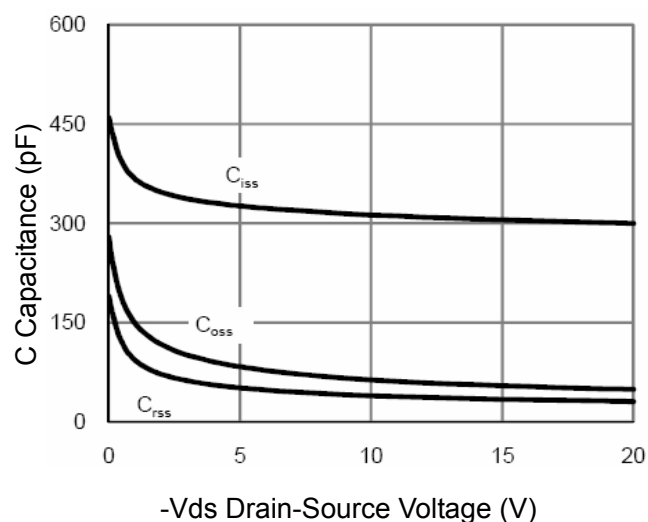


Figure 10 Capacitance vs Vds

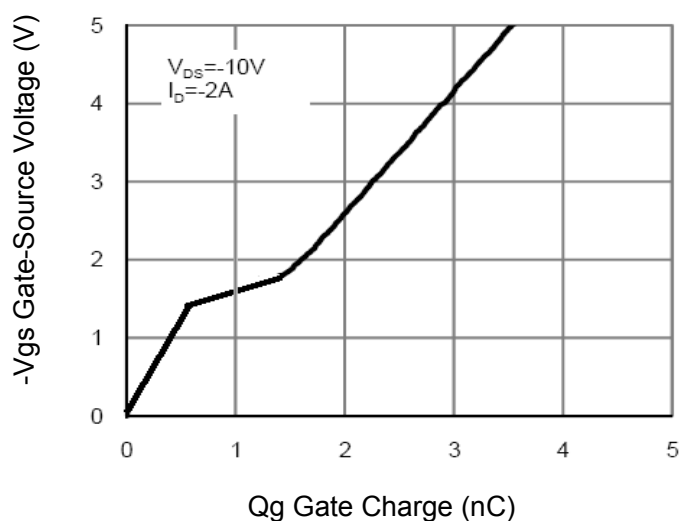


Figure 11 Gate Charge

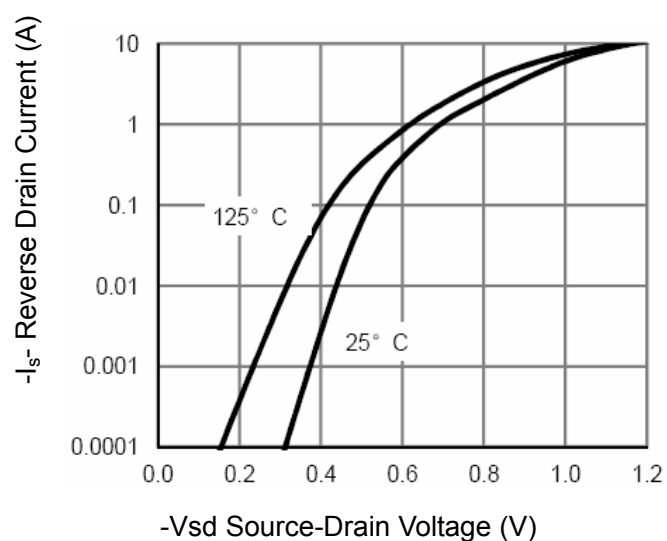


Figure 12 Source- Drain Diode Forward

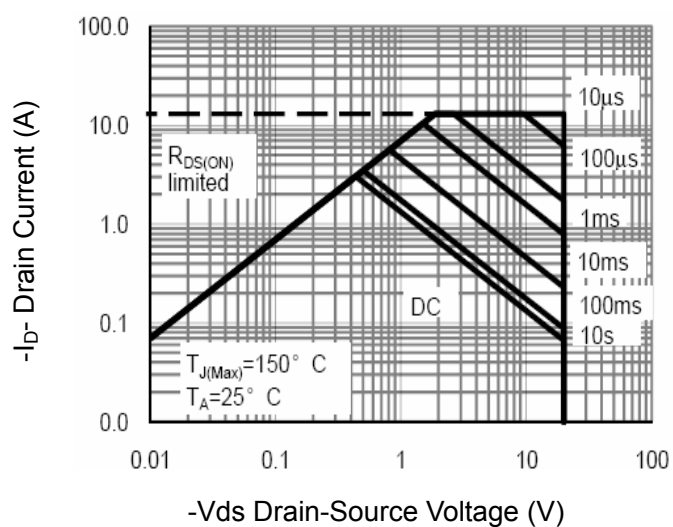


Figure 13 Safe Operation Area

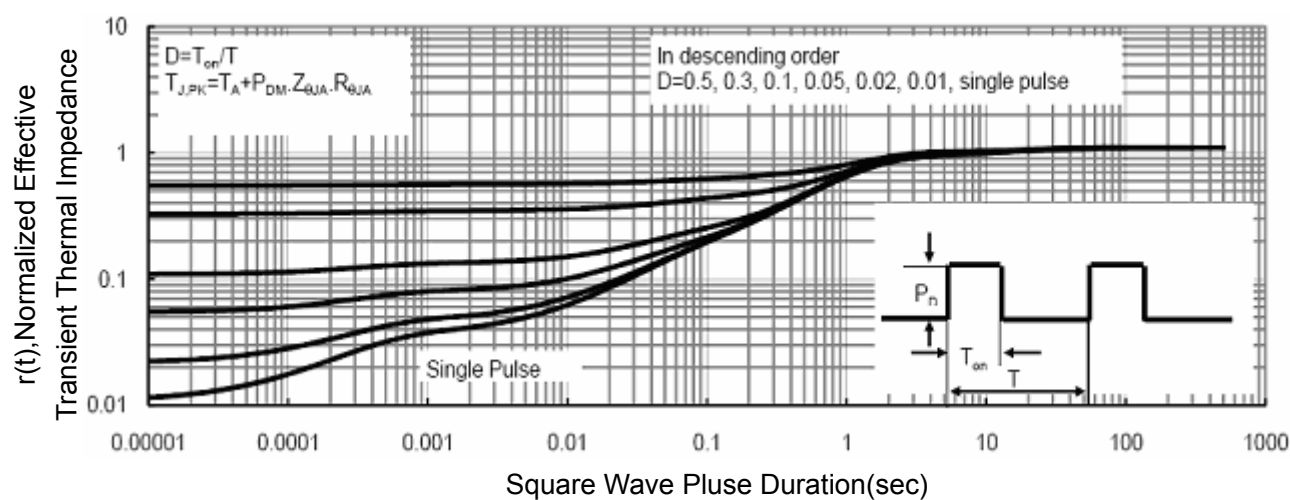
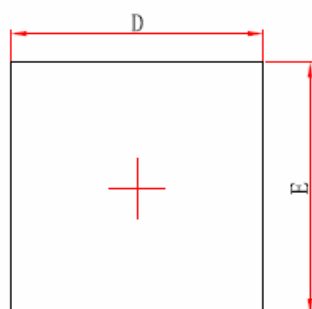
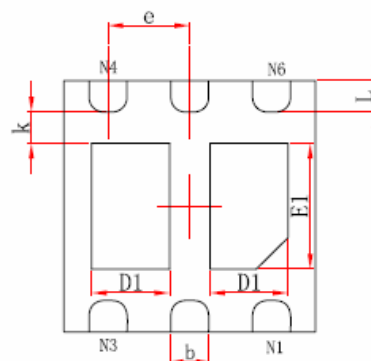


Figure 14 Normalized Maximum Transient Thermal Impedance

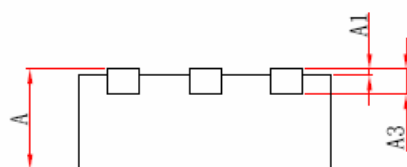
DFN2X2-6L Package Information



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	0.520	0.720	0.020	0.028
E1	0.900	1.100	0.035	0.043
k	0.200MIN.		0.008MIN.	
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
L	0.174	0.326	0.007	0.013