Himax Imaging, Inc.

DATA SHEET

(DOC No. HM5065-DS)

HM5065

5MP CMOS Image Sensor SoC

Preliminary version 03 June, 2012

Himax Imaging, Inc.

HM5065

5.0MP CMOS Image Sensor SoC 1/4″ format

Preliminary

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June, *2012*

Features

- 5.0 megapixel resolution (2592H x 1944V) with 16 border pixels in 1/4” optical format
- Support up to 15 fps with 5MP (JPEG422), 30 fps with analog binning 2x2, 60 fps with analog binning 4x4
- Integrated Image Processing Pipeline functions
  - Pixel defect correction
  - Binning resampling
  - Luminance and color noise reduction
  - Lens shade correction
  - Hue / Saturation adjustment
  - Brightness / Contrast control
  - Edge enhancement
  - Color interpolation and correction
  - Gamma correction
- Embedded imaging sensor controller for automatic exposure control, automatic white balance control, black level compensation, contrast stretching, 50/60 Hz flicker detection and cancelling, and flash support
- Fully programmable independent H and V scaling with derating (max. 1600x1200 FFOV)
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2, RGB 565, RGB 444, RGB 555, JPEG 422 output formats
- 8-bit parallel video interface, horizontal and vertical syncs, 89 MHz (max) clock
- Fully integrated auto-focus VCM Driver
- MIPI CSI-2 dual lanes interface option
- Two-wire serial control interface
- On-chip PLL with SSCG support, 6 MHz to 27 MHz clock input

Key Parameter

Sensor Parameters	Value
Active Pixel Array	2608 x 1960
Optical Format	1/4"
Pixel Size	1.4µ
Image Area Diagonal	4567µm diagonal
Color Filter Array	Bayer RGB
Scan Mode	Progressive
Shutter	Electronic Rolling Shutter
ADC Resolution	10-bit
S/N Ratio (maximum)	35.6dB
Dynamic Range	68dB
Sensitivity (@ 530nm)	520 mV / Lux-sec
CRA (maximum)	25.8º non-linear

Device Parameters		Value
Power Supply	Analog	2.8V
	Digital	1.8V (typical) or 2.6V
Serial Register		SDA, SCL
Output Lane		MIPI-CSI2, Parallel (ITU)
Input Reference Clock		6 to 27MHz
Maximum Readout		15fps@full (JEPG422)
		15fps@1080p (Crop)
		30fps@720p (Crop)
		60fps@VGA
Maximum Readout	MIPI	357MHz per lane
	YUV	89MHz
Data Output Format		YUV (YCbCr422), JPEG422 RGB565 / 555 / 444, RAW
Power Consumption	Full Frame	255mW (1.8V Vdd, JPEG)
	PWDN	<10µW

Order Information

Part Number	CFA	Package Type
HM5065-AGA	Bayer (Color)	Bare Die (RW)
HM5065-APA	Bayer (Color)	PLCC-28
HM5065-APB	Bayer (Color)	PLCC-32
HM5065-APC	Bayer (Color)	PLCC-28
HM5065-APD	Bayer (Color)	PLCC-32

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1 Overview

The HM5065 5.0 megapixel CMOS digital imaging sensor integrates a high-sensitivity pixel array, a digital image processor and imaging sensor control functions. The sensor offers both the 8-bit parallel bus (ITU8) output and the MIPI CSI-2 interface (dual lanes) supporting RGB, YCbCr or JPEG data format. The sensor is capable of streaming full resolution video up to 15fps using the CSI-2 dual lanes interface; similar frame rate could also be realized when streaming with JPEG data on ITU8 bus (ITU-R BT.656-4 YUV 4:2:2 frame format). The use of analog binning or scaling can achieve higher frame rate - typically 30 fps for SVGA and 60fps for VGA.

The sensor has an embedded 2Kbit One-Time-Programmable memory to support storing information related to part-to-part identification and performance variation to be stored for further image quality enhancement. The HM5065 also features an embedded VCM driver for easy module integration, and an advanced auto focus algorithm that could accurately determine the best focus position of the object in a given scene.

The HM5065 supports a 1.8V/2.6V digital power supply and requires a 2.8V analog power supply. The integrated PLL allows for low frequency system clock and flexibility for successful EMC integration.

This complete imaging sensor is ready to connect to imaging sensor enabled baseband processors, back-end IC devices or PDA engines. It is also suited for use in notebook PCs as an embedded imaging sensor.

The HM5065 also includes a wide range of image enhancement functions designed to ensure high image quality. These functions include:

- Automatic Exposure Control
- Automatic White Balance
- Noise reduction and defect correction algorithm
- Advanced lens shading compensation algorithm
- Color space conversion
- Sharpening
- Gamma correction
- Flicker detection and cancellation
- Intelligent image scaling
- Special effects
- Support part-to-part calibration with on-chip OTP memory.
- Advanced Auto Focus algorithm

2 Pin Diagram and Description

2.1 Bare Die

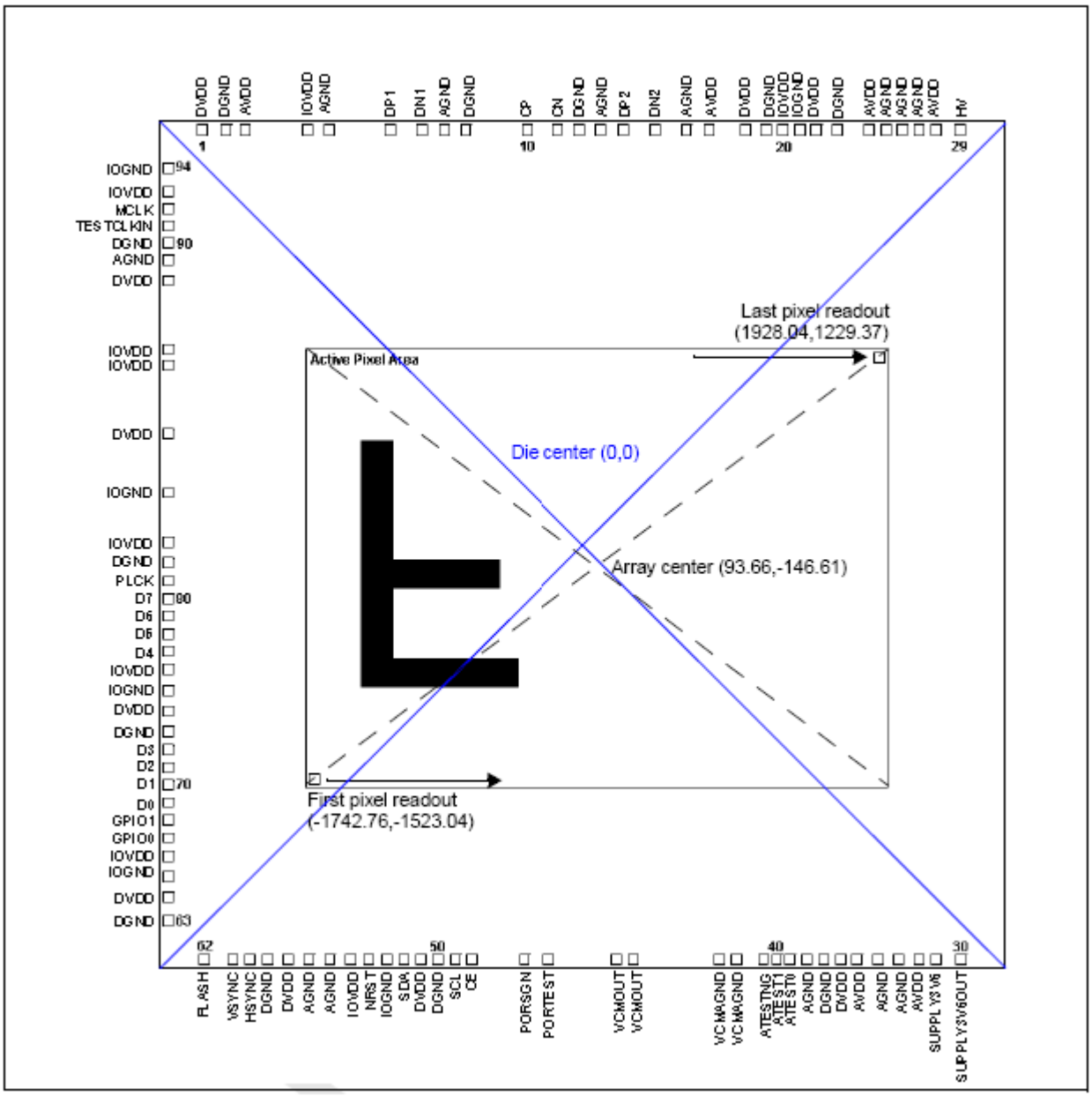


Figure 1: Bare Die Pin Diagram (Top View)

Pin #	Pad Name	Type	Description
1	DVDD	Digital power	Decoupling recommended C2
2	DGND	Ground	Digital ground
3	AVDD	Analog power	Decoupling recommended C4
4	IOVDD	IO power	Decoupling recommended C3
5	AGND	Ground	Analog ground
6	DP1	Output	Differential MIPI data lane 1 (positive)
7	DN1		Differential MIPI data lane 1 (negative)
8	AGND	Ground	Analog ground
9	DGND	Ground	Digital ground
10	CP	Output	Differential MIPI clock (positive)
11	CN		Differential MIPI clock (negative)
12	DGND	Ground	Digital ground
13	AGND	Ground	Analog ground
14	DP2	Output	Differential MIPI data lane 2 (positive)
15	DN2		Differential MIPI data lane 2 (negative)
16	AGND	Ground	Analog ground
17	AVDD	Analog power	Decoupling recommended C4
18	DVDD	Digital power	Decoupling recommended C2
19	DGND	Ground	Digital ground

20	IOVDD	IO power	Decoupling recommended C3
21	IOGND	Ground	IO ground
22	DVDD	Digital power	Decoupling recommended C2
23	DGND	Ground	Digital ground
24	AVDD	Analog power	Decoupling recommended C4
25	AGND	Ground	Analog ground
26	AGND		
27	AGND		
28	AVDD	Analog power	Decoupling recommended C4
29	HV	High voltage (Analog supply)	7.5V HV input pin for OTP programming. leave unconnected in normal mode.
30	SUPPLY3V6OUT	Analog output voltage	3.6V charge pump. Required decoupling C1
31	SUPPLY3V6		
32	AVDD	Analog power	Decoupling recommended C4
33	AGND	Ground	Analog ground
34	AGND		
35	AVDD	Analog power	Decoupling recommended C4
36	DVDD	Digital power	Decoupling recommended C2
37	DGND	Ground	Digital ground
38	AGND	Ground	Analog ground
39	ATEST0	Test pad	No bond
40	ATEST1		

41	ATESTNEG		
42	VCMAGND	High voltage (Analog ground)	VCM sense analog ground
43	VCMAGND		
44	VCMOUT	High voltage (Analog output)	Bond both pads for VCM driver (current sink). Leave unconnected if not used.
45	VCMOUT		
46	PORTEST	Test pad	No bond
47	PORSGN		
48	CE	Input	Imaging sensor chip enable. Pulling this signal low disables the internal regulators, resulting in very low current consumption and no active logic circuitry.
49	SCL	Input	Serial interface slave clock line. Requires external pull-up to IOVDD
50	DGND	Ground	Digital ground
51	DVDD	Digital power	Decoupling recommended C2
52	SDA	Input / Output	Serial interface slave data line. Requires external pull-up to IOVDD
53	IOGND	Ground	IO ground
54	NRST	Input	Active low reset, bond to IOVDD if not required. This signal resets the internal logic, but leaves the voltage rails active
55	IOVDD	IO power	Decoupling recommended C3
56	AGND	Ground	Analog ground

57	AGND		
58	DVDD	Digital power	Decoupling recommended C2
59	DGND	Ground	Digital ground
60	HSYNC	Output	Horizontal synchronization
61	VSYNC		Vertical synchronization
62	FLASH		Flash strobe output
63	DGND	Ground	Digital ground
64	DVDD	Digital power	Decoupling recommended C2
65	IOGND	Ground	IO ground
66	IOVDD	IO power	Decoupling recommended C3
67	GPIO0	Input / Output	May used as NIRQ pin.
68	GPIO1		General purpose input output
69	D0	Output	ITU8 output (D3~D0)
70	D1		
71	D2		
72	D3		
73	DGND	Ground	Digital ground
74	DVDD	Digital power	Decoupling recommended C2
75	IOGND	Ground	IO ground
76	IOVDD	IO power	Decoupling recommended C3
77	D4	Output	ITU8 output (D7~D4)
78	D5		

79	D6		
80	D7		
81	PCLK	Output	Pixel clock
82	DGND	Ground	Digital ground
83	IOVDD	IO power	Decoupling recommended C3
84	IOGND	Ground	IO ground
85	DVDD	Digital power	Decoupling recommended C2
86	IOVDD	IO power	Decoupling recommended C3
87	IOVDD		
88	DVDD	Digital power	Decoupling recommended C2
89	AGND	Ground	Analog ground
90	DGND	Ground	Digital ground
91	TESTCLKIN	Test	No bond
92	MCLK	Input clock	Imaging sensor clock input
93	IOVDD	IO power	Decoupling recommended C3
94	IOGND	Ground	IO ground

Table 1: Die bond pad details

	Value (nF)	Comment
C1 (SUPPLY3V6)	220	
C2 (DVDD)	470	VDD to C2 resistance spec < 0.5Ω.
C3 (IOVDD)	220	
C4 (AVDD)	220	

Table 2: Recommended decoupling capacitors should have a tolerance specification "X5R"

2.2 PLCC Package(MIPI)

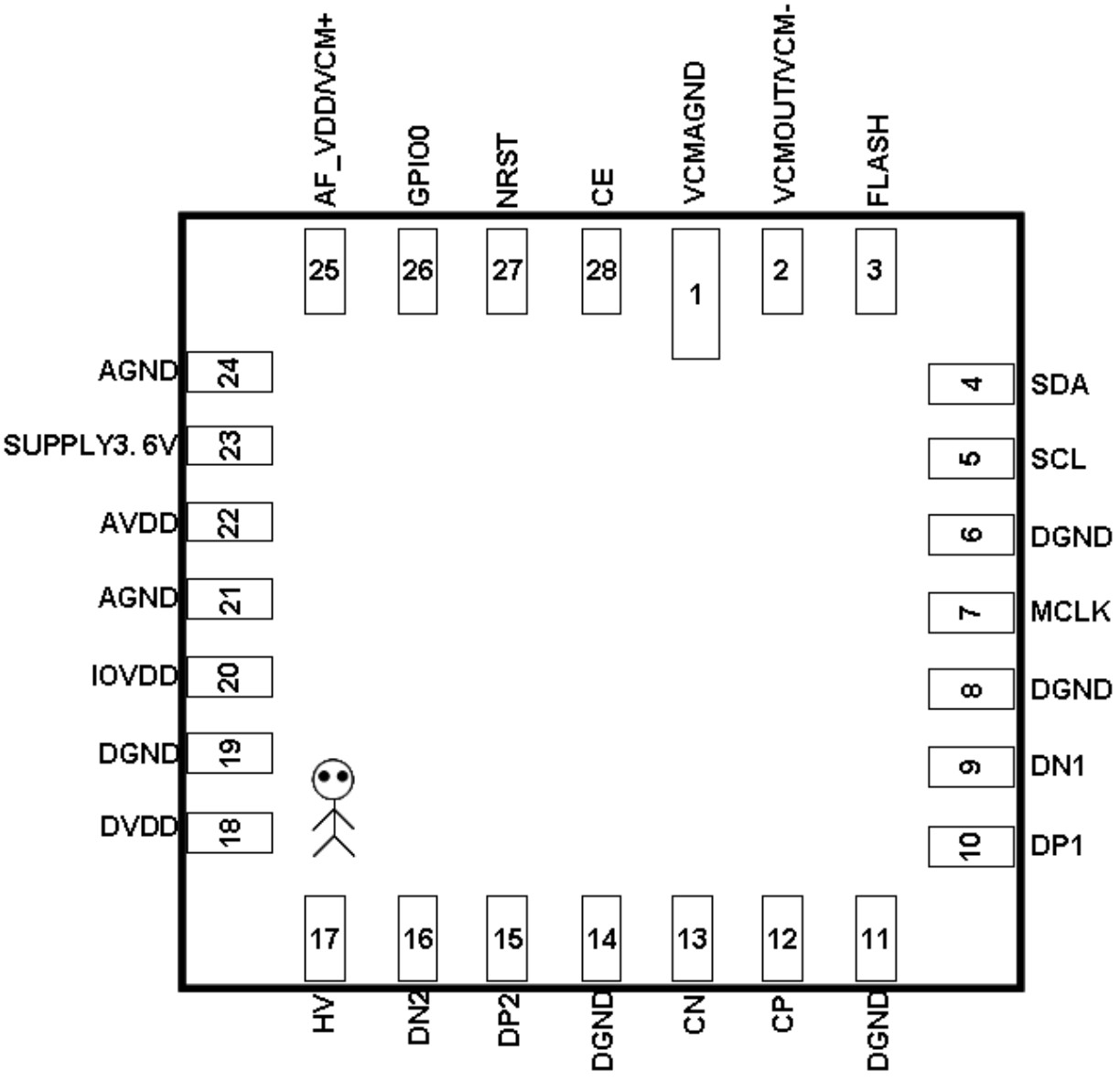


Figure 2: PLCC Pin Diagram (Top View, MIPI)

Pin #	Pad Name	Type	Description
1	VCMAGND	High voltage (Analog ground)	VCM sense analog ground
2	VCMOUT/ VCM-	High voltage (Analog output)	Bond both pads for VCM driver (current sink). Leave unconnected if not used.
3	FLASH	Output	Flash Strobe Output
4	SDA	Input / Output	serial interface slave data line. Requires external pull-up to IOVDD
5	SCL	Input	serial interface slave clock line. Requires external pull-up to IOVDD
6	DGND	Ground	
7	MCLK	Input clock	Imaging sensor clock input
8	DGND	Ground	
9	DN1	Output	Differential MIPI data lane 1 (negative)
10	DP1	Output	Differential MIPI data lane 1 (positive)
11	DGND	Ground	
12	CP	Output	Differential MIPI clock (positive)
13	CN	Output	Differential MIPI clock (negative)
14	DGND	Ground	
15	DP2	Output	Differential MIPI data lane 2 (positive)
16	DN2	Output	Differential MIPI data lane 2 (negative)
17	HV	High voltage (Analog supply)	7.5V HV input pin for OTP Programming. Leave unconnected in normal mode.
18	DVDD	Digital power	Decoupling recommended C2
19	DGND	Ground	
20	IOVDD	IO power	Decoupling recommended C3
21	AGND	Ground	
22	AVDD	Analog power	Decoupling recommended C4
23	SUPPLY3. 6V	Analog output voltage	3.6V charge pump. Required decoupling C1
24	AGND	Ground	
25	AF_VDD/ VCM+	Power	VCM Power
26	GPIO0	Input / Output	May used as NIRQ pin.
27	NRST	Input	Active low reset, bond to IOVDD if not required. This signal resets the internal logic, but leaves the voltage rails active
28	CE	Input	Imaging sensor chip enable. Pulling this signal low disables the internal regulators, resulting in very low current consumption and no active logic circuitry.

Table 3: PLCC Pin Description (MIPI)

2.3 PLCC Package(Parallel)

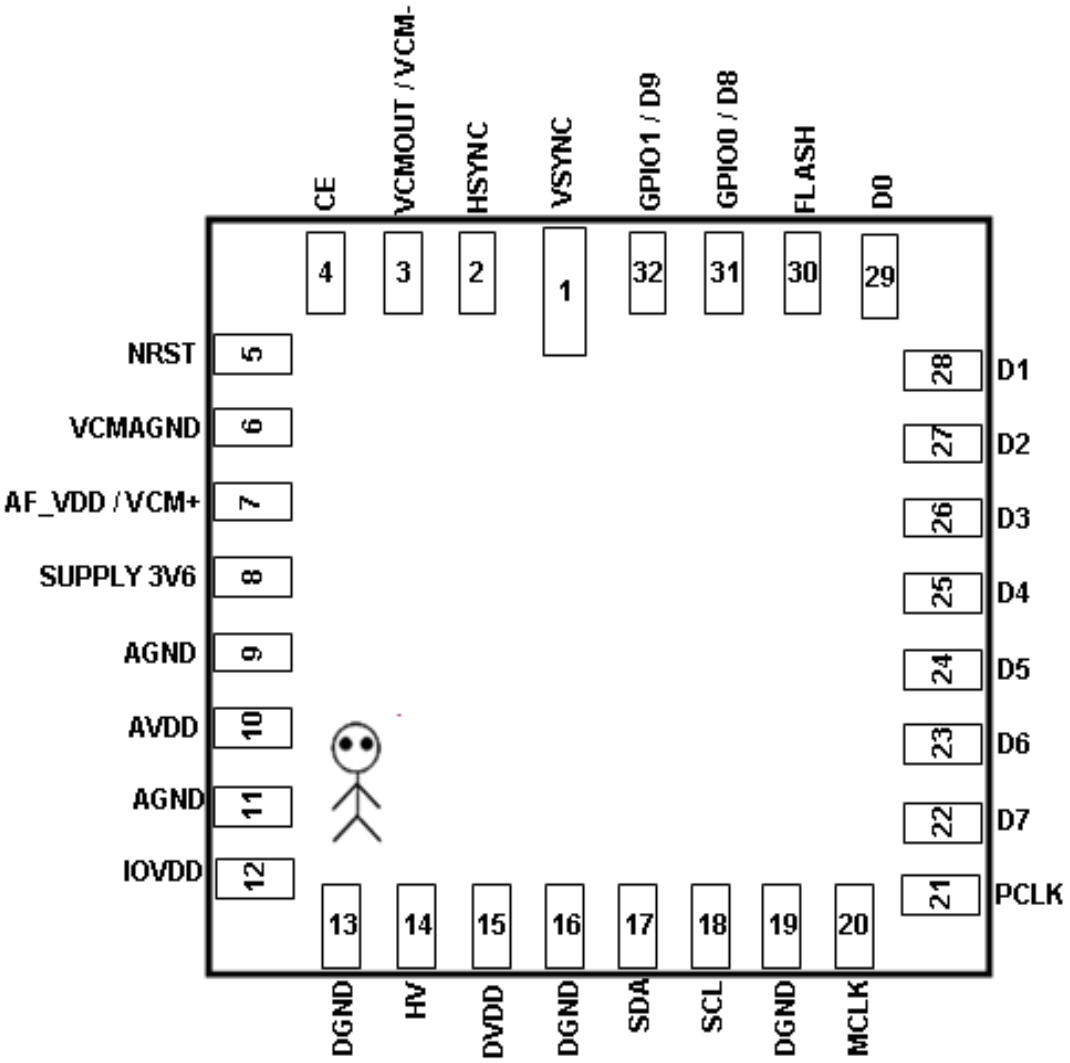


Figure 3: PLCC Pin Diagram (Top View, Parallel)

Pin #	Pad Name	Type	Description
1	VSYNC	Output	Vertical synchronization
2	HSYNC	Output	Horizontal synchronization
3	VCMOUT/ VCM-	High voltage (Analog output)	Bond both pads for VCM driver (current sink). Leave unconnected if not used.
4	CE	Input	Imaging sensor chip enable. Pulling this signal low disables the internal regulators, resulting in very low current consumption and no active logic circuitry.
5	NRST	Input	Active low reset, bond to IOVDD if not required. This signal resets the internal logic, but leaves the voltage rails active
6	VCMAGND	High voltage (Analog ground)	VCM sense analog ground
7	AF_VDD/ VCM+	Power	VCM Power
8	SUPPLY3. 6V	Analog output voltage	3.6V charge pump. Required decoupling C1
9	AGND	Ground	Analog ground
10	AVDD	Analog power	Decoupling recommended C4
11	AGND	Ground	Analog ground
12	IOVDD	IO power	Decoupling recommended C3
13	DGND	Ground	Digital ground
14	HV	High voltage (Analog supply)	7.5V HV input pin for OTP Programming. Leave unconnected in normal mode.
15	DVDD	DVDD power	Decoupling recommended C2
16	DGND	Ground	Digital ground
17	SDA	Input / Output	Serial interface slave data line. Requires external pull-up to IOVDD
18	SCL	Input	Serial interface slave clock line. Requires external pull-up to IOVDD
19	DGND	Ground	Digital ground
20	MCLK	Input clock	Imaging sensor clock input
21	PCLK	Output	Pixel clock
22	D7	Output	ITU8 output (D7)
23	D6	Output	ITU8 output (D6)
24	D5	Output	ITU8 output (D5)
25	D4	Output	ITU8 output (D4)
26	D3	Output	ITU8 output (D3)
27	D2	Output	ITU8 output (D2)
28	D1	Output	ITU8 output (D1)
29	D0	Output	ITU8 output (D0)
30	FLASH	Output	Flash Strobe Output
31	GPIO0/D8	Input / Output	May used as NIRQ pin.
32	GPIO1/D9	Input / Output	General Purpose Input Output

Table 4: PLCC Pin Description (Parallel)

2.4 Silicon thickness

The HM5065 silicon is delivered with a standard thickness of 200 µm.

2.5 Layout, optical center, scribe widths

All dimensions and all coordinates are referenced to the origin at die center.

	Conditions	X size (µm)	Y size (µm)	Area (mm^2)
Die size (µm)	Including scribe	5406.0	5406.0	29.22
	Including seal	5326.0	5326.0	28.36

Table 5: Die size

Parameter	X (µm)	Y (µm)
Die center	0	0
Array center	93.66	-146.61

Table 6: Array details

2.6 Pad opening sizes

	X (µm)	Y (µm)
Pad openings	65	70

Table 7: Pad openings

2.7 Substrate Design Guidelines

- External decoupling capacitors should be placed inside the module between the silicon bond pads and the sidewall. Minimize track length wherever possible.
- Connections to AVDD must be “star-point” connected at the substrate level. Track lengths are not vital.
- Connections to AGND must be “star-point” connected at the substrate level as close as possible to the footprint pad (AGND). Track lengths are not vital.
- Connections to VCMAGND must be “star-point” connected at the substrate level as close as possible to the footprint pad (VCMGND). Track lengths are not vital.
- All VDD pins must be connected to reduce impedance across the die.
- Connections to IOVDD must be “star-point” connected at the substrate level. Track lengths are not vital.
- DN1 and DP1; DN2 and DP2; CN and CP are routed in parallel. The 6 tracks to have the same length (+/- 100um).
- Distance from die pad to point of short should be matched as close as possible, and be as close to the bond pad as possible.
- Width and space rules for DN1/DP1, DN2/DP2, CN/CP to be followed in order to match an impedance of 100 ohm +/- 10%.
- Nets SUPPLY3V6, VCMAGND, VCMOUT, VBAT, AVDD, AGND, IOVDD, VDD and DGND <0.4 Ohm at DC - All these signals to be at least a 100um track width minimum when not part of a copper plane.
- MCLK to be routed away from the 6 CSI2 tracks and as short as possible.
- Avoid DN1/DP1, DN2/DP2 and CN/CP tracks from CSI2 running in parallel to power or ground tracks - if possible separate with ground plane layer or shielding traces.
- Parasitic capacitance on CSI2 data/clock lines to be <4pF.
- Capacitor tracking must be kept as short as possible to die bonding pads.
- Adjacent substrate bond pads carrying the same signal can be merged on a single bond pad if required.

2.8 Application circuits

The die to module substrate connectivity is as shown in the following diagrams.

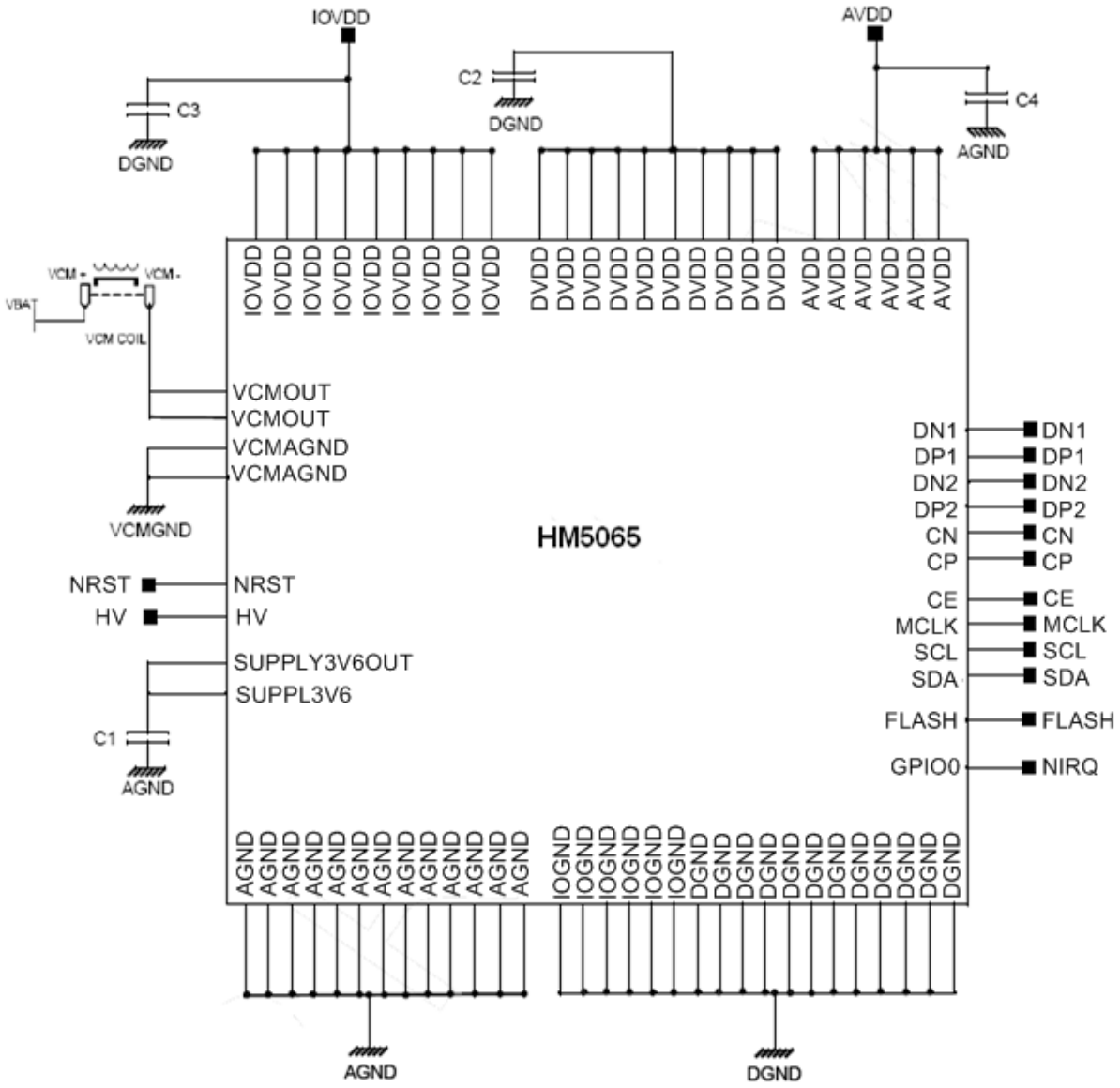


Figure 4 Mobile Industry Processor interface

Note:1 *Serial interface pull-up resistors should have a value based on the serial interface specification (typically 4.7K ohm).*

2 *CN/CP, DN1/DP1, and DN2/DP2 are differential signals and should be routed on balanced 100 ohm impedance tracks.*

3 *C2, C3 and C4 should be kept as physically close to the die as possible.*

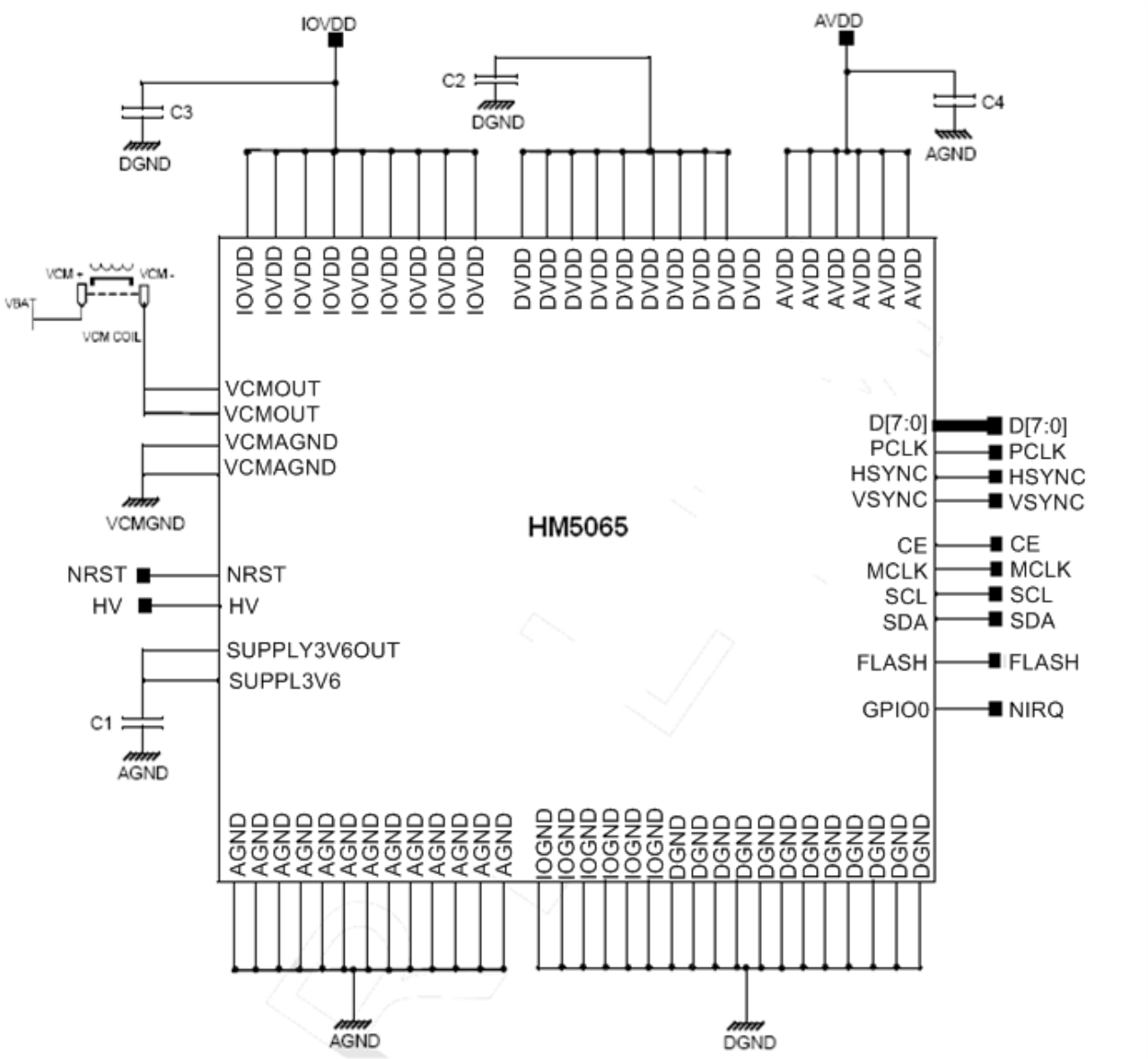


Figure 5 Parallel interface

Note:1 *Serial interface pull-up resistors should have a value based on the serial interface specification (typically 4.7K ohm).*

2 *C2, C3 and C4 should be kept as physically close to the die as possible.*

3 *Keep provision to connect CE to NSTANDBY or to ground at substrate level.*

3 Functional description

The HM5065 simplified block diagram is shown in **Figure 6** Simplified block diagram, with the following main blocks:

- 5 Megapixel pixel array
- Video pipe
- Statistics gathering unit
- Clock generator
- Microprocessor
- Video timing generator

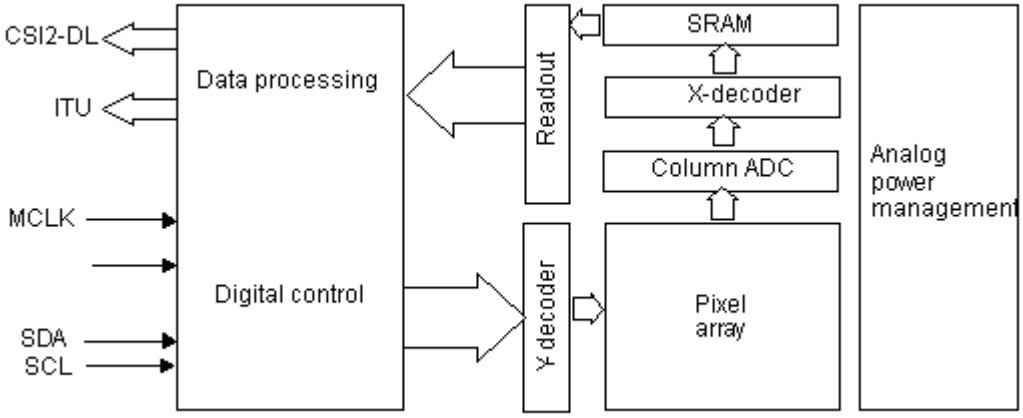


Figure 6 Simplified block diagram

3.1 Operation

A video timing generator controls a 5MP pixel array to produce raw Bayer images. The analog pixel information is digitized and passed into the video pipe. At the end of the video pipe, data is output to the host system over an 8-bit parallel interface along with qualification signals. Alternatively, data could also be output over the CSI2 dual lane interface.

The whole system is controlled by an embedded microprocessor that is running firmware stored in an internal ROM. The external host communicates with this microprocessor over a serial interface. The microprocessor does not handle the video data itself but is able to control all the functions within the video pipe. Real-time information of the video data is gathered by a statistics engine and used by the microprocessor. The processor uses this information to perform real-time image control tasks such as automatic exposure control.

3.2 Imaging pipe diagram

The details of the imaging pipe are shown in **Figure 8** Sensor array. The main functions contained within this diagram are detailed in this chapter.

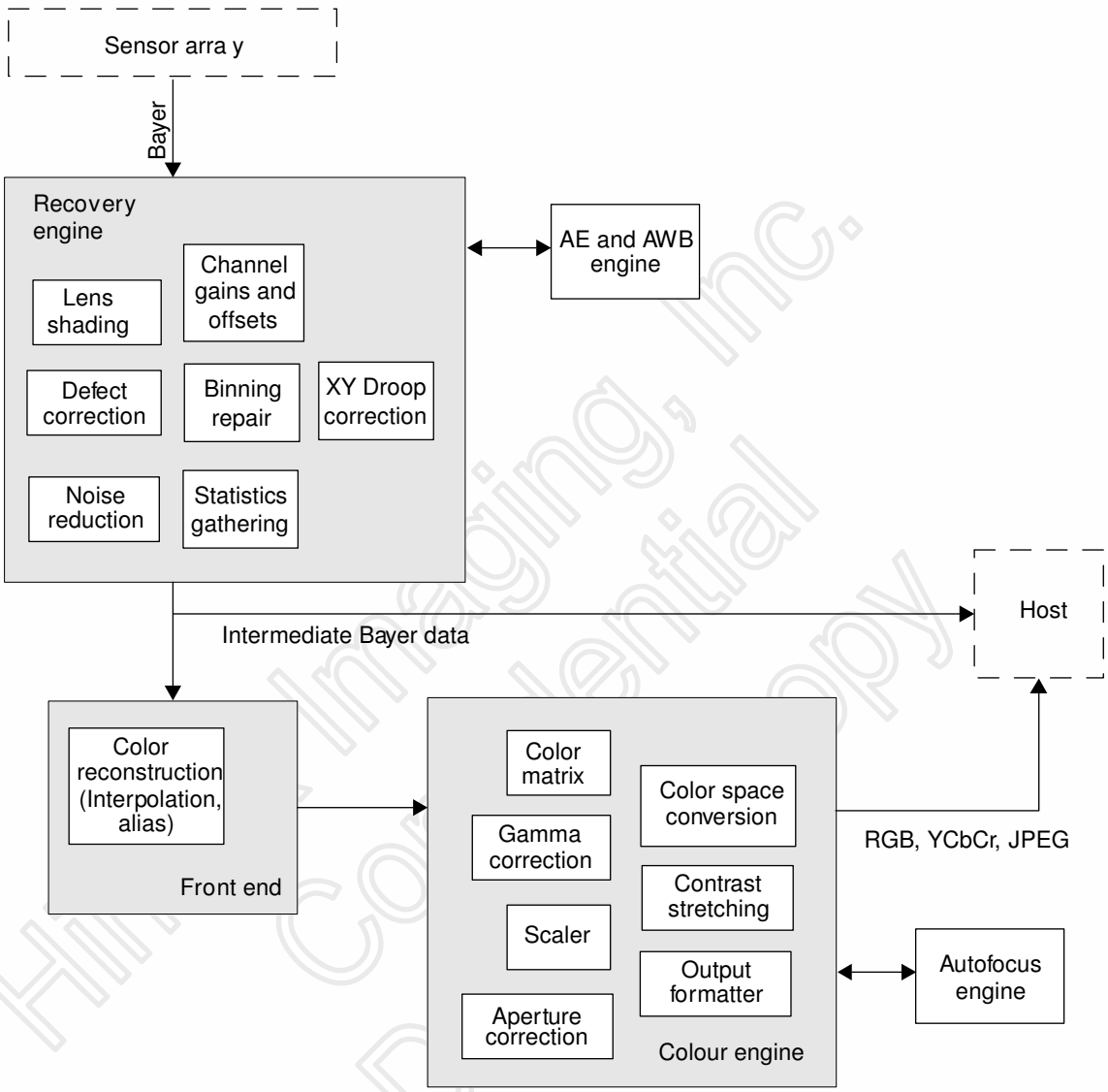


Figure 7 Imaging pipe block diagram

3.3 Sensor array

The HM5065 physical pixel array is 2608 x 1960 pixels (see **Figure 8** Sensor array), with a pixel size of 1.40µm by 1.40µm. The image size read from the array is mode dependent. For 5MP mode, the read out array size is 2592x1944.

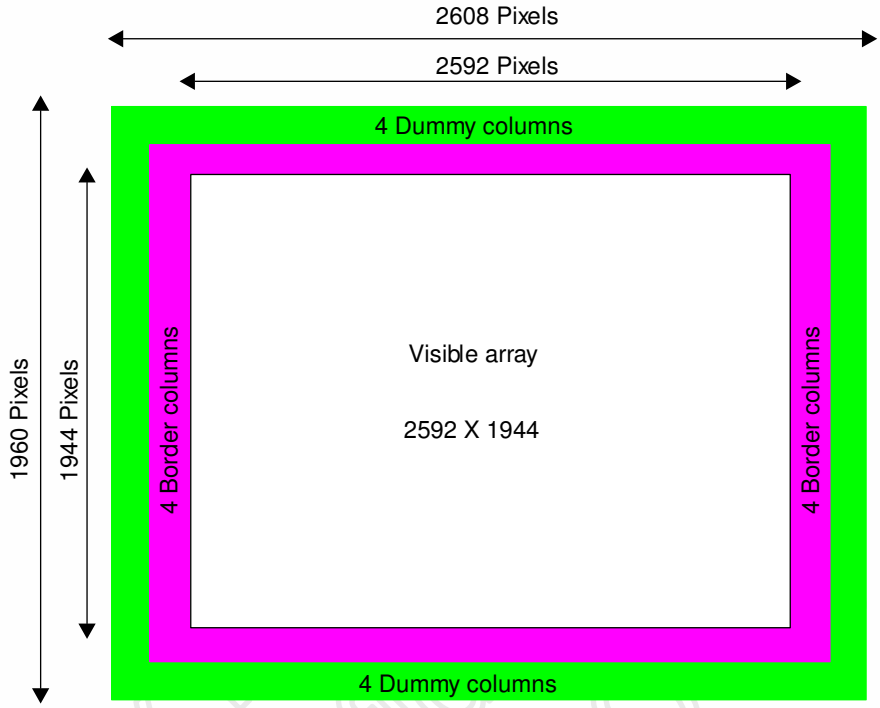


Figure 8 Sensor array

3.3.1 Sensor mode control

The HM5065 can operate the sensor array in few different modes controlled by register bSensorMode.

- SensorMode_5MP : The full array can be read out at 15 fps with JPEG.
- SensorMode_analogbinning_2x2 : A reduced power mode which uses the full array and a technique of analog binning output image at up to 30 fps.
- SensorMode_analogbinning_4x4 : A reduced power mode which uses the full array and a technique of analog binning output image at up to 60 fps.
- SensorMode_subsampling_2x2 : Uses the full array and a technique of sub-sampling output image at up to 30 fps.
- SensorMode_subsampling_4x4 : Uses the full array and a technique of sub-sampling output image at up to 60 fps.

3.3.2 Horizontal mirror and vertical flip

The image data output from the HM5065 can be mirrored horizontally or flipped vertically (or both).

3.4 Recovery engine (RE)

The RE is used to process raw Bayer input from the sensor array to an intermediate Bayer format which is white balanced and noise reduced, and can be supplied to the interpolation engine.

3.4.1 Channel offsets

To achieve the desired black level of Bayer pixel data it is often necessary to apply an offset to the data. This module provides the functionality to apply color channel dependent offset on active pixel data, that is, not dark or black data.

3.4.2 Channel gains

Color dependent gains are applied to active pixel data within this module as part of the automatic white balance function. The gain inputs are re-synchronized to the first active line.

3.4.3 Lens shading compensation

The lens shading is used to compensate for attenuation in the optical signal caused by primary and micro lens roll off. The module uses an advanced anti-vignette algorithm to adapt the lens correction based on lighting condition.

3.4.4 Defect correction

The input to the defect correction filters is a 3 x 3 pixel matrix from which a center pixel and a neighborhood of 8 pixels are extracted. The 8-pixel neighborhood is used to determine the validity of the corresponding center pixel.

3.4.5 Spatial noise reduction

The noise reduction algorithm is adaptive with light level and image content. The noise reduction module implements an algorithm that reduces perceived noise in an image whilst maintaining areas of high definition.

3.4.6 Interpolation

The interpolation module converts Bayer pixel data to RGB and applies an anti-alias filter to the data. It also generates the sharp data used in the aperture correction block.

3.5 Color engine (CE block)

The role of the CE is to process the RGB data from the recovery engine into a specific format requested by the host, for example, RGB565 for LCD display.

3.5.1 Color matrix

A matrix color correction transform is performed on the outputs of the scaler; the matrix is detailed in **Figure 9** Color matrix. The contents of the matrix are varied depending on lighting condition.

$$\begin{bmatrix} rcof00 & rcof01 & rcof02 \\ rcof10 & rcof11 & rcof12 \\ rcof20 & rcof21 & rcof22 \end{bmatrix}$$

Figure 9 Color matrix

The matrix equations are:

Ro = Rin.rcof00 + Gin.rcof01 + Bin.rcof02

Go = Rin.rcof10 + Gin.rcof11 + Bin.rcof12

Bo = Rin.rcof20 + Gin.rcof21 + Bin.rcof22

Note: The neutral-preserving (“Eigen-grey”) property of the matrix can be achieved by ensuring the matrix rows sum to unity.

3.5.2 Aperture correction

The aperture correction module is used to add a certain amount of sharpening to the scaled RGB data, which can be programmed to reduce as the light level drops. The aperture correction module also includes a function known as coring to allow control of the minimum magnitude which any edge on the image must exceed before sharpening is applied. This ensures that small edges such as noise are not amplified by the sharpening. The coring can be programmed to increase as the light level drops.

3.5.3 RGB scaling

The CE architecture includes an optional RGB scaler/smoothing module which produces an image fully compatible with existing image reconstruction techniques. This module is intended for use during viewfinder modes to provide a lower power image for display on LCD.

3.5.4 Special effects

The special effects module is used to apply simple transforms onto the input data. The supported effects are: Black and White, Negative, Solarising and Sketch. There are also a number of color effects which can only be applied to YCbCr data.

3.5.5 Zoom

The zoom function can be used to achieve a continuous zoom by simply selecting the commands **ZoomContinous_In**, **ZoomContinous_Out** and **ZoomStop**. It is also possible to perform a single step of zoom by selecting **ZoomStep_In** and **ZoomStep_Out**.

It is possible to zoom between the sensor size selected and the output size (the output size must be smaller than the sensor mode size).

3.5.6 Derating

The HM5065 contains an internal derating module. This is designed to reduce the peak output data rate of the device by spreading the data over the whole frame period and allowing a subsequent reduction in output clock frequency. Refer Section 0 for more information.

Note: *The interline period is not guaranteed to be consistent for all derating ratios. This means the host capture system must be able to cope with use of the sync signals or embedded codes rather than relying on fixed line counts.*

3.5.7 Gamma correction

The gamma module is a gain curve applied to each of the three image components from the sharpening module. There is a gamma control to allow the intensity of gamma correction to be modified.

3.5.8 YCbCr conversion

This module performs color space conversion from RGB to YCbCr. It is used to control the contrast and color saturation of the output image as well as the fade to black feature.

3.5.9 Dither

The dither block is used in RGB modes to reduce contouring in the image when the data is truncated to lower ranges. This is achieved by determining the error introduced by truncation and adding/subtracting this residual energy to/from the subsequent pixel.

3.6 Video compression module

The JPEG encoder receives YCbCr data from the image reconstruction engine and encodes it using baseline sequential JPEG technique. It outputs a standard JPEG data stream with all the required markers and segments required by decoders.

3.6.1 JPEG Features

- Supports YCbCr 4:2:2 as input data format.
- Baseline ISO/ IEC 10918-1 JPEG compliance.
- Programmable quantization tables.
- Capable of streaming the 5MP image at a rate of 15 frames per second.
- Manual / automatic compression control via scaled quantization tables.
- Automatic compression control targeted at file size and/or peak bit-rate.
- Progressive high-frequency roll-off option for increased compression.
- Intraframe rate-control via zig-zag sequence truncation.

Quantizer

Quantizer scales the DCT coefficients with programmable luminance and chrominance Q-tables. These Q-tables are programmed according to image characteristics, and modified by the squeeze setting. The larger the squeeze setting, the more severe the quantization and the greater the compression achieved.

Squeeze values can be manually set via **user squeeze mode**, or automatically set, and dynamically adjusted, by the **auto squeeze** module.

Entcoder16

The entcoder16 (entropy coder with 16-bit output) converts the quantized data stream to a symbol stream, including differential encoding of DC samples and run-length encoding of zero-valued AC samples according to the JPEG standard, and finally Huffman-encodes the symbol stream using hardwired baseline JPEG tables to compress the image. It also includes the JPEG header and embeds restart interval markers (if requested by nonzero restart interval setting) as per the JPEG standard.

Auto Squeeze

Auto squeeze is the VC's in-built dynamic compression control system. It adjusts the squeeze parameter based on measurements of two key criteria derived from the previous frame: output file size, and FIFO fullness. Squeeze is subsequently driven iteratively towards the optimal value, satisfying the two conditions:

1. FIFO stability, i.e. fullness has not exceeded a user-defined dead-zone, AND
2. Output file size <= a user-defined target.

3.6.2 JPEG compression

At the simplest level, the video compressor has one control which is the squeeze setting, which tells the system how hard to compress. A change in compression is achieved by scaling the quantization tables.

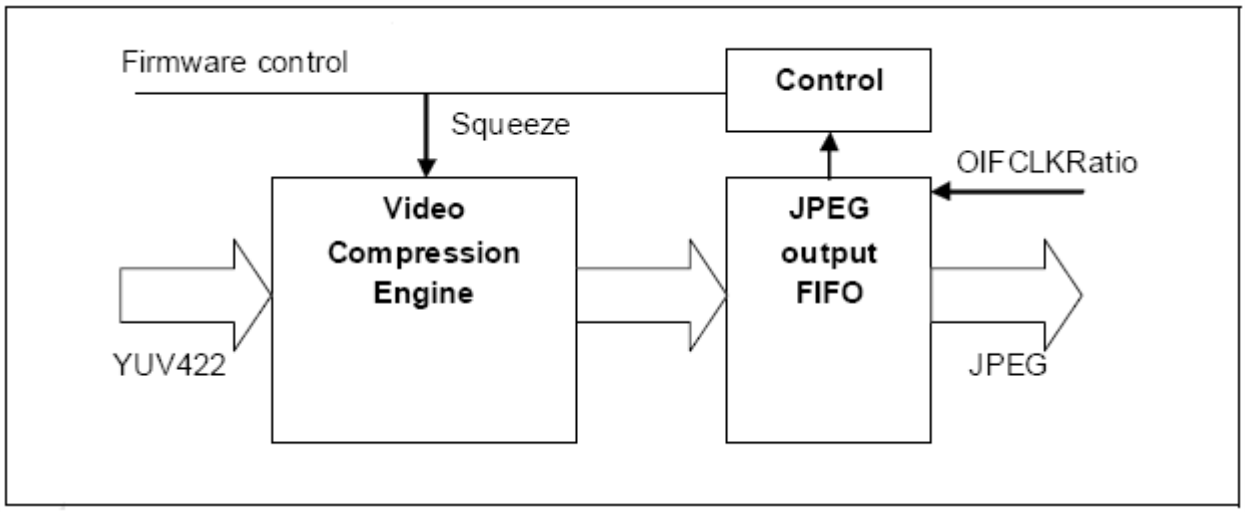


Figure 10 JPEG output

The FIFO shown in the figure above is being constantly monitored with fixed break points, if the FIFO fill state passes one of these break points the squeeze value is increased or decreased.

The amount of data in the FIFO is dependant on a number of factors:

- The squeeze factor set
- The complexity of the scene
- The speed at which the FIFO is being emptied (bOIFClkRatio)

3.6.3 JPEG squeeze controls

The strength of compression or the level of squeeze operated on the image (and therefore the quality of the final image) can be controlled in two ways via the **bJpegSqueezeSettings** register (note each context can be set independently);

bJpegSqueezeSettings {0x004d}

0x00 - User squeeze mode
0x01 - Auto squeeze mode

In auto squeeze mode, the JPEG compression engine is trying to achieve a target file size and constantly changes the compression ratio. This is the preferred mode when using the output JPEG to create a video, or in preview mode.

wJpegTargetFileSize {0x004e, 0x004f}: Input required size in KBytes

In user squeeze mode, the JPEG compression engine will use a constant level of squeeze. This is recommended when trying to capture a high quality image and for snapshot or flashgun modes. For ease of use, the level of squeeze can be adjusted for each pipe context between a high, medium or low level. The value of these squeeze settings can be configured by using the following registers:

bJpegImageQuality {0x0050}

0x00 - High quality. Value set in **bHiSqueezeValue {0x064b}**
0x01 - Medium quality. Value set in **MedSqueezeValue {0x064c}**
0x02 - Low quality. Value set in **bLowSqueezeValue {0x064d}**

3.6.4 JPEG output as a conventional frame

To keep compatibility with conventional frame format, the JPEG frame is output in a series of packets targeted to look like image lines. The Hsync envelopes each packet (line) of data and the Vsync envelopes the complete frame. The start of the frame is indicated by a transition of the Vsync and Hsync. This will occur when the output FIFO has accumulated enough JPEG data for the first line (default line size 512Bytes). When this line is output, it will then output blocks of blank data (16Byte blocks) until the next 512Bytes of data is available.

The number of bytes per line can be programmed using the following registers, both 16 bit registers should be programmed with the same value:

- **wLineLength { MSB 0x064e, LSB 0x064f}**
- **uwThres { MSB 0x0651, LSB 0x0652 }**

Note: *The number of PCLK in a line is equal to 2 times the line length. The maximum line length is 2K.*

In most cases the JPEG data will not fill the last line of data and padding data is added after the JPEG end of image marker **0xFFD9** filling the remainder of the last line. Note that it is possible that the JPEG data will exactly fill the line and no padding is required. The value of padding bytes is default to **0xA5**.

It is not possible to control the timing of the Vsync and Hsync signals in JPEG mode. User can however change the polarity of the signals and select if the Hsync is present or not during the interframe period.

PCLK can be made to be present during active JPEG data or during the interline or interframe periods. The rising edge of PCLK is always half clock delayed from both Hsync and Vsync.

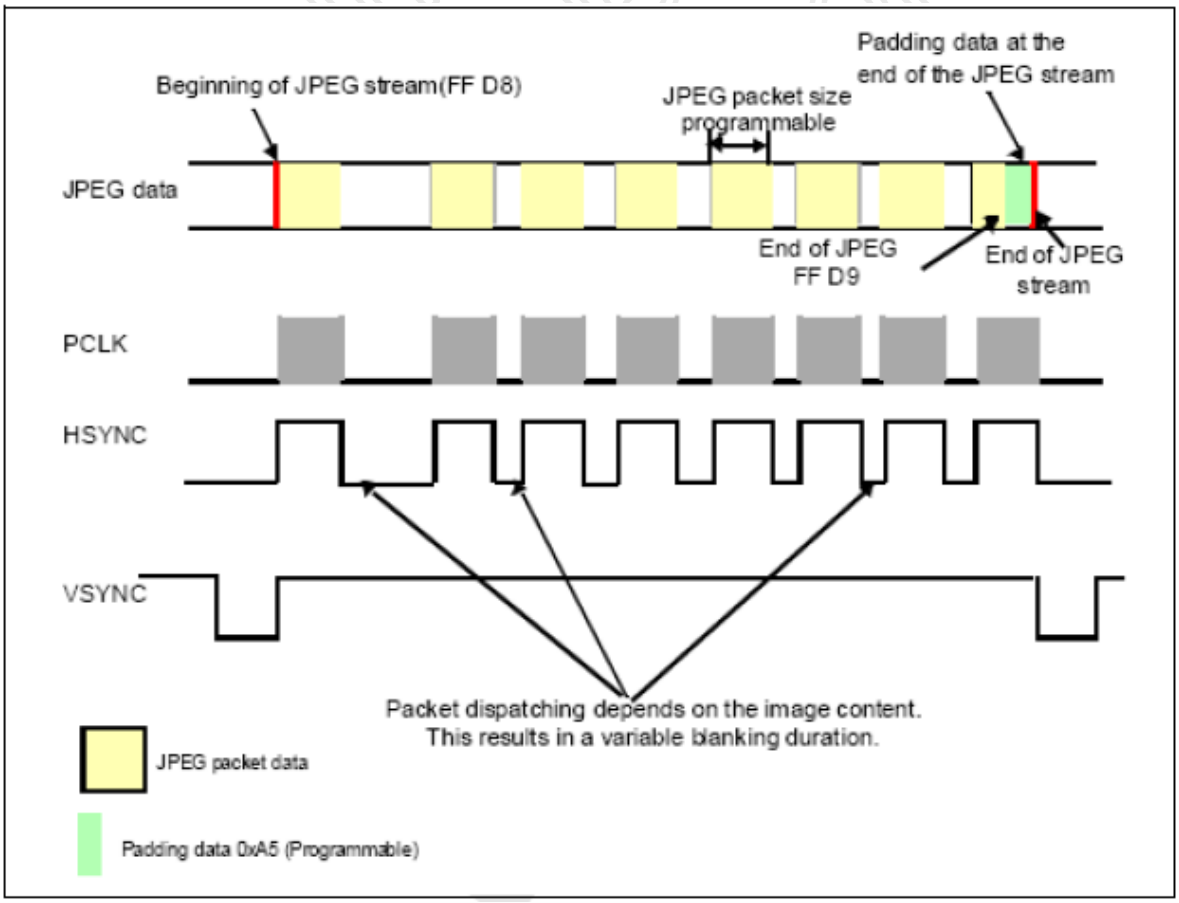


Figure 11 JPEG Frame

Note: *The minimum inter-packet (line) blanking time is 16 clock cycles, and is always a multiple of 16 clock cycles*

Marker Function	Name	Value
Start of Image	SOI	FFD8
Define Quantization Tables	DQT	FFDB
State of frame for baseline	DCT SOF	FFC0
Define Huffman Tables	DHT	FFC4
Start of Scan	SOS	FFDA
End of Image	EOI	FFD9

Table 8: JPEG data embedded markers

3.7 Microprocessor functions

The microprocessor inside the HM5065 is responsible for the control loop functions and handles the serial interface communication with the host processor. From this communication it allows the host control over the device via the User interface registers.

Dark Calibration

The microprocessor uses information from the array to ensure that the optimal and consistent 'black' level is achieved from the output.

Automatic Exposure Control

Using the information from the statistics gathering engine, the appropriate exposure settings for the scene is calculated and using a combination of exposure control, analog gain and digital gain the device will outputs a correctly exposed image. The host can program the exposure target within a range of EV values or can control the system manually setting a known exposure time, analog gain and digital gain.

HM5065 has a 16 bits register **uwDirectModeCodedAnalogGain** (0x0136/7) to control analog gain and Table 9 specifies the valid analog gain values.

Gain value (0x0136/ 0x0137)	Analog gain
0x0000	0.00 dB (x1.00)
0x0010	0.56 dB (x 1.07)
0x0020	1.16 dB (x1.14)
0x0030	1.80 dB (x1.23)
0x0040	2.50 dB (x1.33)
0x0050	3.25 dB (x1.45)
0x0060	4.10 dB (x1.60)
0x0070	5.00 dB (x1.78)

0x0080	6.00 dB(x2.00)
0x0090	7.20 dB (x2.29)
0x00A0	8.50 dB (x2.66)
0x00B0	10.10 dB (x3.20)
0x00C0	12.00 dB (x4.00)
0x00D0	14.50 dB (x5.31)
0x00E0	18.10 dB (x8.03)
0x00E4	19.20 dB (x9.12)
0x00E8	20.60 dB (x10.72)
0x00EC	22.10 dB (x12.74)
0x00F0	24.10 dB (x16.03)

Table 9: Analog gain control

Flicker Detection and Cancellation

The 50/60 Hz flicker frequency present in many lighting sources is visible when the integration time is not an integer multiple of this frequency. The HM5065 will adjust the integration time to ensure that the flicker effect is minimized

Note: *Flicker is present when using an integration time shorter than the period of the lighting frequency (less than 8.333 ms for 60 Hz, and less than 10 ms for 50 Hz).*

Contrast Stretching

This block stretches the histogram of the image to enhance the overall contrast, whereby an image with no saturated blacks or white is made darker and the light areas lighter. The strength of this stretch is controlled by registers **fpWhitePixTarget** (0x0574/5) and **fpBlackPixTarget** (0x0576/7).

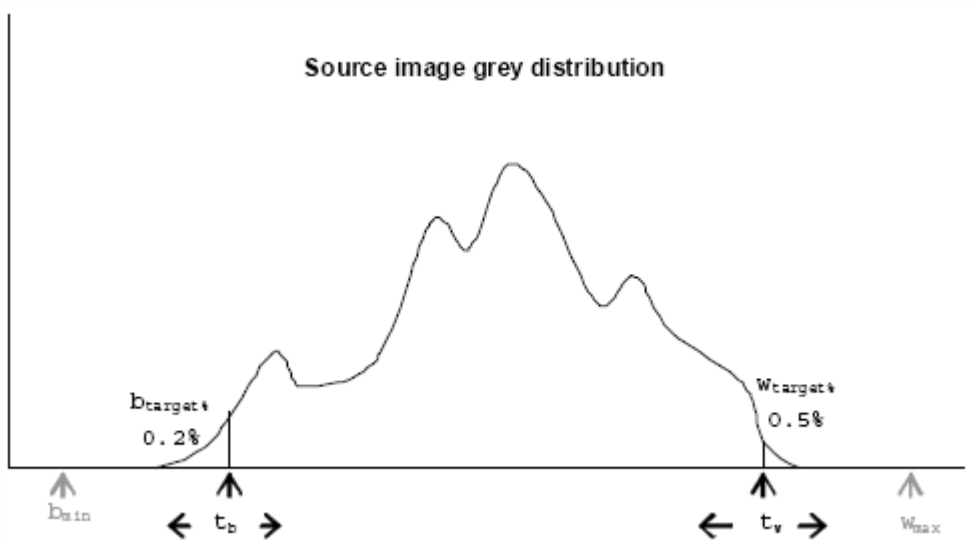


Figure 12 Example of a given histogram of an image before contrast stretching

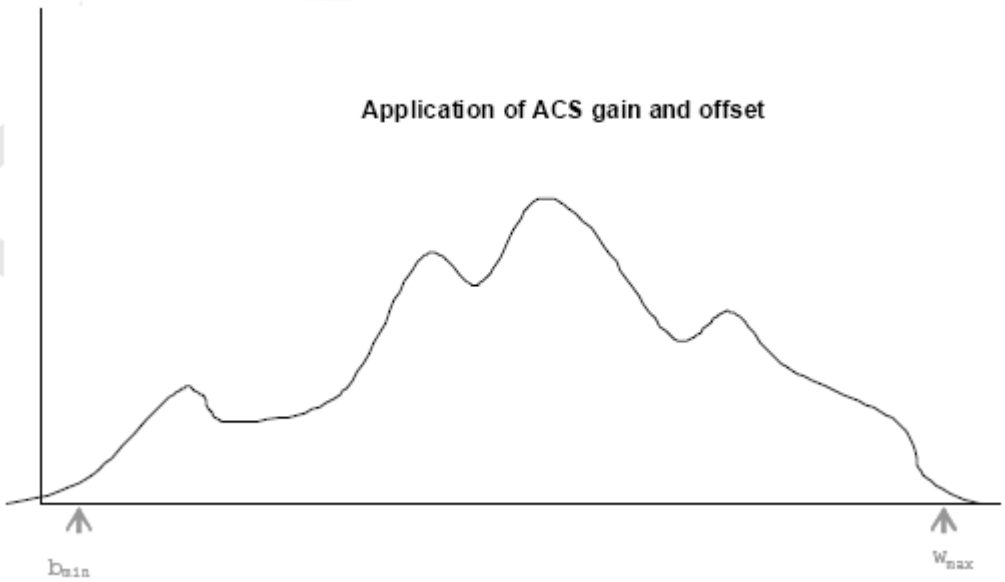


Figure 13 Histogram after contrast stretching

Automatic White Balance

Using the information output by the statistics gathering engine the microprocessor adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image. In addition to the standard white balance operation a constrainer operates on this information which ensures that the white balance achieved fits within the expected color temperature of real life illuminants.

Frame Rate Control

HM5065 contains a firmware based programmable timing generator. This automatically designs internal video timings, PLL multipliers, clock dividers, and so on to achieve a target frame rate with a given input clock frequency.

Optionally an automatic frame rate controller can be enabled. This system examines the current exposure status and adapts the frame rate based on this information. This function is typically useful in low-light scenarios where reducing the frame rate extends the useful integration period. This reduces the need for the application of analog and digital gain and results in better quality images.

Active Noise Management

The microprocessor is able to modify certain video pipe functions according to the current exposure settings determined by the automatic exposure controller. The main purpose of this is to improve the noise level in the system under low lighting conditions. Functions which 'strength' is reduced under low lighting conditions (for example, aperture correction) are controlled by 'dampers'. Functions which 'strength' is increased under low lighting conditions are controlled by 'promoters'.

Fade to Black

The microprocessor will fade the output signal to black to ensure that under the darkest conditions, when the image is not of sufficient quality, the device will output black. This operation is achieved by scaling the RGB to YCbCr matrix.

Auto Focus Algorithm

The auto focus operation is split into Algorithm layer and Driver layer. The Driver layer contains registers that set the appropriate operating range of the selected lens driver (e.g. VCM, piezo-actuator, etc.) The range can be determined through product characterization. Both registers **AF_OTP_uwHostDefMacro** (0x06cd, 0x06ce) and **AF_OTP_uwHostDefInfinity** (0x06cf, 0x06d0) are used to store Macro and Infinity positions respectively for the lens driver. Alternatively, host can choose to store these values in the OTP and they will be loaded automatically during sensor power up.

The Algorithm layer provides room to adjust various auto focus parameters such as lens movement, focusing accuracy (in terms of step size and algorithm), focusing range (macro, landscape, or normal mode), statistics zones, etc.

OTP Calibration Data

HM5065 supports retrieval of data from OTP (depending on register setting) for part-to-part calibration. These include anti-vignette parameters, color matrix parameters, and also the lens driver operating positions.

Interrupt Events

HM5065 supports five trigger events as follows:

a) Operating mode changed
b) Camera mode switched (switching of image pipes)
c) JPEG status updated
d) Number of frames output
e) AF locked

If any of the trigger events occurs, the corresponding bits in register **bInt_Event_Status** (0x000a) will be set. There is no auto-clear feature implemented in HM5065 – the external processor will need to write a '0' to clear the flag.

Note: *The interrupt statuses are only updated during sensor streaming.*

The sensor can be configured to generate external interrupt based on the triggering events. This external interrupt toggles the NIRQ pin which is active low. Register **bInt_Event_Enable** (0x000b) is used to select which events should toggle the NIRQ pin. The detail of interrupt events is described in .

Event	Description
Operating mode	This bit tracks any changes to sensor operation state, namely streaming and standby (stop).
Camera mode	This bit tracks any changes to image pipebank. Switching between pipebank0 and pipebank1 will triggered this flag. If auto focus is enabled, this bit also tracks the start and stop of auto focus algorithm.
JPEG status	If JPEG format is selected, this bit is set at the end of every JPEG frame output.
Number of frames output	This bit is set when the number(s) of frames required (through register **bRequiredStreamLength** (0x0015)) is streamed out.
Auto Focus locked	This bit indicates the auto focus algorithm is completed and the focused position is found.

Table 10: Description of interrupt events

3.8 Video pipe context configuration

3.8.1 Video pipe setup

The HM5065 has a single video pipe, the control of this pipe can be loaded from either of two possible setups Pipebank 0 and Pipebank 1;

Pipebank 0 and Pipebank 1 control the operations shown below:

- Image size
- Crop control
- Image format (for example, JPEG 4:2:2, YCbCr 4:2:2 and RGB565)

3.8.2 Context Switching

In normal operation, the image pipebank can be switched without the need to stop streaming. The change will occur at the next frame boundary after the change to the register has been made.

One sample application of this function is to stream an output targeting a display (for example, QQVGA RGB 444) then switch to capture an image with no need to stop streaming or enter any other operating mode.

It is important to note the output size selected for both image pipebanks must be appropriate to the sensor mode used, that is, to configure Pipebank 0 to QQVGA and Pipebank 1 to 5MP the sensor mode must be set to Fullsize mode.

The register **bActivePipeSetupBank** allows selection of the image pipebank, by default the Pipebank 0 is used.

3.8.3 ViewLive operation

ViewLive is an option which allows a different pipe context to be applied to alternate frames of the output data. The controls for ViewLive function are found in the register bank where the **fEnable {0x0013}** register allows the host to enable or disable the function.

When ViewLive is enabled the output data switches between Pipebank 0 and Pipe bank 1 on each alternate frame.

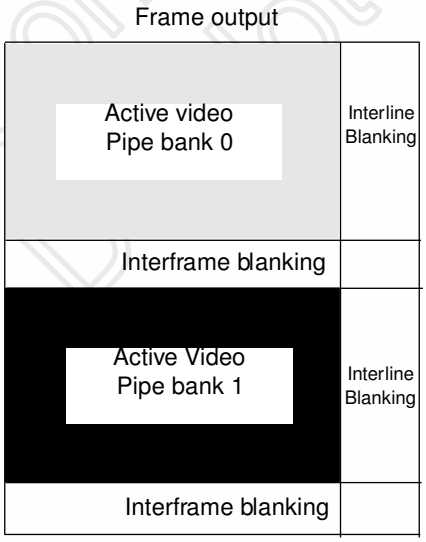


Figure 14 ViewLive frame output format

3.9 Operational Mode Control

The microprocessor allows high level control of the modes in which the HM5065 can operate. This avoids the need for the host to be concerned with the complexity of controlling the timing or power management during mode changes.

The HM5065 can operate only with internal generated VDD voltage supply. However, care must be taken on signaling and power up sequence to ensure proper sensor operation.

The VDD voltage is generated by internal regulator and this can be controlled with the CE pin. **Figure 15 State machine at power-up and user mode transitions** show the operational state machines with few control pins.

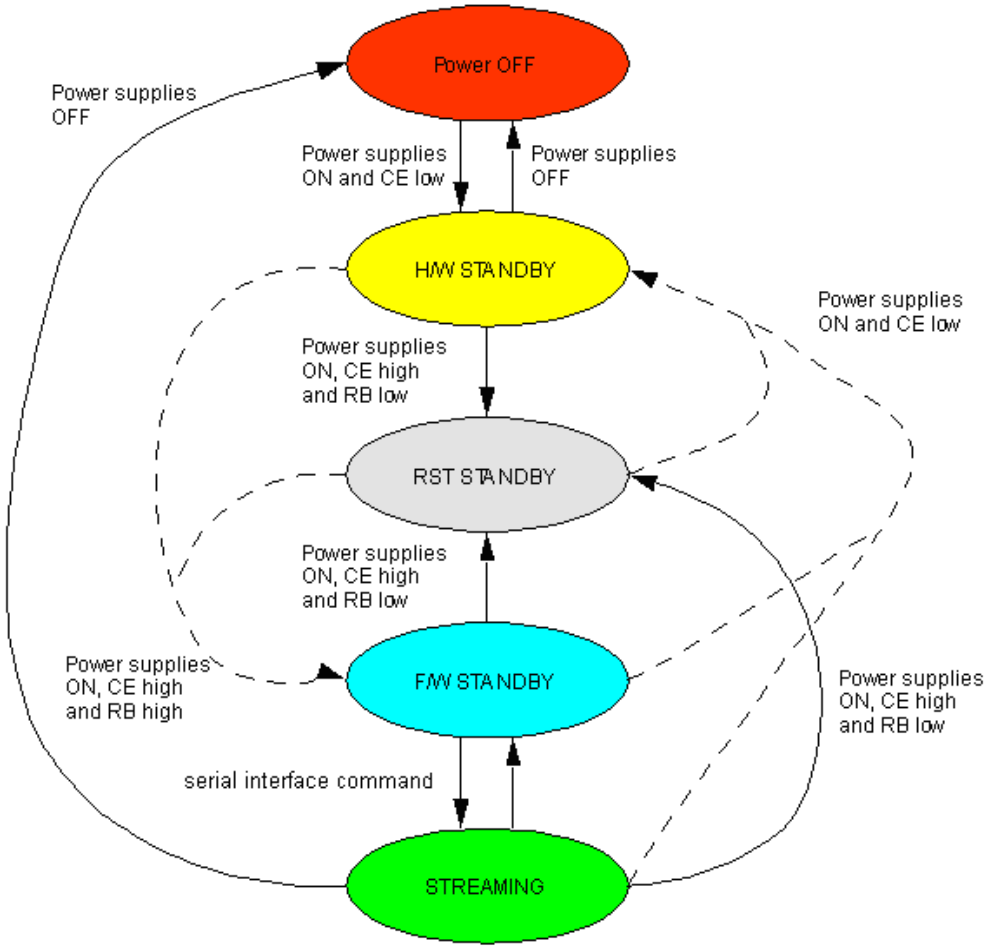


Figure 15 State machine at power-up and user mode transitions

The power-down mode is entered and exited by driving the hardware CE signal. Transitions between all other modes are initiated by serial interface transactions from the host system or automatically after time-outs.

Hardware Standby Mode

The HM5065 enters H/W STANDBY mode when the CE pin on the device is pulled low. Power consumption is very low most clocks inside the device are switched off.

In this state serial interface communication is not possible. The device I/O pins have a very high-impedance.

RST Standby Mode

The HM5065 enters RST STANDBY mode when the NRST pin on the device is pulled low. The NRST pin is internally 'AND' with the POR (power on reset).

All registers are reset to their default values.

F/W Standby Mode

The HM5065 enters F/W STANDBY mode when the CE pin on the device is pulled HIGH. Power consumption is low; most clocks inside the device are switched off. The POR reset happens when CE is enabled (high) and the device is reset to the default state, independent of the condition of the NRST pin. It is common to tie the NRST pin high to IOVDD and use only the CE line to control the reset of the device.

In this state serial interface communication is possible when CLK is present. The IO on the CLK is failsafe. The clock can be started at anytime but the F/W will not start to initialize until the clock is running.

Streaming Mode

This is the fully operational mode where the device outputs a continuous stream of images, according to the set image format parameters and frame rate control parameters.

Power Up Sequence

- CE pin is pull to logic 1
- The digital supplies must be on and stable.
- The internal digital supply of the HM5065 is enabled by an internal switch mechanism.
- All internal registers are reset to default values by an internal power on reset cell.

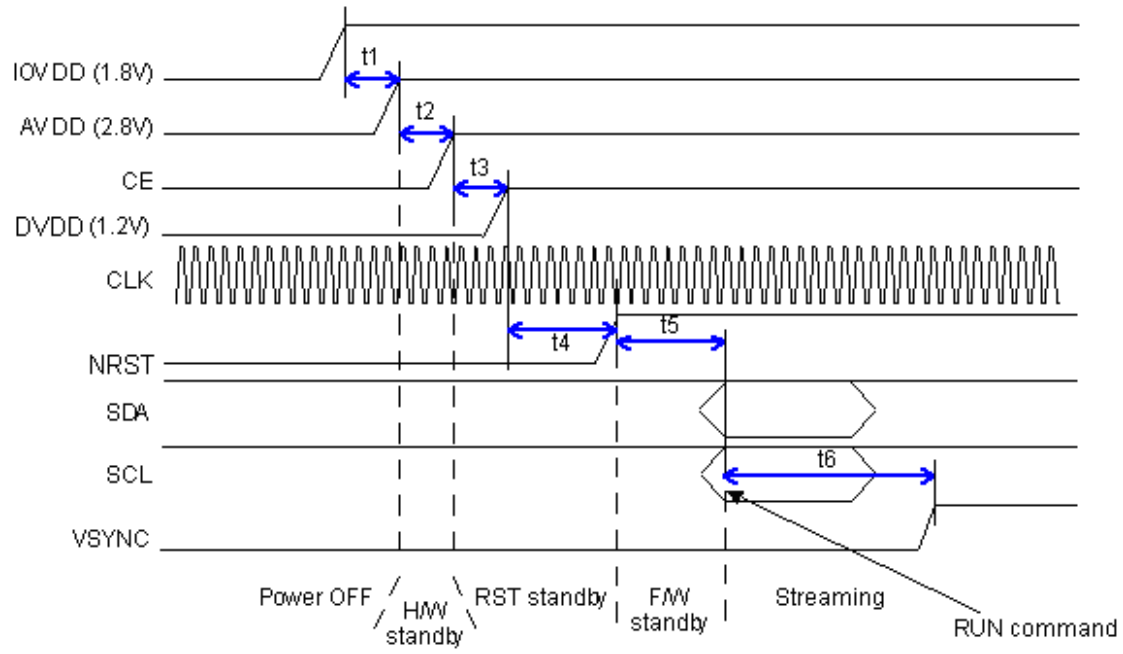


Figure 16 Power-up sequence

t1 >= 0 µs
t2 >= 0 µs
t3 <= 20 µs (this is the time for the internally generated 1.2V line to come up)
t4 >= 0 µs
t5 >= 30 ms (this is the time for the F/W to initialize, ready for a command)
t6 <= 10 ms

Note: *The first serial interface command could be a 'RUN' command if there is no firmware patching and sensor configuration necessary.*

ST recommends that no serial interface activity occurs during the transition (rising or falling) of the IOVDD.

Power Down Sequence

The power-down state is entered when CE is pulled low or the supplies are removed.

During the power-down state (CE = logic 0)

- The internal digital supply of the HM5065 is shut down by an internal switch mechanism. This method allows a very low power-down current value.
- The device input / outputs are fail-safe, and consequently can be considered high impedance.

3.10 Output format on ITU interface

The HM5065 supports the following data formats:

- JPEG 4:2:2
- YCbCr 4:2:2
- RGB565
- RGB555
- RGB444
- Bayer 10-bit

The required data format is selected using the **bDataFomat** control found in the pipe context registers.

3.10.1 Image size

An output frame consists of a number of active lines and a number of interframe lines. Each line consists of embedded line codes (if selected), active pixel data and interline blank data.

Note: *By default, interline blanking data is not qualified by the PCLK and therefore is not captured by the host system.*

Depending on the sensor mode, the image size can be either the full output from the sensor or a scaled output. The output image size can be selected from one of nine (9) pre-selected sizes or a manual image size can be used.

3.10.2 YCbCr data format

Two standard outputs are available – Rec 601 and JFIF, where

YCbCr Rec 601: Y = [16:235], CbCr = [16:240]
YCbCr JFIF: Y = [1:254], CbCr = [1:254]

YCbCr 422 data format requires 4 bytes of data to represent two adjacent pixels. ITU601-656 defines the order of the Y, Cb and Cr components as shown in **Figure 17** Standard YCbCr data order.

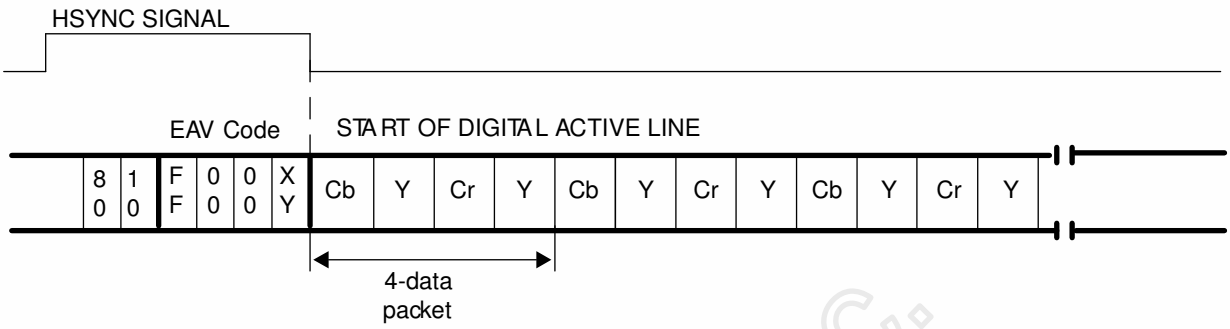


Figure 17 Standard YCbCr data order

The HM5065 **bYCbCrSetup** register can be programmed to change the order of the components as shown in **Figure 18** YCbCr data swapping options register bYCbCrSetup.f

	Bit [1] Y first	Bit [0] Cb first	Components order in 4-byte data packet 1st	2nd	3rd	4th
	1	0	Y	Cb	Y	Cr
DEFAULT	0	0	Cb	Y	Cr	Y
	1	1	Y	Cr	Y	Cb
	0	1	Cr	Y	Cb	Y

Figure 18 YCbCr data swapping options register bYCbCrSetup

3.10.3 RGB and bayer 10 bit data formats

The HM5065 can output data in the following formats:

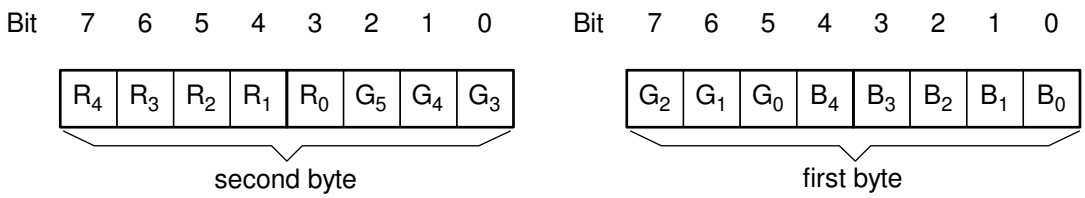
- RGB565
- RGB555
- RGB444
- Bayer 10-bit

Note: *Pixels in Bayer 10-bit data output are defect corrected, correctly exposed and white balanced. Any of all these functions can be disabled*

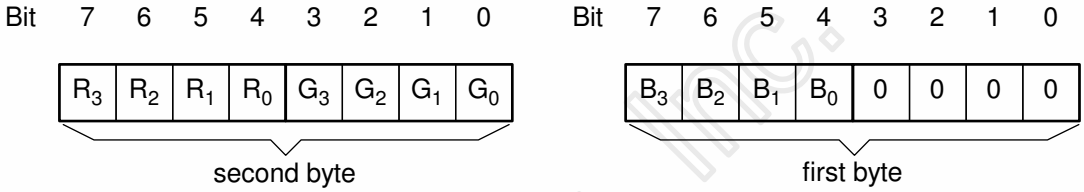
.

In each of these modes, 2 bytes of data are required for each output pixel. The encapsulation of the data is shown in **Figure 19 RGB data formats**.

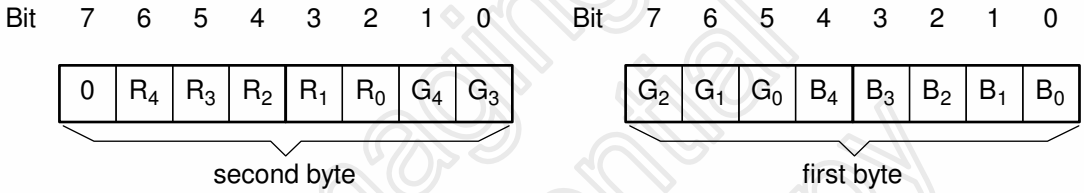
(1) RGB565 data packing



(2) RGB 444



(3) RGB 555



(4) Bayer 10-bit

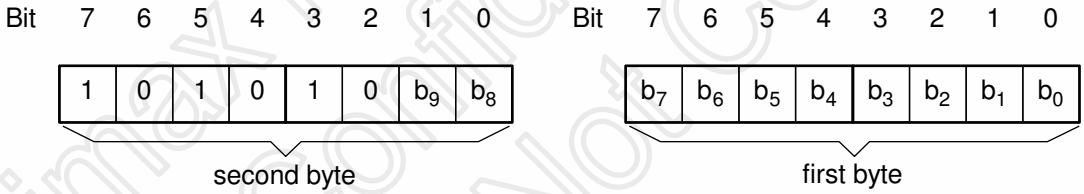


Figure 19 RGB data formats

Manipulation of RGB data

It is possible to modify the encapsulation of the RGB data in a number of ways:

- swap the location of the RED and BLUE data
- reverse the bit order of the individual color channel data
- reverse the order of the data bytes themselves

3.10.4 Line / frame blanking data

The values which are output during line and frame blanking are an alternating pattern of 0x10 and 0x80 by default.

3.11 Data synchronization methods

External capture systems can synchronize with the data output from HM5065 in one of two ways:

1. Synchronization codes are embedded in the output data (ITU656 compatible mode).
2. Via the use of two additional synchronization signals: VSYNC and HSYNC.

Both methods of synchronization can be programmed to meet the needs of the host system.

3.11.1 Embedded codes

The embedded code sequence can be inserted into the output data stream to enable the external host system to synchronize with the output frames. The code consists of a 4-byte sequence starting with 0xFF, 0x00, and 0x00. The final byte in the sequence is based on definition shown in **Table 11** and **Table 12**.

Prevention of false synchronization codes

The HM5065 is able to prevent the output of 0xFF and/or 0x00 data from being misinterpreted by a host system as the start of synchronization data.

3.11.2 ITU656 compatible mode

The structure of an image frame with 656 codes is shown in **Figure** 20.

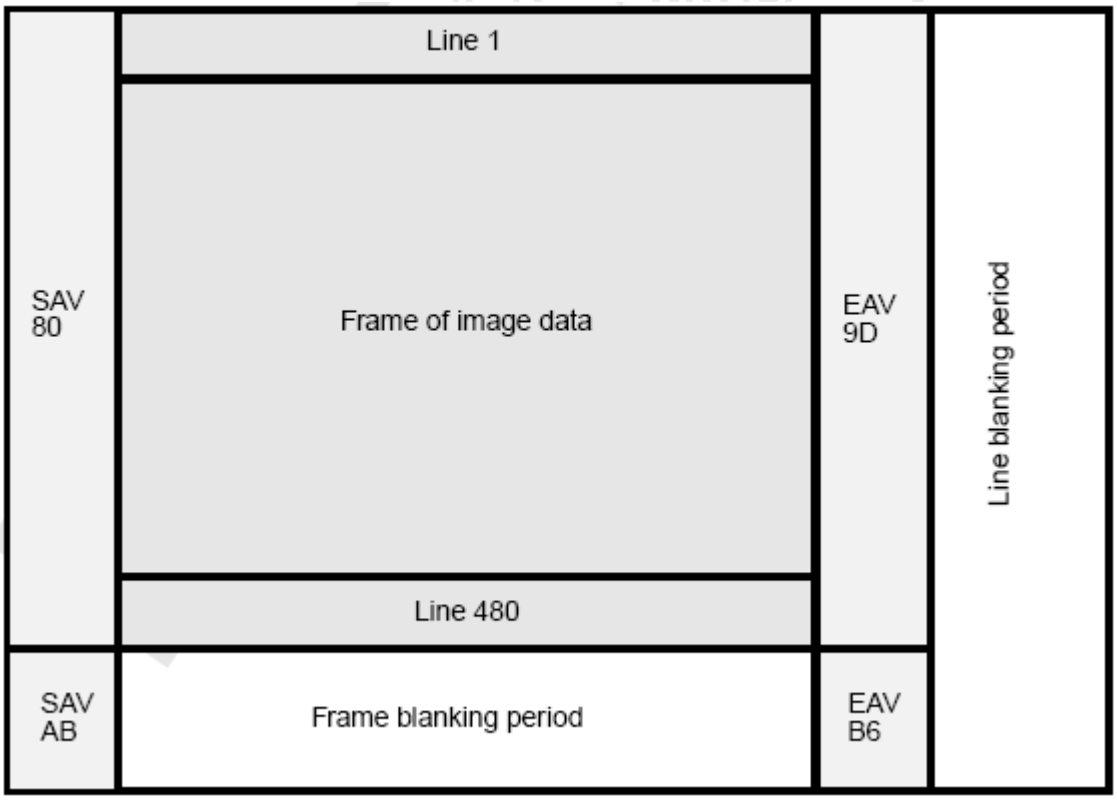


Figure 20: 656 frame structure with even codes

The synchronization codes for odd and even frames are listed in **Table 11** and **Table 12**. By default all frames output from the HM5065 are EVEN. It is possible to set all frames to be ODD or to alternate between ODD and EVEN.

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 80
EAV	Line end - active	FF 00 00 9D
SAV (blanking)	Line start - blanking	FF 00 00 AB
EAV (blanking)	Line end - blanking	FF 00 00 B6

Table 11: ITU656 embedded synchronization code definition (even frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 C7
EAV	Line end - active	FF 00 00 DA
SAV (blanking)	Line start - blanking	FF 00 00 EC
EAV (blanking)	Line end - blanking	FF 00 00 F1

Table 12: ITU656 embedded synchronization code definition (odd frames)

3.11.3 VSYNC and HSYNC

The HM5065 can provide two programmable hardware synchronization signals: VSYNC and HSYNC. The position of these signals within the output frame is automatically set where the signals track the active video portion of the output frame regardless of its size.

Horizontal synchronization signal (HSYNC)

The HSYNC signal can be controlled. The following options are available:

- enable/disable
- select polarity
- all lines or active lines only

The HSYNC signal envelops all the active video data on every line in the output frame regardless of the programmed image size. Line codes (if selected) fall outside the HSYNC envelope as shown in **Figure 21** HSYNC timing example.

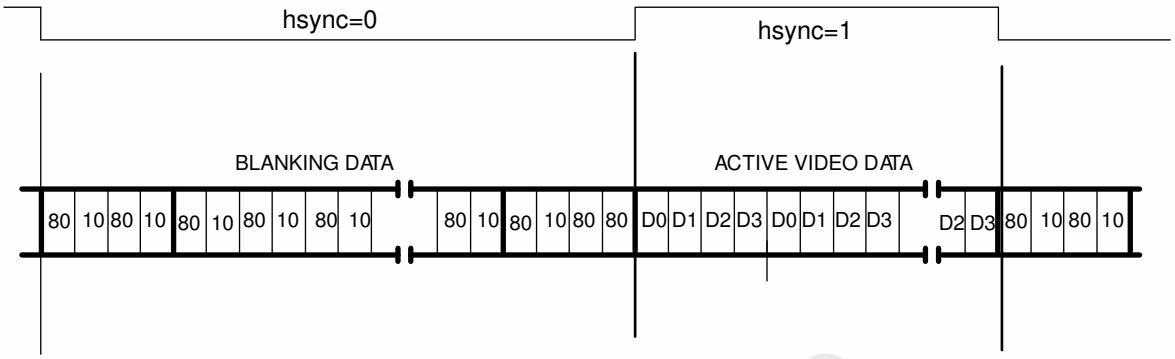


Figure 21 HSYNC timing example

Vertical synchronization (VSYNC)

The VSYNC signal can be controlled. The following options are available:

- enable/disable
- select polarity

The VSYNC signal envelops all the active video lines in the output frame regardless of the programmed image size as shown in **Figure 22 VSYNC timing example**.

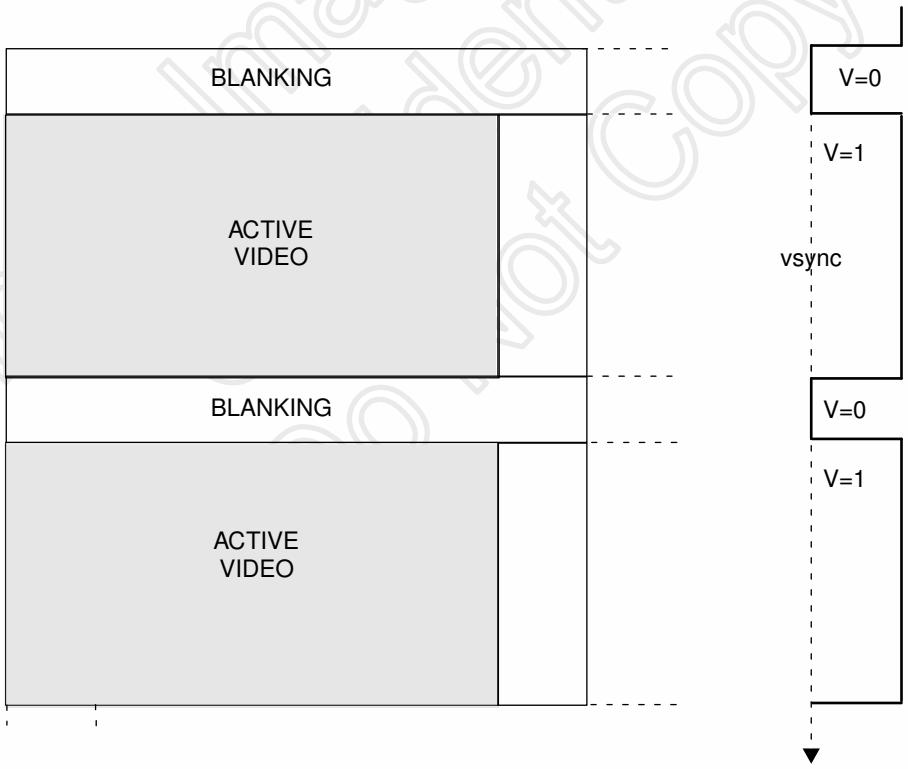


Figure 22 VSYNC timing example

3.11.4 Pixel clock (PCLK)

The PCLK signals synchronize the data between the host and the receiver. The following options are available:

- enable/disable
- enable/disable during vertical/horizontal blanking

Note: *If PCLK is disabled during vertical or horizontal or both blanking, there will be trailing of 4 clocks occurred before and after the VSYNC/HSYNC transition.*

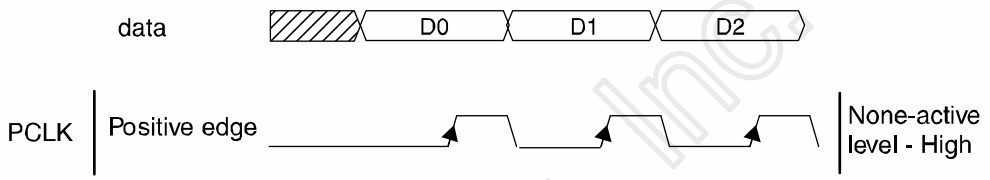


Figure 23 PCLK options

The YCbCr and RGB timings are represented in **Figure** 24, with the associated qualifying PCLK clock.

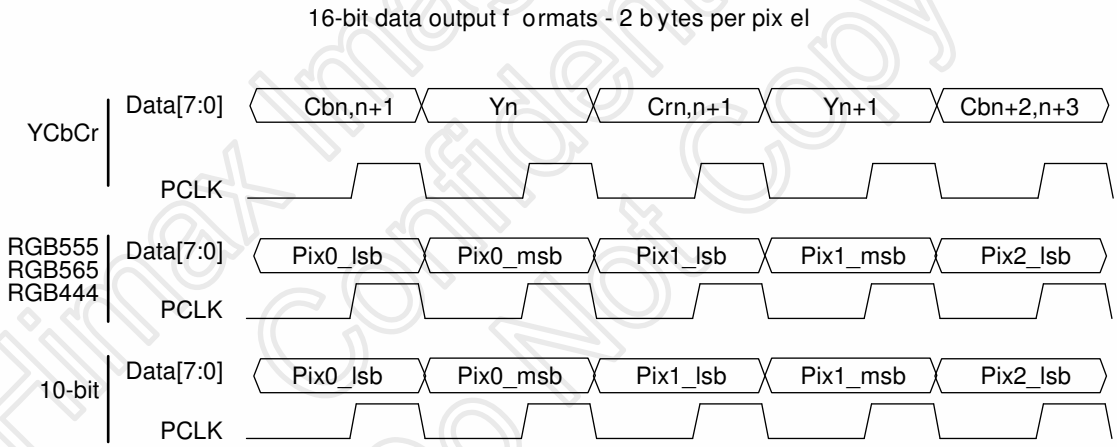


Figure 24 Qualification clock

In practice, the user may be required to write some additional setup information prior to receiving the required data output.

3.11.5 Derating

When the scaler is operating, the clock manager employs derating to reduce the peak output rate of the device by spreading the data over the full frame period.

The derating employed for some resolution is shown in **Table 13**.

Mode	Resolution			Derating ratio
SR[1]	5MP	2592	1944	1
	UXGA	1600	1200	1
	XGA	1024	768	1
	SVGA	800	600	2
	VGA	640	480	4
	CIF	352	288	4
	QVGA	320	240	8
Subsampling 2x2 Analog Binning 2x2[2]	XGA	1024	768	1
	SVGA	800	600	1
	VGA	640	480	2
	CIF	352	288	2
	QVGA	320	240	2
	QCIF	176	144	4
	QQVGA	160	120	4
Subsampling 4x4 Analog Binning 4x4[3]	VGA	640	480	1
	CIF	352	288	1
	QVGA	320	240	1
	QCIF	176	144	2
	QQVGA	160	120	2

Table 13: Sample derating values

The output PCLK rate is calculated as:

$$PCLK = \frac{PCLK_{max}}{\text{Derating ratio}}$$

Note: When outputting image data in JPEG format, the duty cycle of PCLK changes slightly with the clock ratio set to 3. Host should expect the resultant PCLK to carry a duty cycle of 33% in this case. Other clock ratios are not affecting the PCLK duty cycle. The derating ratio can be limited using the **bClockRatio** register.

[1]Single read mode (full 5MP: 2608 x 1960 array).

[2]Subsampling / Analog binning 2x2 mode (1304 x 980 array).

[3]Subsampling / Analog binning 4x4 mode (652 x 490 array).

3.12 Timing control

3.12.1 Input clock

The HM5065 requires an external reference clock. The external clock should be a DC coupled square wave and may have been RC filtered. The clock input is fail-safe in power down mode.

The HM5065 contains an internal PLL allowing it to produce accurate frame rates from a wide range of input clock frequencies. This also allowed the input clock to be much lower than the system clock. The input range is from 6 MHz to 27 MHz. The external clock frequency register must be programmed accordingly.

3.12.2 PLL operation

The HM5065 contains a firmware based programmable timing generator which automatically configures the internal video timing, PLL multipliers and clock dividers to achieve a target operation. The timing generator is controlled and constrained by the required PLL frequency, frame rate and scaling factor, this in turn affects the output PCLK frequency.

Timing control

The HM5065 can be configured to allow sensor to meet the input frequency constraints of a host application. The **fpTargetPllOutputFrequencyMhz** register sets required the maximum frequency generated by the system clock manager and therefore limits the output frequency and is based on the following equation:

$$fpTargetPllOutputFrequencyMhz = 2 \bullet PCLK_{max}$$

The $PCLK_{max}$ may be a limitation on the host and using the following approximate calculation can help work out the framerate achievable with this output PCLK rate;

$$Framerate = \frac{PCLK_{max}}{\text{Image size} \bullet \text{data format} \bullet 1.10}$$

- Image size = 2592 x 1944 for 5MP sensor mode
- Data format = 2 for YCbCr 4:2:2 and RGB (as these are 2 Bytes per pixel)
- (1.10) is an increase of 10% to take into account interline and interframe.

3.13 Spread Spectrum Clock Generator

The PLL contains an Spread Spectrum Clock Generator block (SSCG) effective for EMI reduction. This feature is off by default and is intended for use if channel blocking becomes an issue on the baseband platform.

A primary source of EMI is the high speed CSI serial data link. The modulation period and depth are fully programmable. The spread mode is selectable between center spread (default) or down spread. The default register settings produce a setup which introduces +/- 0.25% (minimum) center spreading with a modulation period of the sensor line length. The SSCG registers can only be reprogrammed with new values when the sensor is in software standby mode.

Index	Byte	Register name	Data type	Default	Type	Comment
0x30c0	HI	sscg_mod_period	16UI	0x00 0x00	RW	Bit[12:0] 13-bit modulation period.
0x30c1	LO					
0x30c2~ 0x30c3	-	-	-	-	-	Reserved.
0x30c4	HI	sscg_inc_step	16UI	0x00 0x00	RW	Bit[14:0] 15-bit modulation depth
0x30c5	LO					
0x30c6~ 0x30c7	-	-	-	-	-	Reserved.
0x30c8		sscg_strb	8UI	0x00	RW	Trigger to strobe mod_period and inc_step and spread control together: 0x00: No strobe input 0x01: Asynchonous strobe input (0x01 -> 0x00)[7]
0x30c9~ 0x30cb	-	-	-	-	-	Reserved.
0x30cc		sscg_strb_bypass	8UI	0x00	RW	Strobe bypass: 0x00: No bypass 0x01: Bypass inputs without registering the strobe signal
0x30cd~ 0x30cf	-	-	-	-	-	Reserved.
0x30d0		sscg_spread_control	8UI	0x01	RW	Spread mode: 0x00: Center spread 0x01: Down spread
0x30d1~ 0x30d3	-	-	-	-	-	Reserved.
0x30d4		sscg_control	8UI	0x00	RW	Spread spectrum modulation: 0x00: Disable 0x01: Enable

Table 14: Spread spectrum clock generator settings - [0x30c0 - 0x30d4]

[7] Strobing signal needs at least two FBCLK (feedback clock of PLL) clock cycles where FBCLK = PLL output freq / PLL divider.

3.13.1 Setting up the SSCG

When SSCG is enabled, a triangular modulation profile will be generated at the PLL output. The maximum modulation frequency is governed by PLL bandwidth, which has to be at least five times the modulation frequency. If the modulation frequency exceeds the limitation, distorted triangular profile will be observed at the PLL output.

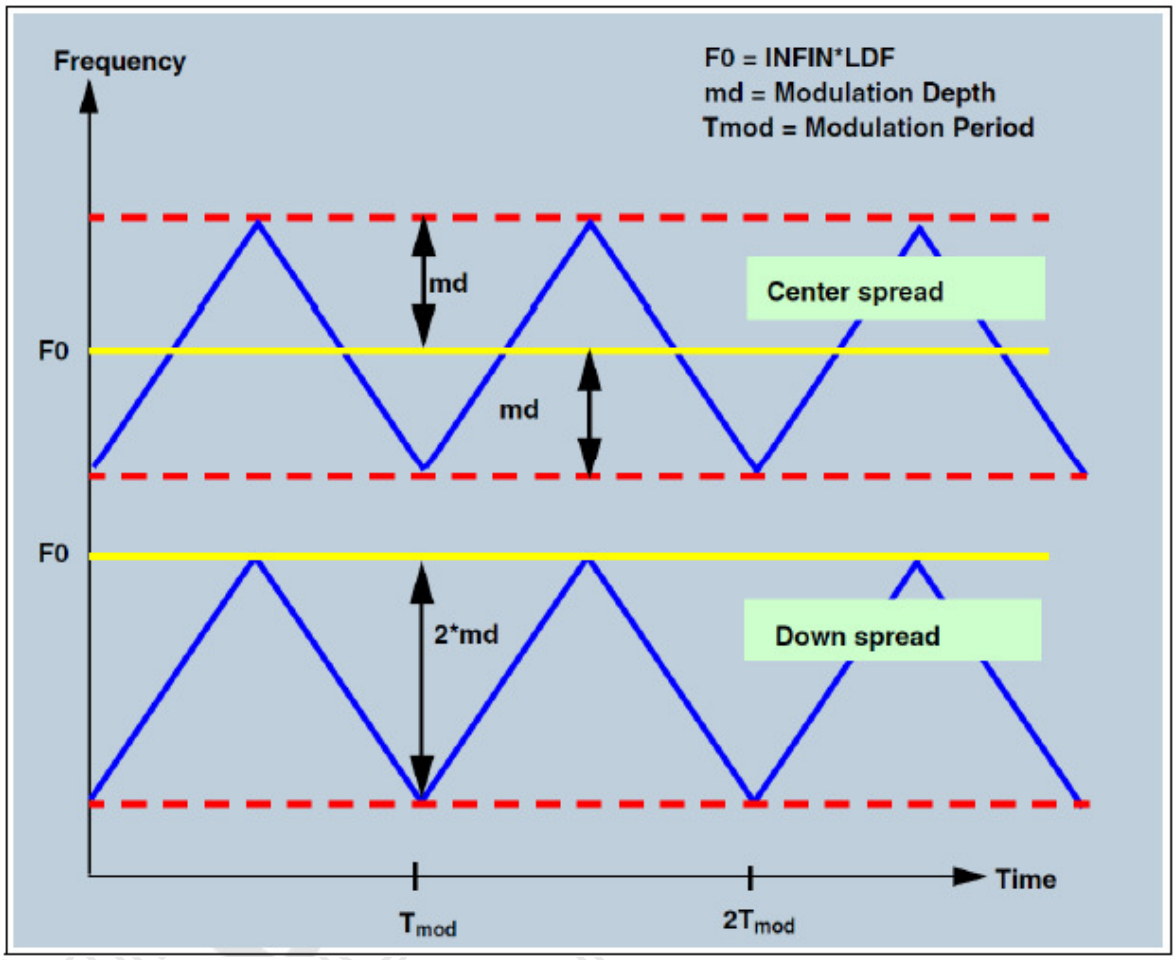


Figure 25 SSCG PLL output in the center and down spread modes

Note: *The **sscg_mod_period** and modulation depth (**sscg_inc_step**) should be set before activating the modulation.*

Setting up the SSCG involves few registers which are calculated as follows:

$$\text{sscg\_mod\_period} = \text{round}\left(\frac{\text{feedback clock of PLL when locked}}{4 * \text{modulation frequency}}\right)$$

$$\text{sscg\_inc\_step} = \text{round}\left(\frac{(2^{15} - 1) * \text{peak modulation depth (\%)} * \text{PLL divider}}{100 * 5 * \text{sscg\_mod\_period}}\right)$$

where $\text{sscg\_inc\_step} * \text{sscg\_mod\_period} < 2^{15} - 1$

$$\text{modulation depth (quantized)} = \frac{\text{sscg\_mod\_period} * \text{sscg\_inc\_step} * 100 * 5}{(2^{15} - 1) * \text{PLL divider}} \%$$

3.13.2 Sample SSCG setup

Assume the HM5065 has the following parameters:

- External clock = 12 MHz
- Target PLL output frequency = 714 MHz

Resulting in the PLL divider setting = 714 / (12 / 2) = 119

Assume the target modulation frequency of 24 kHz is desired with a modulation depth of +/- 2.0% (center spread). Hence,

sscg_mod_period = round (feedback clock of PLL / (4 * modulation frequency))
sscg_mod_period = round (12 / 2 MHz / (4 * 24 kHz))
sscg_mod_period = round (62.5) = 63

sscg_inc_step = round ((2^{15} - 1) * modulation depth * PLL divider / (5 * 100 * sscg_mod_period))
sscg_inc_step = round ((2^{15} - 1) * 2 * 119 / (5 * 100 * 63))
sscg_inc_step = round (247.57) = 248

To ensure parameters are within range:
sscg_mod_period * **sscg_inc_step** = 63 * 248 = 15624 (less than 2^{15} - 1).

mod. depth (quantized) = sscg_mod_period * sscg_inc_step * 100 * 5 / ((2^{15} - 1) * PLL divider) %
mod. depth (quantized) = 63 * 248 * 100 * 5 / ((2^{15} - 1) * 119) %
mod. depth (quantized) = 2.00345%
Thus, error in modulation depth = 2.00345 - 2.00 = 0.00345%

If sscg_mod_period = 64 is chosen, then

sscg_inc_step = 244
mod. depth (quantized) = 2.00243
error in modulation depth = 0.00243%

The above calculations show that the quantization error in the modulation depth depends on the flooring and rounding of **sscg_mod_period** and **sscg_inc_step**. For this reason, both parameters should be judiciously rounded/floored to minimize the quantization error in the modulation depth.

With these values, registers should be updated with following sequence:

1. fpTargetPllOutputFrequencyMhz (registers 0x00b2/0x00b3) = 714.0
2. sscg_mod_period (registers 0x30c0/0x30c1) = 63
3. sscg_inc_step (registers 0x30c4/0x30c5) = 248
4. sscg_spread_control (register 0x30d0) = 0
5. sscg_strobe (register 0x30c8) = 1
6. wait for 2 clock cycles of FBCLK (feedback loop clock of PLL)
7. sscg_strobe (register 0x30c8) = 0
8. sscg_control (register 0x30d4) = 1

4 Camera Serial Interface

The video stream which is output from the HM5065 via the Camera Serial Interface (CSI) on dual lane contains both video data and other auxiliary information. This section describes the frame and line formats and their embedded control codes. The HM5065 is MIPI CSI-2 v0.90 compliant and it is backward compatible with v0.65.

4.1 Functional Layers

- CSI-2 uses MIPI D-PHY as the physical layer with two power levels
  - High Speed (HS)
  - Low Power (LP)
- The physical layer comprises of
  - One clock lane and two data lanes
  - Unidirectional clock lane supporting Ultra Low Power Mode (ULPM)
  - Unidirectional data lane supporting ULPM (using forward escape mode)
  - Power on/off and reset sequences are defined as transitions to/from ULPM

The CSI-2 functional layer implemented in HM5065 is described by **Figure** 26.

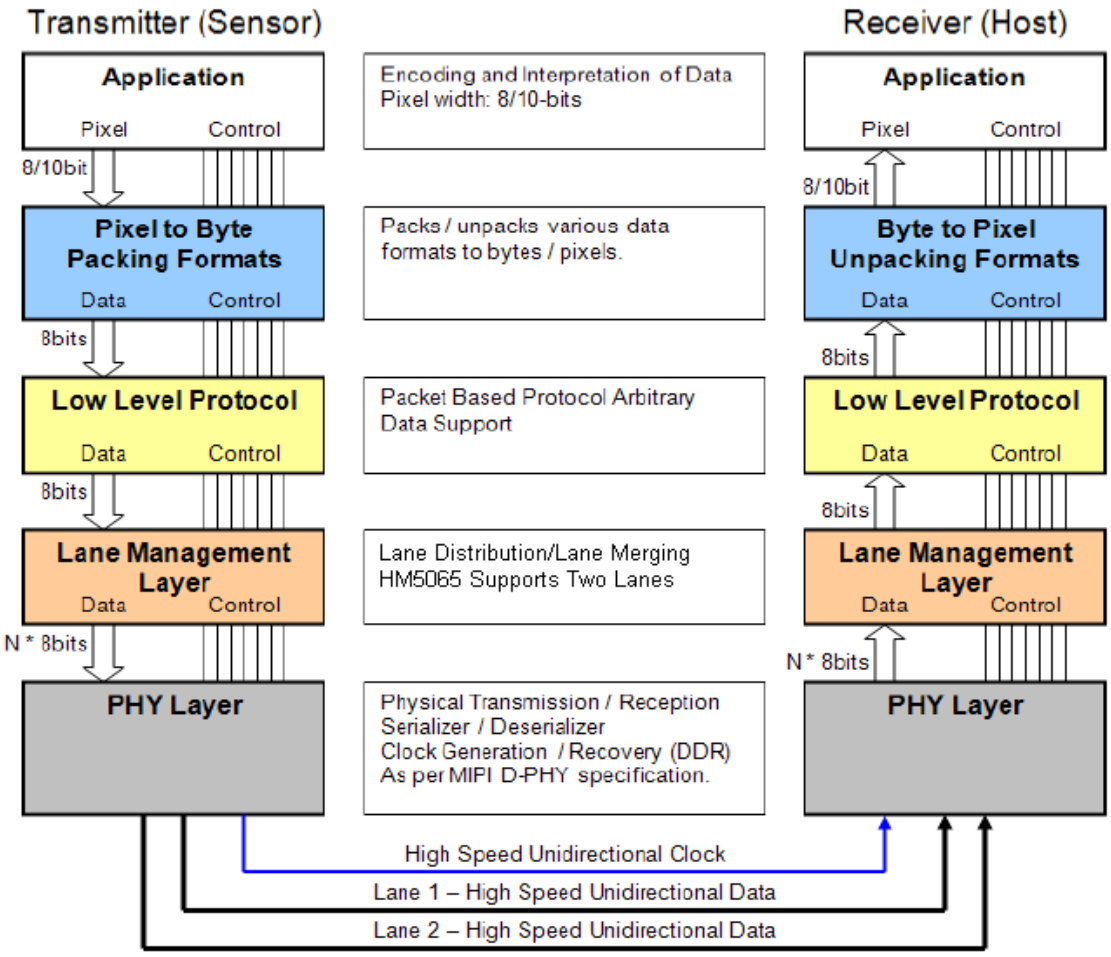


Figure 26 CSI-2 functional layers

4.2 Line Voltages

- High-speed signalling below MOS threshold level
  - Enables independent operation of High Speed (HS) and Low Power (LP)
- Full-swing level 1.2V
  - Required for low power operation

The MIPI D-PHY line voltages are described by **Figure 27** Line voltages and the implementation is described in **Figure 28** Driver Implementation.

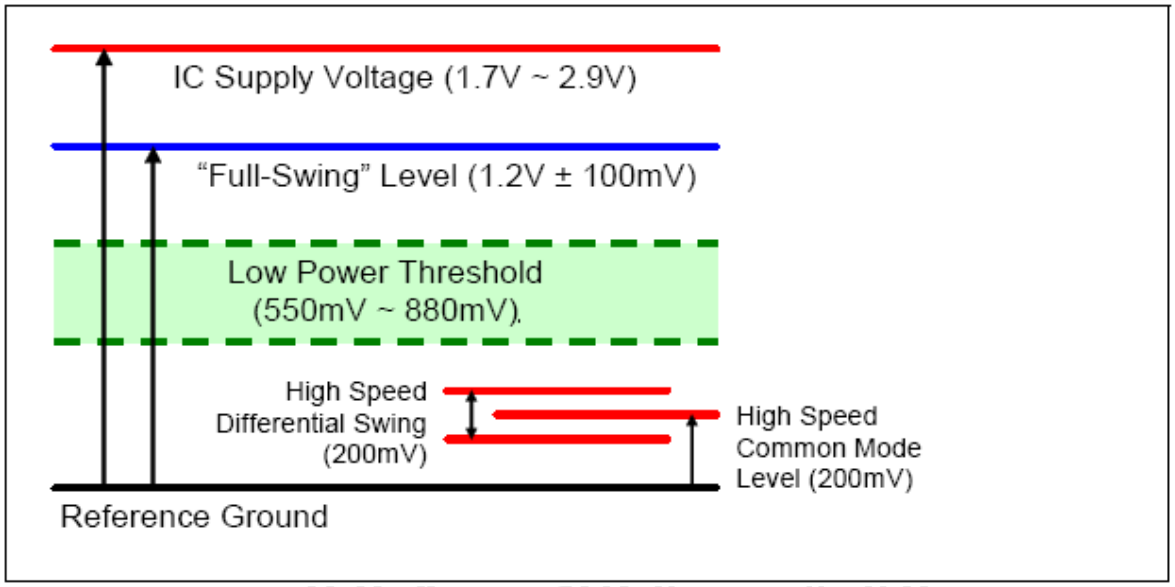


Figure 27 Line voltages

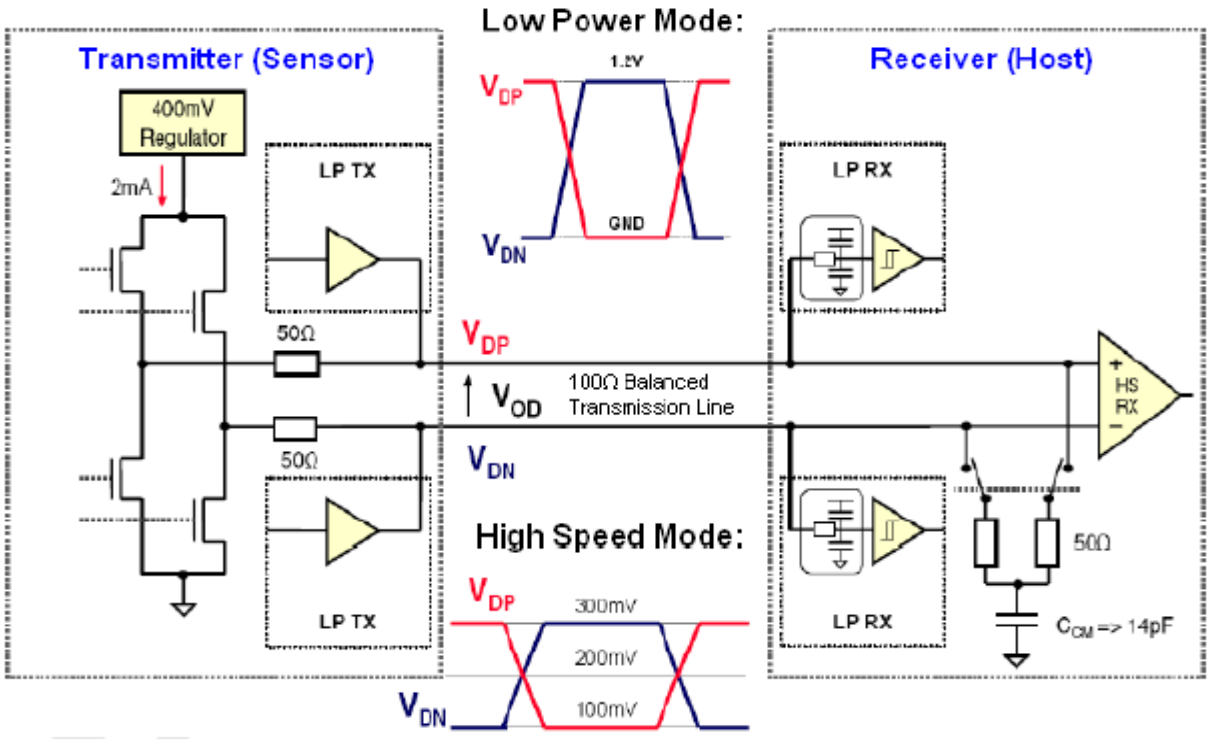


Figure 28 Driver Implementation

4.3 Low Level Protocol (LLP)

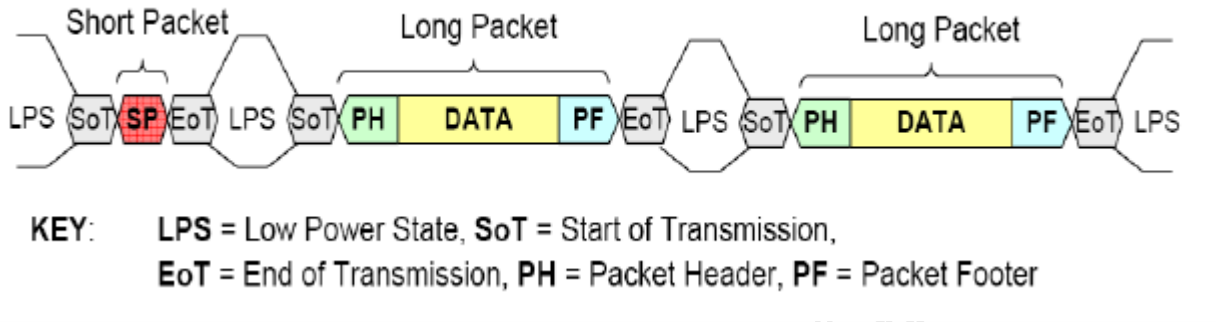


Figure 29 Low level protocol

4.4 LLP Long Packet Format

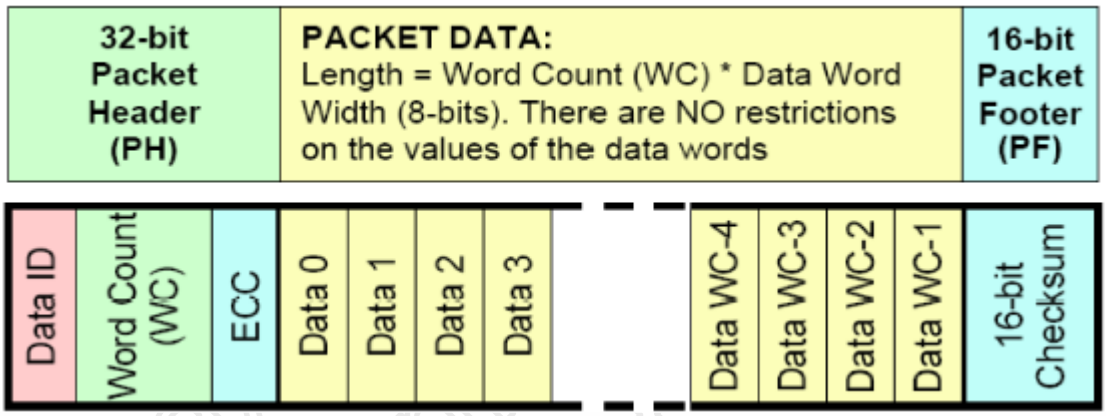


Figure 30 Long packet format

4.5 LLP Short Packet Format

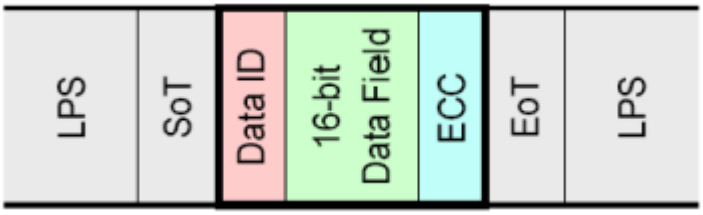
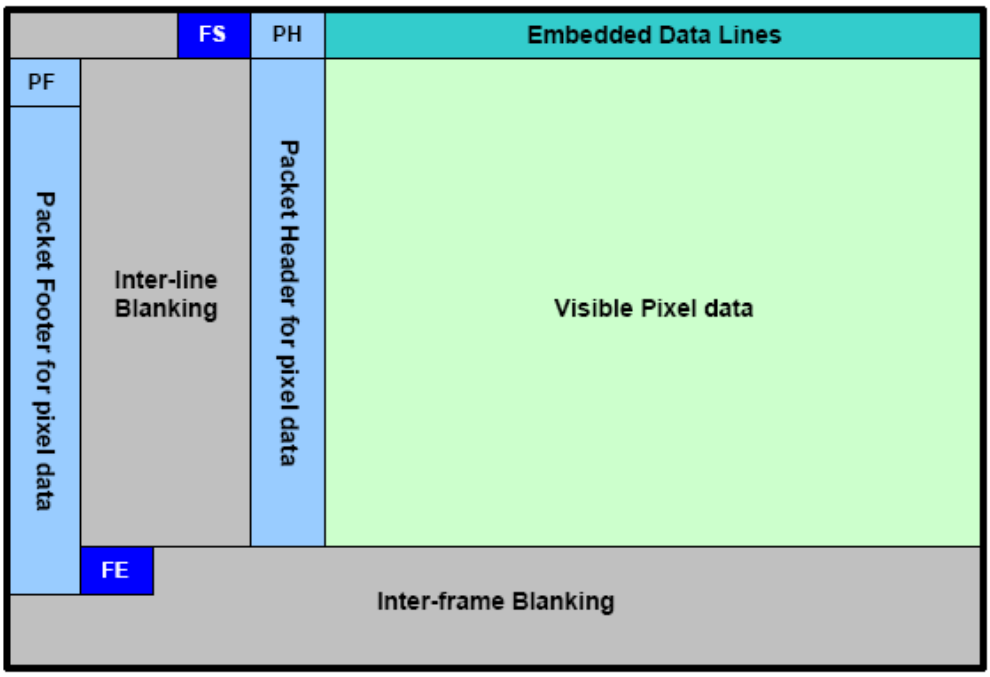


Figure 31 Short packet format

4.6 Frame Format

The frame format for the HM5065 is shown in **Figure** 32.



Key:
FS – Frame Start packet
FE – Frame End packet
PH – Packet Header of Embedded Data Lines
PF – Packet Footer of Embedded Data Lines (checksum)

Figure 32 Frame format

4.7 Embedded Data Lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values with a frame of CSI data.

The number of embedded data lines at the start and end of the frame is specified as part of the frame format description. HM5065 has no embedded data lines.

4.8 Visible Pixel Data

The visible pixels contain valid image data. The correct integration time and analog gain for the visible pixels is specified in the embedded lines at the start of the frame. The number of visible pixels can be varied.

5 Host communication – Serial Control Interface

The interface used on the HM5065 is a subset of the serial interface standard. Higher level protocol adaptations have been made to allow for greater addressing flexibility. This extended interface is known as the V2W interface.

5.1 Protocol

A message contains two or more bytes of data preceded by a START (S) condition and followed by either a STOP (P) or a repeated START (Sr) condition followed by another message.

STOP and START conditions can only be generated by a V2W master.

After every byte transferred the receiving device must output an acknowledge bit which tells the transmitter if the data byte has been successfully received or not.

The first byte of the message is called the device address byte and contains the 7-bit address of the V2W slave to be addressed plus a read/write bit which defines the direction of the data flow between the master and the slave.

The meaning of the data bytes that follow device address changes depending whether the master is writing to or reading from the slave.

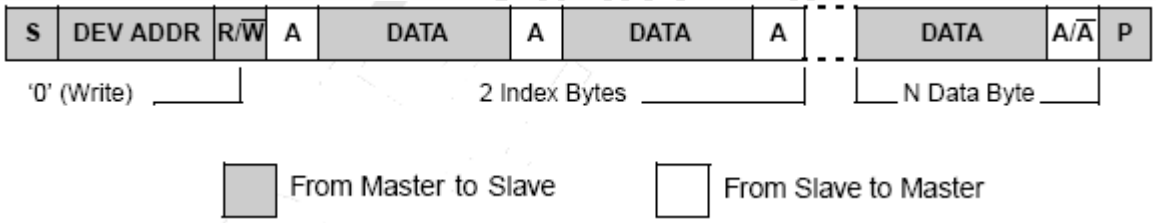


Figure 33 Write message

For the master writing to the slave the device address byte is followed by 2 bytes which specify the 16-bit internal location (index) for the data write. The next byte of data contains the value to be written to that register index. If multiple data bytes are written then the internal register index is automatically incremented after each byte of data transferred. The master can send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a STOP condition or sends a repeated START (Sr).

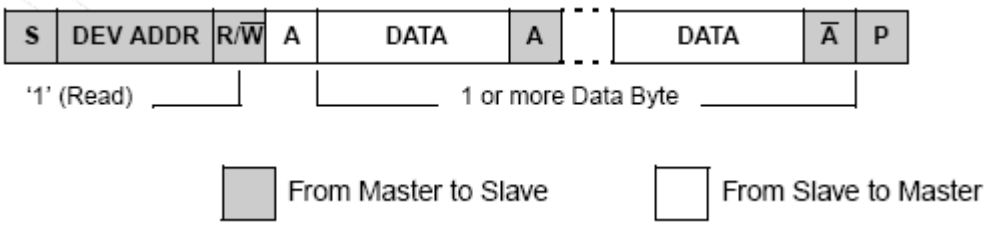


Figure 34 Read message

For the master reading from the slave the device address is followed by the contents of last register index that the previous read or write message accessed. If multiple data bytes are read then the internal register index is automatically incremented after each byte of data read. A read message is terminated by the bus master generating a negative acknowledge after reading a final byte of data.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

5.2 Detailed Overview of the Message Format

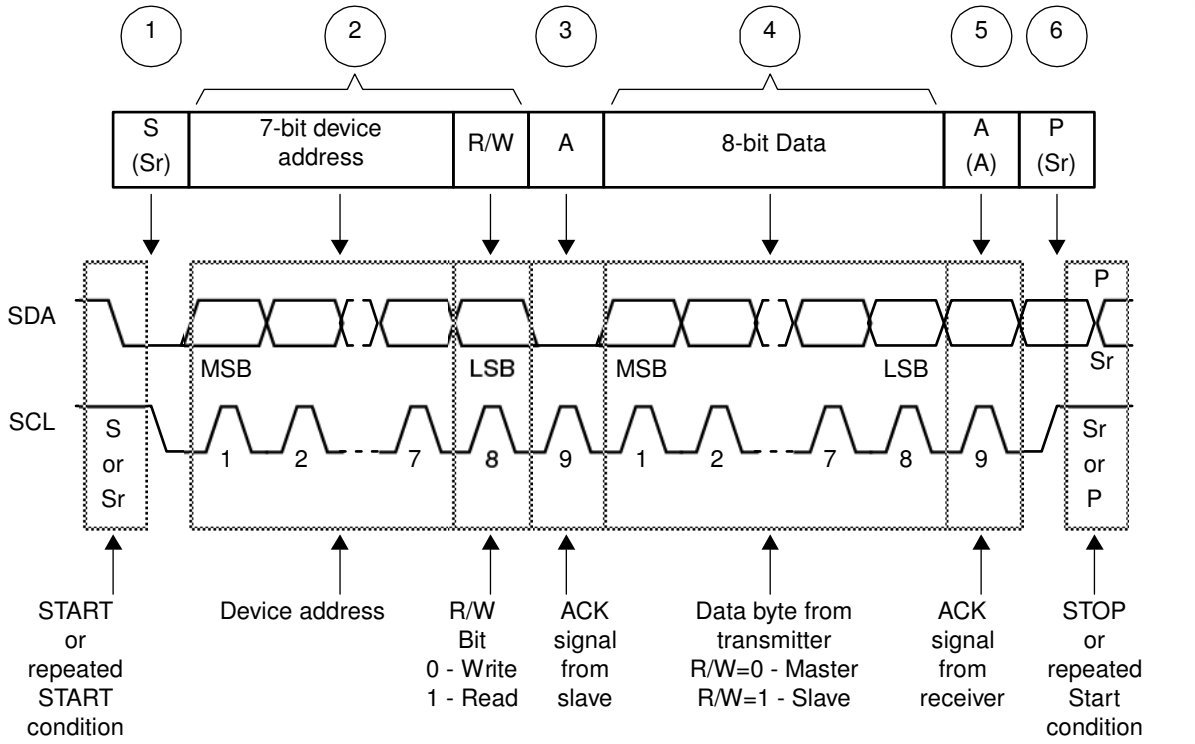


Figure 35 Detailed overview of message format

The V2W generic message format consists of the following sequence:

1. Master generates a START condition to signal the start of new message.
2. Master outputs, MS bit first, a 7-bit device address of the slave the master is trying to communicate with followed by a R/W bit.
   a) R/W = 0 then the master (transmitter) is writing to the slave (receiver).
   b) R/W = 1 the master (receiver) is reading from the slave (transmitter).
3. The addressed slave acknowledges the device address.
4. Data transmitted on the bus
   a) When a write is performed then master outputs 8-bits of data on SDA (MS Bit first).
   b) When a read is performed then slave outputs 8-bits of data on SDA (MS Bit First).
5. Data receive acknowledge
   a) When a write is performed slave acknowledges data.
   b) When a read is performed master acknowledges data.
6. Repeat 4 and 5 until all the required data has been written or read.
   Minimum number of data bytes for a read =1 (Shortest Message length is 2-bytes).
   The master outputs a negative acknowledge for the data when reading the last byte of data. This causes the slave to stop the output of data and allows the master to generate a STOP condition.
7. Master generates a STOP condition or a repeated START.

Sensor address	0	0	1	0	0	0	0	R/W
Sensor write address 20_H	0	0	1	0	0	0	0	0
Sensor read address 21_H	0	0	1	0	0	0	0	1

Figure 36 Device addresses

5.3 Data Valid

The data on SDA is stable during the high period of SCL. The state of SDA is changed during the low phase of SCL. The only exceptions to this are the start (S) and stop (P) conditions as defined below. (See *Section 8.6: serial interface slave interface* for full timing specification).

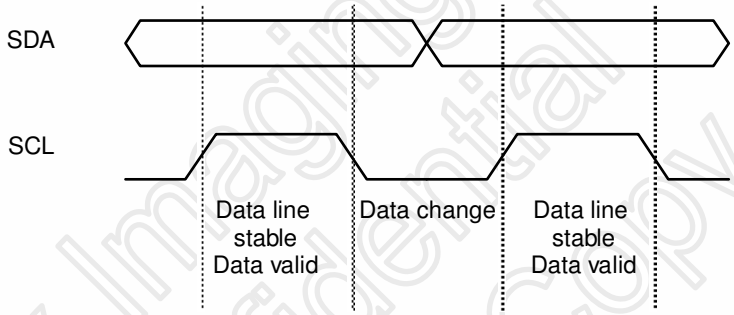


Figure 37 SDA data valid

5.4 Start and Stop Conditions

A START (S) condition defines the start of a V2W message. It consists of a high to low transition on SDA while SCL is high. A STOP (P) condition defines the end of a V2W message. It consists of a low to high transition on SDA while SCL is high.

After STOP condition the bus is considered free for use by other devices. If a repeated START (Sr) is used instead of a stop then the bus stays busy. A START (S) and a repeated START (Sr) are considered to be functionally equivalent.

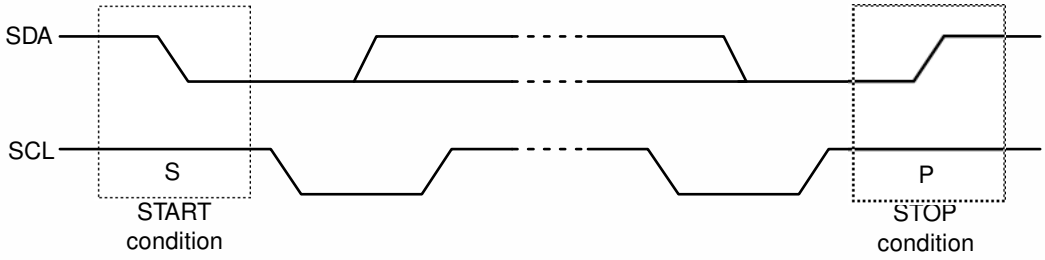


Figure 38 START and STOP conditions

5.5 Acknowledge

After every byte is transferred, the receiver must output an acknowledge bit. To acknowledge the data byte, the receiver pulls SDA during the 9th SCL clock cycle generated by the master. If the SDA is not pulled low, then the transmitter stops the output of data and releases control of the bus back to the master so that it can either generate a STOP or a repeated START condition.

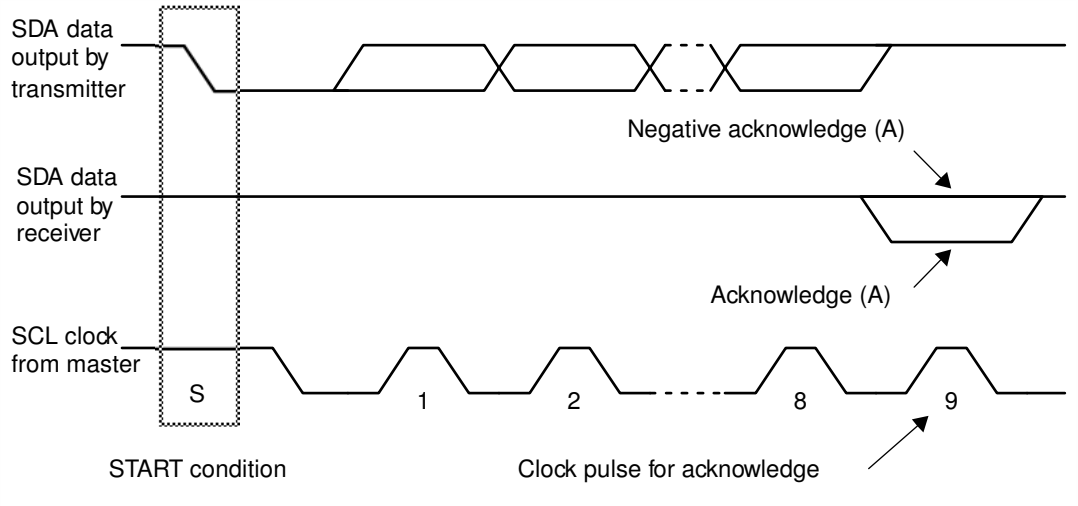


Figure 39 Data acknowledge

5.6 Index Space

Communication using the serial bus center around a number of registers internal to the either the sensor or the co-processor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The internal register locations are organized in a 64k by 8-bit wide space. This space includes “real” registers, SRAM, ROM and/or micro controller values.

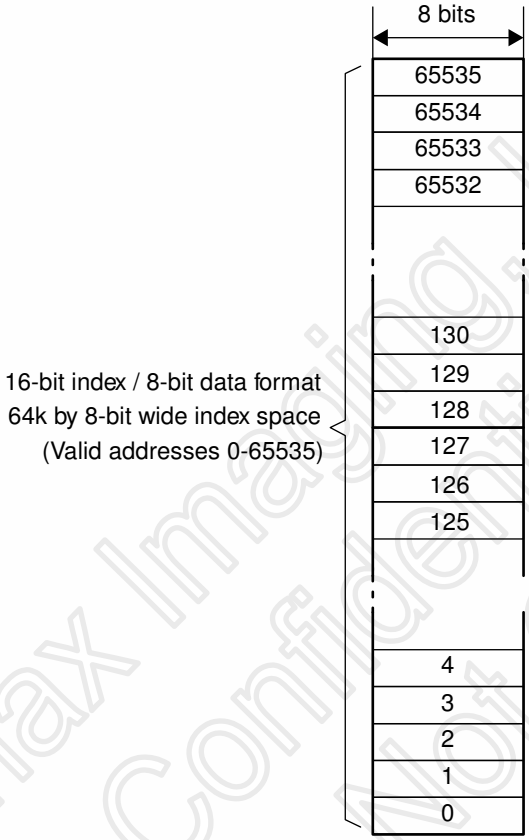


Figure 40 Internal register index space

5.7 Types of Message

This section gives guidelines on the basic operations to read data from and write data to HM5065.

The serial interface supports variable length messages. A message contains no data bytes or one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available is detailed below.

- Single location, single byte data read or write.
- Write no data byte. Only sets the index for a subsequent read message.
- Multiple locations, multiple data read or write for fast information transfers.

Any messages formats other than those specified in the following section is considered invalid.

5.7.1 Random Location, Single Data Write

For the master writing to the slave the R/W bit is set to zero. The register index value written is preserved and is used by a subsequent read. The write message is terminated with a stop condition from the master.

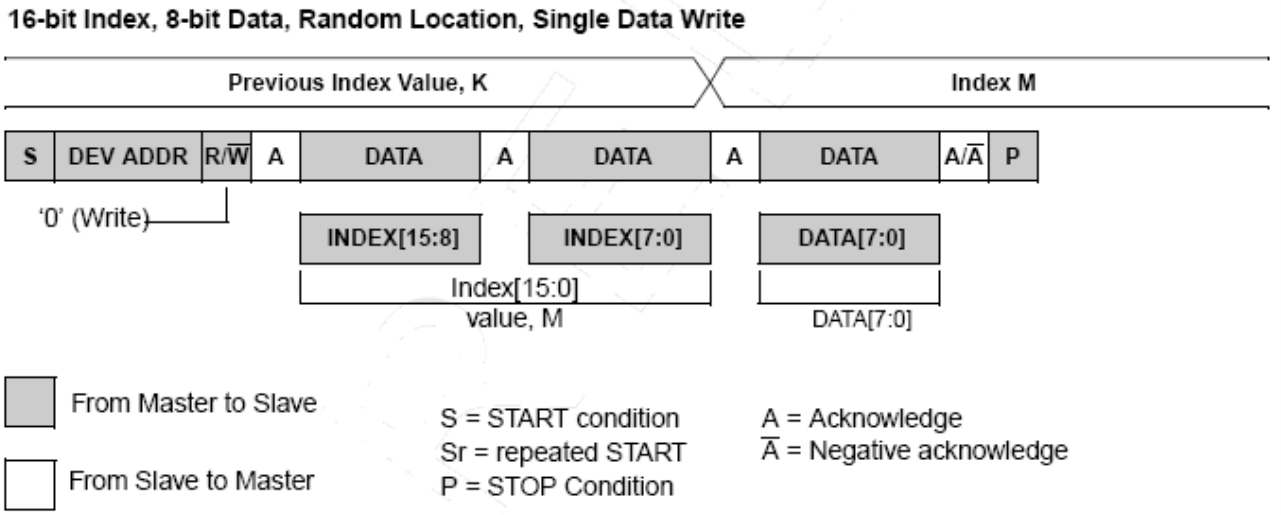


Figure 41 Random location, single write

5.7.2 Current Location, Single Data Read

For the master reading from the slave the R/W bit is set to one. The register index of the data returned is that accessed by the previous read or write message.

The first data byte returned by a read message is the contents of the internal index value and NOT the index value. This was the case in older V2W implementations.

Note that the read message is terminated with a negative acknowledge (A) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the SDA line cannot rise, which is part of the stop condition.

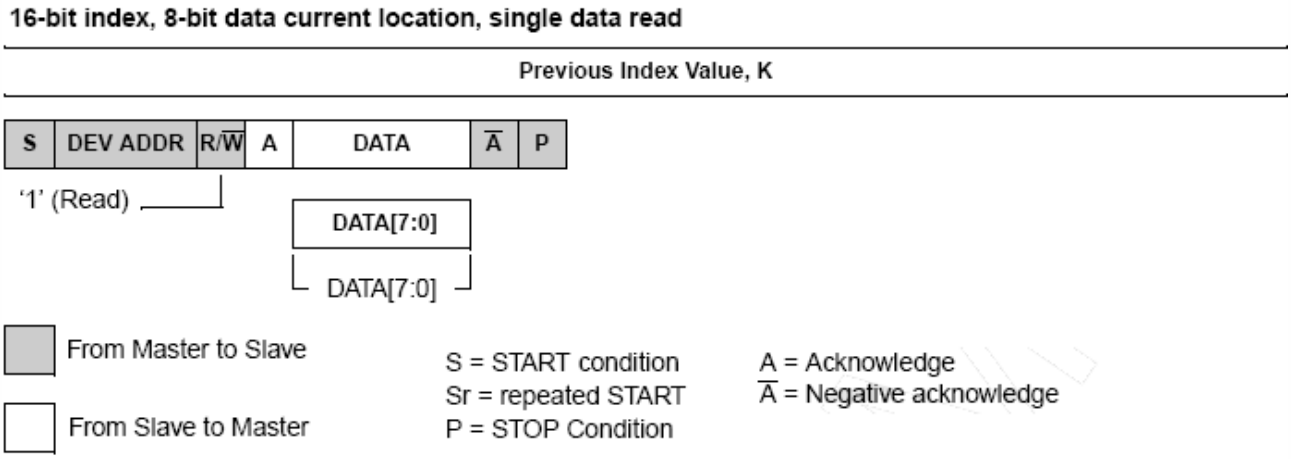


Figure 42 Current location, single read

5.7.3 Random Location, Single Data Read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages.

As mentioned in the previous example, the read message is terminated with a negative acknowledge (A) from the master.

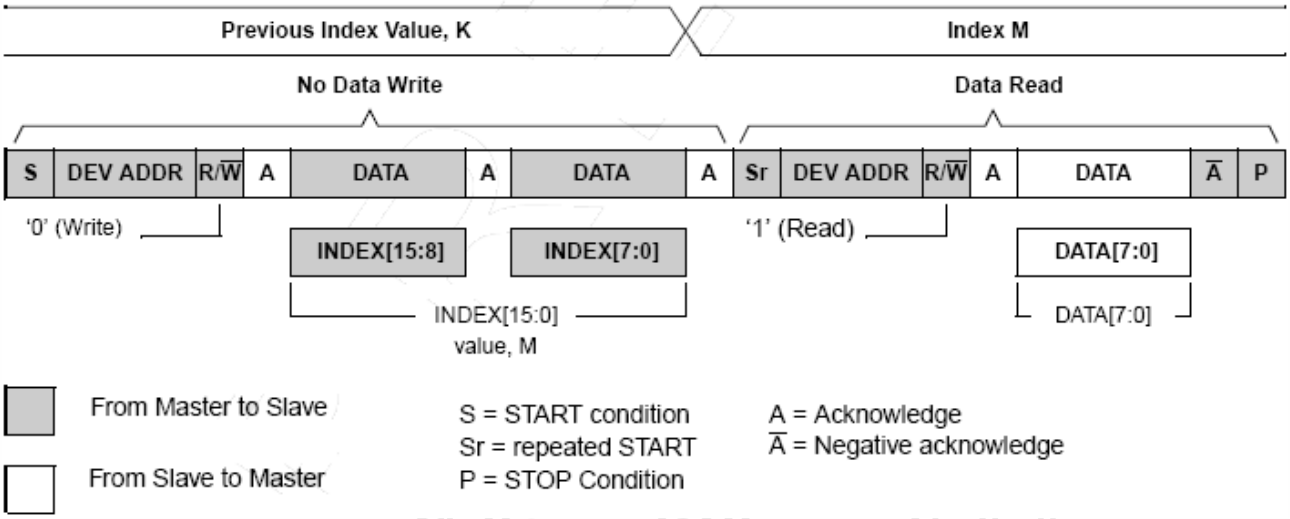


Figure 43 16-bit index, 8-bit data random index, single data read

5.7.4 Multiple Location Write

For messages with more than 1 data byte the internal register index is automatically incremented for each byte of data output, making it possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

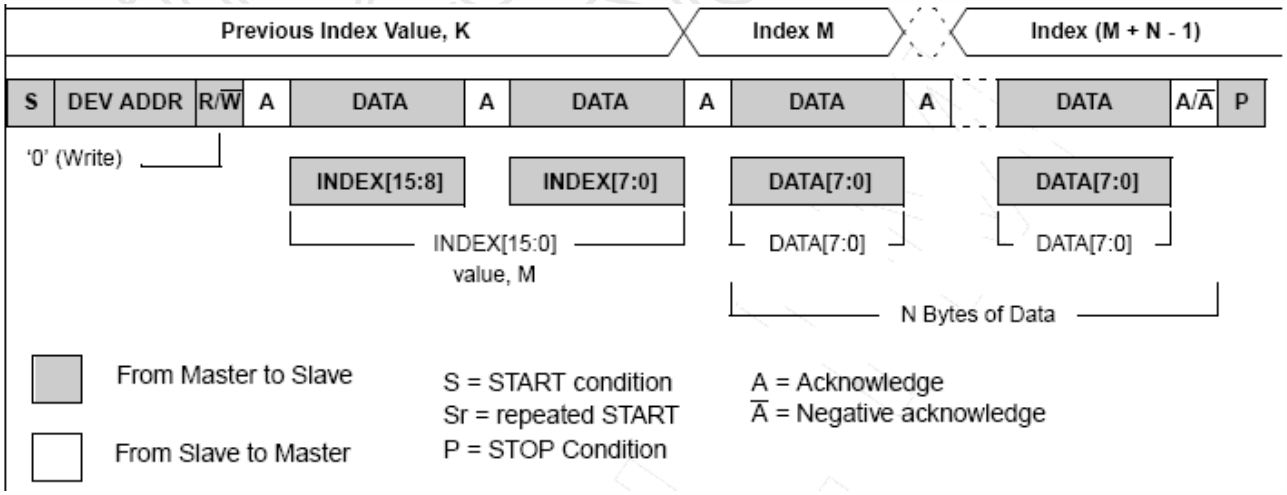


Figure 44 16-bit index, 8-bit data multiple location write

5.7.5 Multiple Location Read Starting from the Current Location

In the same manner to multiple location writes, multiple locations can be read with a single read message.

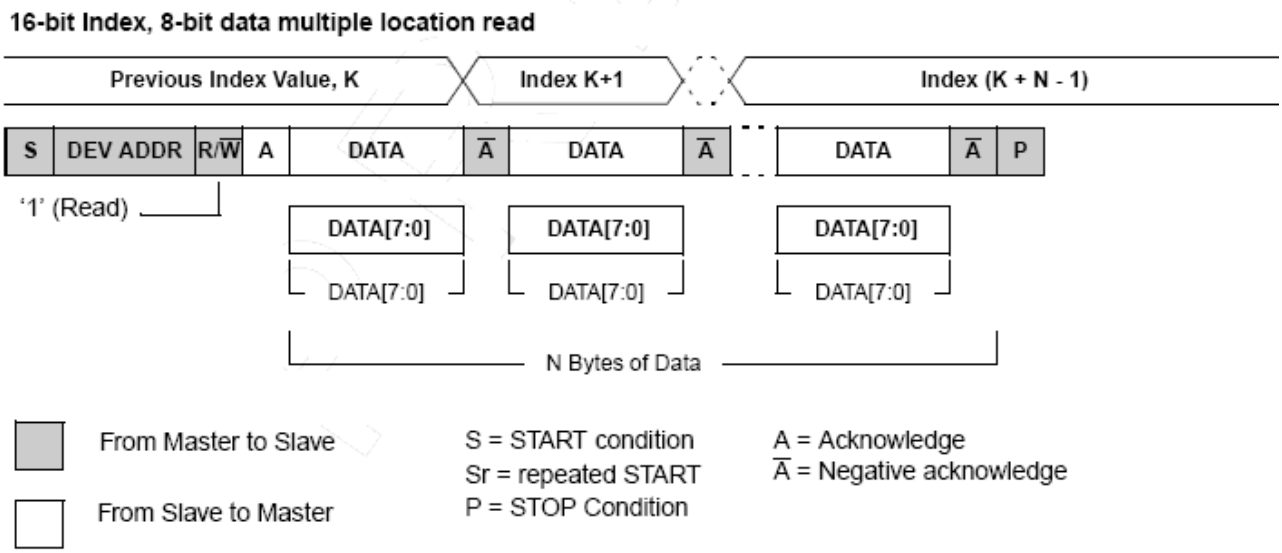


Figure 45 Multiple location read

5.7.6 Multiple Location Read Starting from Random Location

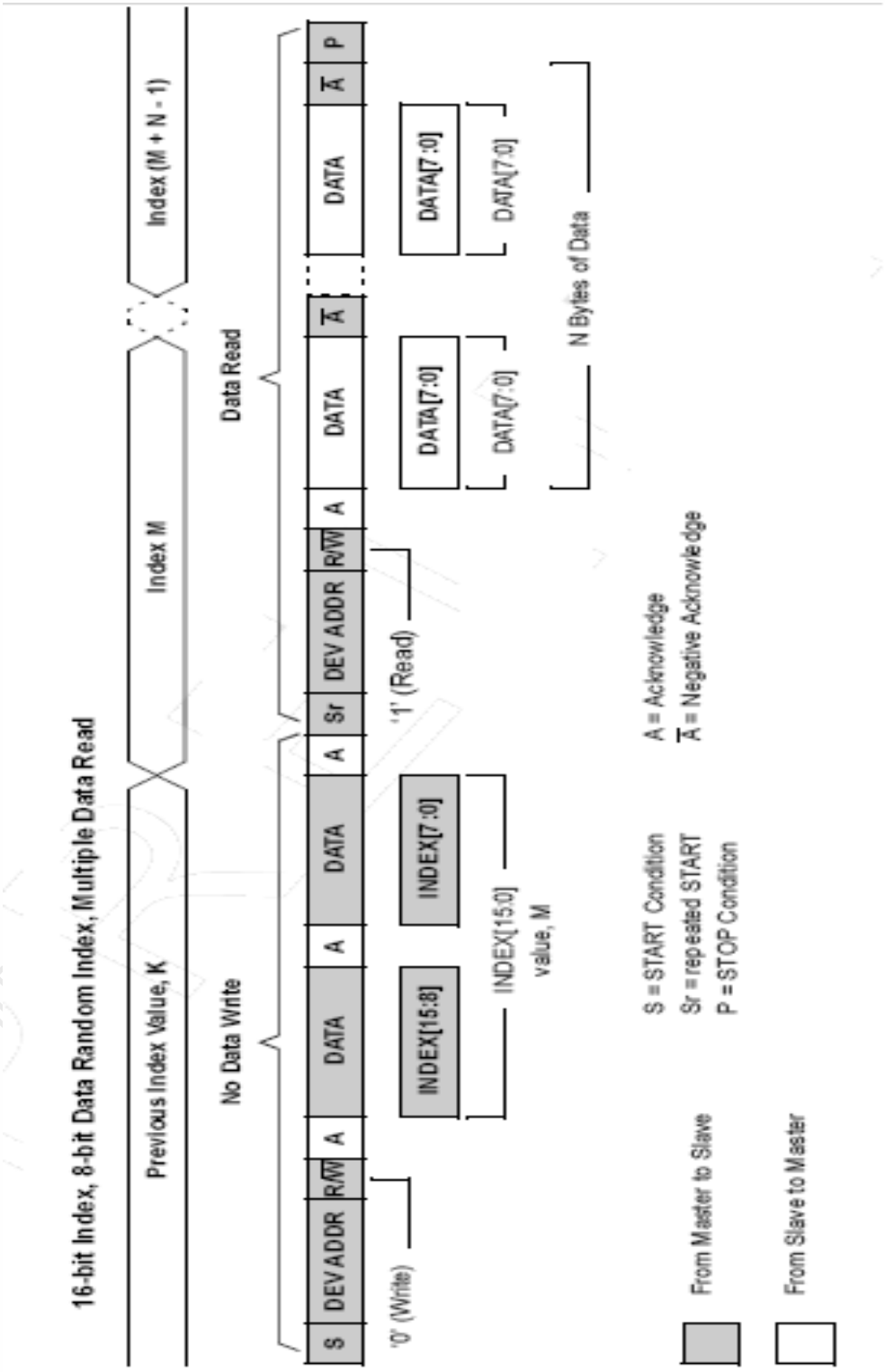


Figure 46 Multiple location read starting from a random location

6 Programming model and register description

6.1 Programming Model

The HM5065 addressable register/memory space is configured as shown in **Figure 47 System/host view of HM5065**. It consists of four principal areas, each of which provides a different function:

1. **User Interface:** this area starting from address zero provides the user interface. Register reads and writes to this block are passed through the internal microcontroller and processed. All operational control of the device by the host should be performed through these user interface locations. Many of these registers are detailed in .

Note: *Registers not listed in this datasheet should be considered as reserved or read-only and should NOT be written to, as this may cause unpredictable results.*

- **Hardware registers**: provides direct access to hardware registers associated with each functional block of the device. In normal operation, these registers will be accessed under the control of the microcontroller and hence they should never be accessed by the host system. However, they may be directly accessed by the host for debug and test purposes.
- **XDATA RAM**: provides temporary variable storage for the on-board microcontroller.
- **Patch RAM**: provides memory space to download firmware patches and modify device operation. This provides a software update mechanism without the need for a new program ROM.

Figure 47 System/host view of HM5065 memory

6.2 Register Description

Register contents represent different data types as described in **Table 15: Register naming prefix**.

Type	Length	Description
bXXXX	8-bit	1-byte unsigned data
uwXXXX	16-bit	2-byte unsigned data
udwXXXX	32-bit	4-byte unsigned data
fpXXXX	16-bit	Floating point (ST FLOAT900)
fXXXX	1-bit	Flag (TRUE/FALSE)
iXXXX	8-bit	Sign short

Table 15: Register naming prefix

Note: *The HM5065 serial interface write address is 0x3E.*

Function type	Name
RO	Read only register
RW	Read and Write register
RWS	Static Read and Write register. Value should only be updated during software standby.

Table 16: Valid register function types

Registers not listed in this datasheet should be considered as reserved or read-only should NOT be written to, as this may cause unpredictable results. All register are accessible after initialized.

All serial interface locations contain an 8-bit byte. However, certain parameters require 16 bits or more to represent them and are therefore stored in more than 1 location.

Note: *For all parameters more than 8 bits, the MSB register must be written before the LSB register.*

The data stored in each location can be interpreted in different ways as shown below. Register contents represent different data types as described in **Table 17: Data types** .

Data type	Name	Range	Description
UI8	8-bit unsigned integer	0 to 255	
SI8	8-bit signed integer	-128 to 127	Two's complement notation
UI16	16-bit unsigned integer	0 to 65535	
SI16	16-bit signed integer	-32768 to 32767	Two's complement notation
C8	8-bit coded		This indicates that the value is decoded to select one of several functions or modes.
FP16	16-bit floating point	-858154598 to 858154598	Float900 is used in ST coprocessors to represent floating point numbers in 2 bytes of data. It conforms to the following structure: Bit[15] = Sign bit (1 represents negative) Bit[14:9] = 6 bits of exponent, biased at decimal 31 Bit[8:0] = 9 bits of mantissa

Table 17: Data types

6.3 Register Description

6.3.1 Device Parameters

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	Hi	uwDeviceID	UI16	0x03 0x9E	RO	16-bit sensor model number, 0x039E = 926
0x0001	Lo					
0x0002		bFirmwareVsn	UI8	0x20	RO	Firmware version. For HM5065 Cut 2.0 firmware version is 0x20
0x0003		bPatchVsn	UI8	0x00	RO	Patch version
0x0004~ 0x0008		-	-	-	-	Reserved.
0x0009		EXCLOCKLUT	C8	0x15	RWS	Look-Up Table (LUT) for external clock: 0x10: 12.0 Mhz 0x11: 13.0 Mhz 0x12: 13.5 Mhz 0x13: 14.4 Mhz 0x14: 18.0 Mhz 0x15: 19.2 Mhz 0x16: 24.0 Mhz 0x17: 26.0 Mhz 0x18: 27.0 Mhz

0x000a		bInt_Event_Flag	C8	0x00	RW	Status of interrupt events. Respective bit is set to '1' if the corresponding event is triggered. Write '0' to clear the bit. Bit[0]: Operating mode Bit[1]: Camera mode Bit[2]: JPEG status Bit[3]: Number of frames output Bit[4]: AF locked Refer *Section 3.7: Microprocessor functions - Interrupt events* for more detail.
0x000b		bInt_Event_Enable	C8	0x00	RW	Specify which events should generate an external interrupt (NIRQ pin): Bit[0]: Operating mode Bit[1]: Camera mode Bit[2]: JPEG status Bit[3]: Number of frames output Bit[4]: AF locked 0: No external interrupt 1: Generate external interrupt if event is triggered. Refer *Section 3.7: Microprocessor functions - Interrupt events* for more detail.
0x000c		bNextAfterStreamed	C8	0x00	RW	Specify subsequent sensor operation after number of frames streamed (defined by register **bRequiredStreamLength**): 0x00: Stop streaming 0x01: Switch to Pipebank 0

Table 18: Device parameters - [0x0000 - 0x000c]

6.3.2 ModeManager

Index	Byte	Register name	Data type	Default	Type	Comment
0x0010		bUserCommand	C8	0x00	RW	Sensor operating mode: 0x00: CMD_STOP 0x01: CMD_RUN 0x02: CMD_POWEROFF
0x0011		bState	C8	0x10	RO	Status: 0x10: STATE_RAW (upon power up) 0x20: STATE_IDLE 0x30: STATE_RUNNING
0x0012		bActivePipeSetupBank	C8	0x00	RW	Select current active pipebank: 0x00: Pipebank 0 0x01: Pipebank 1

0x0014		bNumberOfFrames Streamed	UI8	0x00	RO	Counts the number of frames streamed.
0x0015		bRequiredStreamLength	UI8	0x00	RW	Define number of frames to be streamed: 0x00: Continuous streaming
0x0016		fCSIEnable	C8	0x00	RWS	Enable/Disable CSI output: 0x00: Disable 0x01: CSI2 single lane 0x02: CSI2 dual lane

Table 19: ModeManager - [0x0010 - 0x0016]

6.3.3 ZoomControl

Index	Byte	Register name	Data type	Default	Type	Comment
0x0020		bZoomControl	C8	0x00	RW	Zoom control: 0x00: ZoomStop 0x01: ZoomContinuous_In 0x02: ZoomContinuous_Out 0x03: ZoomStep_In 0x04: ZoomStep_Out
0x0021	HI	uwZoomStepSize	UI16	0x00 0x01	RW	Zoom step size: 0x01: 1 step 5%
0x0022	LO					
0x0023~ 0x002e		-	-	-	-	Reserved.
0x002f		bMinScalerFactor	UI8	0x14	RW	This sets the minimum scaler factor during zooming. Default: 20
0x0030		bMaxDeratingRatio	UI8	0x14	RW	This sets the maximum derating ratio. Default: 0x14 lower nibble for P0 higher nibble for P1

Table 20: ZoomControls - [0x0020 - 0x0030]

6.3.4 PipeSetupBank0 (preview bank)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		bSensorMode	C8	0x00	RWS	Sensor mode: 0x00: Fullsize 0x01: Analogbinning 2x2 0x02: Analogbinning 4x4 0x03: Subsampling 2x2 0x04: Subsampling 4x4
0x0041		bImageSize	C8	0x00	RW	Pre-defined output image size: 0x00: ImageSize_5MP 0x01: ImageSize_UXGA 0x02: ImageSize_SXGA 0x03: ImageSize_SVGA 0x04: ImageSize_VGA 0x05: ImageSize_CIF 0x06: ImageSize_QVGA 0x07: ImageSize_QCIF 0x08: ImageSize_QQVGA 0x09: ImageSize_QQCIF 0x0A: ImageSize_Manual
0x0042	HI	uwManualHSize	UI16	0x00 0x00	RW	Output image width. Need to be set when the "ImageSize_Manual" in register **bImageSize** is selected.
0x0043	LO					
0x0044	HI	uwManualVSize	UI16	0x00 0x00	RW	Output image height. Need to be set when the "ImageSize_Manual" in register **bImageSize** is selected.
0x0045	LO					
0x0046		bDataFormat	C8	0x00	RW	Output data format: 0x00: DataFormat_YCbCr_Jfif 0x01: DataFormat_YCbCr_Rec601 0x02: DataFormat_YCbCr_Custom 0x03: DataFormat_RGB_565 0x04: DataFormat_RGB_565_Custom 0x05: DataFormat_RGB_444 0x06: DataFormat_RGB_555 0x07: DataFormat_RAW10ITU10 0x08: DataFormat_RAW10ITU8 0x09: DataFormat_JPEG
0x0047~ 0x0048		-	-	-	-	Reserved.
0x0049		bGammaGain	UI8	0x14	RW	Gamma gain for R, B, G channels Range: 0~31 Default: 20
0x004a		bGammaInterpolation	UI8	0x00	RW	Gamma interpolation Range: 0~16 (classic)

0x004b		-	-	-	-	Reserved.
0x004c		bPeakingGain	UI8	0x0f	RW	Peaking Gain Range: 0~63 Default: 15
0x004d		bJpegSqueezeSettings	C8	0x00	RW	Compression mode for JPEG output: 0x00: User squeeze mode 0x01: Auto squeeze mode
0x004e	HI	wJpegTargetFileSize	UI16	0x00 0x00	RW	Targeted file size (in terms of Kbytes) when using auto squeeze mode.
0x004f	LO					
0x0050		bJpegImageQuality	C8	0x00	RW	When user squeeze mode is selected, this register determines the quality of the JPEG output image: 0x00: High quality 0x01: Medium quality 0x02: Low quality The amount of compression (squeezing) is determined by value set in registers **bHiSqueezeValue**, **bMedSqueezeValue**, and **bLowSqueezeValue** in

Table 21: PipeSetupBank0 - [0x0040 - 0x0050]

6.3.5 PipeSetupBank1 (capture bank)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0060		bSensorMode	C8	0x00	RWS	Sensor mode: 0x00: Fullsize 0x01: Analogbinning 2x2 0x02: Analogbinning 4x4 0x03: Subsampling 2x2 0x04: Subsampling 4x4
0x0061		bImageSize	C8	0x00	RW	Pre-defined output image size: 0x00: ImageSize_5MP 0x01: ImageSize_UXGA 0x02: ImageSize_SXGA 0x03: ImageSize_SVGA 0x04: ImageSize_VGA 0x05: ImageSize_CIF 0x06: ImageSize_QVGA 0x07: ImageSize_QCIF 0x08: ImageSize_QQVGA 0x09: ImageSize_QQCIF 0x0A: ImageSize_Manual
0x0062	HI	uwManualHSize	UI16	0x00	RW	Output image width.

0x0063	LO			0x00		Need to be set when the “ImageSize_Manual” in register **bImageSize** is selected.
0x0064	HI	uwManualVSize	UI16	0x00 0x00	RW	Output image height. Need to be set when the “ImageSize_Manual” in register **bImageSize** is selected.
0x0065	LO					
0x0066		bDataFormat	C8	0x00	RW	Output data format: 0x00: DataFormat_YCbCr_Jfif 0x01: DataFormat_YCbCr_Rec601 0x02: DataFormat_YCbCr_Custom 0x03: DataFormat_RGB_565 0x04: DataFormat_RGB_565_Custom 0x05: DataFormat_RGB_444 0x06: DataFormat_RGB_555 0x07: DataFormat_RAW10ITU10 0x08: DataFormat_RAW10ITU8 0x09: DataFormat_JPEG
0x0067~ 0x0068		-	-	-	-	Reserved.
0x0069		bGammaGain	UI8	0x14	RW	Gamma gain for R, B, G channels Range: 0~31 Default: 20
0x006a		bGammaInterpolation	UI8	0x00	RW	Gamma interpolation Range: 0~16 (classic)
0x006b		-	-	-	-	Reserved.
0x006c		bPeakingGain	UI8	0x0f	RW	Peaking Gain Range: 0~63 Default: 15
0x006d		bJpegSqueezeSettings	C8	0x00	RW	Compression mode for JPEG output: 0x00: User squeeze mode 0x01: Auto squeeze mode
0x006e	HI	wJpegTargetFileSize	UI16	0x00 0x00	RW	Targeted file size (in terms of Kbytes) when using auto squeeze mode.
0x006f	LO					
0x0070		bJpegImageQuality	C8	0x00	RW	When user squeeze mode is selected, this register determines the quality of the JPEG output image: 0x00: High quality 0x01: Medium quality 0x02: Low quality

Table 22: PipeSetupBank1 - [0x0060 - 0x0070]

6.3.6 PipeSetupCommon

Index	Byte	Register name	Data type	Default	Type	Comment
0x0080		bContrast	UI8	0x73	RW	Contrast Range: 0~200 Default: 115
0x0081		bColorSaturation	UI8	0x76	RW	Color saturation Range: 0~200 Default: 118
0x0082		bBrightness	UI8	0x64	RW	Brightness Range: 0~200 Default: 100
0x0083		fHorizontalMirror	C8	0x01	RW	Horizontal mirror : 0x00: Disable 0x01: Enable
0x0084		fVerticalFlip	C8	0x01	RW	Vertical flip : 0x00: Disable 0x01: Enable
0x0085		bYCrCbOrder	C8	0x02	RW	Y, Cr, and Cb output order: 0x00: Cb-Y-Cr-Y 0x01: Cr-Y-Cb-Y 0x02: Y-Cb-Y-Cr 0x03: Y-Cr-Y-Cb

Table 23: PipeSetupCommon - [0x0080 - 0x0085]

6.3.7 ClockChainParameterFPInputs

Index	Byte	Register name	Data type	Default	Type	Comment
0x00b0	HI	fpExternalClock	FP16	0x46 0x66	RWS	External clock frequency used in Mhz . Refer to register **EXCLOCKLUT** for pre-defined options. This register is automatically filled if one of the pre-defined options is selected. The register may be overwritten if the external clock frequency does not listed in the pre-defined options. Range: 6.0~27.0 Default: 19.1875
0x00b1	LO	FrequencyMhz				
0x00b2	HI	fpTargetPllOutput	FP16	0x50	RWS	Specify the target PLL output

0x00b3	LO	FrequencyMhz		0xC9		frequency in Mhz . Value must be set before the sensor start streaming to be in effect. Range: 450.0~1000.0 Default: 713.0

Table 24: ClockChainParameterFPInputs - [0x00b0 - 0x00b3]

6.3.8 StaticFrameRateControl

Index	Byte	Register name	Data type	Default	Type	Comment
0x00c8	HI	uwDesiredFrameRate_ Num	UI16	0x00 0x0f	RW	Numerator of desired framerate Default: 15
0x00c9	LO					
0x00ca		bDesiredFrameRate_Den	UI8	0x01	RW	Denominator of desired framerate

Table 25: StaticFrameRateControl - [0x00c8 - 0x00ca]

6.3.9 StaticFrameRateStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x00d8	HI	fpRequested FrameRate_Hz	FP16	0x00 0x00	RO	Requested framerate in Hz
0x00d9	LO					
0x00da	HI	fpMaxFrameRate_Hz	FP16	0x00 0x00	RO	Maximum allowed framerate in Hz
0x00db	LO					
0x00dc	HI	fpMinFrameRate_Hz	FP16	0x00 0x00	RO	Minimum allowed framerate in Hz
0x00dd	LO					

Table 26: StaticFrameRateStatus - [0x00d8 - 0x00dd]

6.3.10 ExposureControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0128		bMode	C8	0x00	RW	Exposure control mode: 0x00: AUTOMATIC_MODE 0x01: COMPILED_MANUAL_MODE 0x02: DIRECT_MANUAL_MODE

0x0129		bMetering	C8	0x00	RW	Metering mode : 0x00: ExposureMetering_flat 0x01: ExposureMetering_backlit 0x02: ExposureMetering_centerd
0x012a		bManualExposureTime_s_num	UI8	0x01	RW	Numerator of manual exposure time in seconds.
0x012b		bManualExposureTime_s_den	UI8	0x1e	RW	Denominator of manual exposure time in seconds. Default: 30
0x012c	HI	fpManualDesiredExposureTime_us	FP16	0x59 0xaa	RW	Desired manual exposure time in microseconds. Default: 15008.0
0x012d	LO					
0x012e	HI	fpColdStartDesiredTime_us	FP16	0x59 0xaa	RWS	Desired cold start time in microseconds. Default: 15008.0
0x012f	LO					
0x0130		iExposureCompensation	SI8	0xfd	RW	Exposure compensation Range: -7 to +7 Default: -3
0x0131		-	-	-	-	Reserved.
0x0132	HI	uwDirectModeCoarseIntegration_lines	UI16	0x00 0x00	RW	Direct mode coarse integration lines
0x0133	LO					
0x0134	HI	uwDirectModeFineIntegration_pixels	UI16	0x00 0x00	RW	Direct mode fine integration pixels
0x0135	LO					
0x0136	HI	uwDirectModeCodedAnalogGain	UI16	0x00 0x00	RW	Direct mode coded analog gain
0x0137	LO					
0x0138	HI	fpDirectModeDigitalGain	FP16	0x00 0x00	RW	Direct mode digital gain
0x0139	LO					
0x013a~ 0x0141		-	-	-	-	Reserved.
0x0142		fFreezeAutoExposure	C8	0x00	RW	Freeze auto exposure: 0x00: FALSE 0x01: TRUE
0x0143	HI	fpUserMaximumIntegrationTime_us	FP16	0x64 0x7f	RW	User defined maximum integration time in microseconds. Default: 654336.0
0x0144	LO					

0x0145~ 0x0147		-	-	-	-	Reserved.
0x0148		bAntiFlickerMode	C8	0x01	RW	Anti-flicker mode: 0x00: Inhibit 0x01: Enable

Table 27: ExposureControls - [0x0128 - 0x0148]

6.3.11 ExposureAlgorithmControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x015c	HI	fpDigitalGainFloor	FP16	0x3e 0x00	RW	Digital gain floor
0x015d	LO					
0x015e	HI	fpDigitalGainCeiling	FP16	0x41 0x00	RW	Digital gain ceiling Default: 3.0
0x015f	LO					

Table 28: ExposureAlgorithmControls - [0x015c - 0x015f]

6.3.12 ExposureStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x017c	HI	uwCoarseIntegration Pending_lines	UI16	0x00 0x00	RO	Pending coarse integration (in terms of number of lines) for next frame.
0x017d	LO					
0x017e	HI	uwFineIntegration Pending_pixels	UI16	0x00 0x00	RO	Pending fine integration (in terms of number of pixels) for next frame.
0x017f	LO					
0x0180	HI	fpAnalogGainPending	FP16	0x00 0x00	RO	Pending analog gain to be applied to next frame.
0x0181	LO					
0x0182	HI	fpDigitalGainPending	FP16	0x00 0x00	RO	Pending digital gain to be applied to next frame.
0x0183	LO					
0x0184	HI	fpDesiredExposure Time_us	FP16	0x00 0x00	RO	Desired exposure setting in microseconds.
0x0185	LO					
0x0186	HI	fpCompiledExposure Time_us	FP16	0x00 0x00	RO	Desired compiled exposure in microseconds.
0x0187	LO					
0x0189	HI	uwUserMaximum	UI16	0x00	RO	User defined maximum integration

0x018a	LO	IntegrationLines		0x00		lines.
0x018b	HI	fpTotalIntegration TimePending_us	FP16	0x00 0x00	RO	Pending total integration time in microseconds for next frame.
0x018c	LO					
0x018d	HI	uwCodedAnalogGain Pending	UI16	0x00 0x00	RO	Pending analog gain (coded) to be applied to next frame.
0x018e	LO					

Table 29: ExposureStatus - [0x017c - 0x018e]

6.3.13 FlickerDetect

Index	Byte	Register name	Data type	Default	Type	Comment
0x0190		fEnableDetect	C8	0x01	RW	Enable detection: 0x00: FALSE 0x01: TRUE
0x0191		fDetectionStart	C8	0x00	RW	Start detection: 0x00: FALSE 0x01: TRUE
0x0192		bMaxNumberAttempt	UI8	0x3c	RW	Max number of attempt s: 0x00: Continuously until the flicker is detected. Default: 60
0x0193	HI	uwFlickerIdentification Threshold	UI16	0x00 0x18	RW	Flicker identification threshold Default: 24
0x0194	LO					
0x0195		bWinTimes	UI8	0x14	RW	Win times If the number of either 50hz or 60hz detected larger than this value, it confirms the flicker detection correctly. Default: 20
0x0196		bFrameRateShiftNumber	UI8	0x01	RW	Frame rate shift number during detection .
0x0197		fManualFrefEnable	C8	0x00	RW	Manually set flicker frequency: 0x00: FALSE 0x01: TRUE
0x0198	HI	uwManuFref100	UI16	0x00 0x00	RW	Manual reference 100
0x0199	LO					
0x019a	HI	uwManuFref120	UI16	0x00	RW	Manual reference 120

0x019b	LO			0x00		
0x019c	HI	fpFlickerFrequency	FP16	0x4b 0x20	RW	Detected flicker frequency. Default: 100.0
0x019d	LO					

Table 30: FlickerDetect - [0x0190 - 0x019d]

6.3.14 WhiteBalanceControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x01a0		bMode	C8	0x01	RW	Mode: 0x00: OFF 0x01: AUTOMATIC 0x02: AUTO_INSTANT 0x03; MANUAL_RGB 0x04: CLOUDY_PRESET 0x05: SUNNY_PRESET 0x06: LED_PRESET 0x07: FLUORESCENT_PRESET 0x08: TUNGSTEN_PRESET 0x09: HORIZON_PRESET
0x01a1		bManualRedGain	UI8	0x00	RW	Host defined Red gain. Used when register **bMode** is set to "MANUAL_RGB".
0x01a2		bManualGreenGain	UI8	0x00	RW	Host defined Green gain. Used when register **bMode** is set to "MANUAL_RGB".
0x01a3		bManualBlueGain	UI8	0x00	RW	Host defined Blue gain. Used when register **bMode** is set to "MANUAL_RGB".
0x01a4		bMiscSettings	C8	0x00	RW	Miscellaneous Settings: Bit[2]: fFreezeIterativeWhiteBalance 0: White balancing 1: Freeze white balance algorithm
0x01a5	HI	fpHue_R_Bias	FP16	0x3e 0x00	RW	fpHue_R_Bias. Default: 1.0
0x01a6	LO					
0x01a7	HI	fpHue_B_Bias	FP16	0x3e 0x00	RW	fpHue_B_Bias. Default: 1.0
0x01a8	LO					

Table 31: WhiteBalanceControls - [0x01a0 - 0x01a8]

6.3.15 WhiteBalanceStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x01c0		bStatus	C8	0x00	RO	White balance status: 0x00: Stable 0x01: Not stable
0x01c1~ 0x01c7		-	-	-	-	Reserved.
0x01c8	HI	fpNormRedGain	FP16	0x00 0x00	RO	Normalized red gain for current frame.
0x01c9	LO					

Table 32: WhiteBalanceStatus - [0x01c0 - 0x01c9]

6.3.16 OTP_WB_PRESET

Index	Byte	Register name	Data type	Default	Type	Comment
0x01e0	HI	fp_Part_RedGain	FP16	0x00 0x00	RW	Red gain offset from OTP to compensate part-to-part variation.
0x01e1	LO					
0x01e2	HI	fp_Part_GreenGain	FP16	0x00 0x00	RW	Green gain offset from OTP to compensate part-to-part variation.
0x01e3	LO					
0x01e4	HI	fp_Part_BlueGain	FP16	0x00 0x00	RW	Blue gain offset from OTP to compensate part-to-part variation.
0x01e5	LO					

Table 33: OTP_WB_PRESET - [0x01e0 - 0x01e5]

6.3.17 ImageStability

Index	Byte	Register name	Data type	Default	Type	Comment
0x0291		fWhiteBalanceStable	C8	0x00	RO	Is white balance algorithm stable? 0x00: FALSE 0x01: TRUE
0x0292		fExposureStable	C8	0x00	RO	Is exposure algorithm stable ? 0x00: FALSE 0x01: TRUE
0x0293		-	-	-	-	Reserved.

0x0294		fStable	C8	0x00	RO	Image stable status: 0x00: FALSE 0x01: TRUE

Table 34: ImageStability - [0x0291 - 0x0294]

6.3.18 ExpSensorConstants

Index	Byte	Register name	Data type	Default	Type	Comment
0x02c0	HI	uwSensorAnalogGain Floor	UI16	0x00 0x00	RW	Sensor analogue gain floor (coded analog gain)
0x02c1	LO					
0x02c2	HI	uwSensorAnalogGain Ceiling	UI16	0x00 0xf0	RW	Sensor analogue gain ceiling (coded analog gain) Default: 240
0x02c3	LO					

Table 35: ExpSensorConstants - [0x02c0 - 0x02c3]

6.3.19 FlashControl

Index	Byte	Register name	Data type	Default	Type	Comment
0x02d0		bFlashMode	C8	0x00	RW	Mode: 0x00: FLASH_OFF 0x01: FLASH_TORCH
0x02d1		fFlashRecommended	C8	0x00	RW	Recommended use of flash: 0x00: FALSE 0x01: TRUE

Table 36: FlashControl - [0x02d0 - 0x02d1]

6.3.20 AntiVignetteControl

Index	Byte	Register name	Data type	Default	Type	Comment
0x02e0	HI	GR_X_Coeff	SI16	0x00 0x00	RW	Antivignette coefficients for Green-in-Red color channel. (ST algorithm AV2x2)
0x02e1	LO					
0x02e2	HI	GR_Y_Coeff	SI16	0x00 0x00	RW	
0x02e3	LO					
0x02e4	HI	GR_X2_Coeff	SI16	0x00	RW	

0x02e5	LO			0x00		
0x02e6	HI	GR_Y2_Coeff	SI16	0x00 0x00	RW	
0x02e7	LO					
0x02e8	HI	GR_XY_Coeff	SI16	0x00 0x00	RW	
0x02e9	LO					
0x02ea	HI	GR_X2Y_Coeff	SI16	0x00 0x00	RW	
0x02eb	LO					
0x02ec	HI	GR_XY2_Coeff	SI16	0x00 0x00	RW	
0x02ed	LO					
0x02ee	HI	GR_X2Y2_Coeff	SI16	0x00 0x00	RW	
0x02ef	LO					
0x02f0	HI	R_X_Coeff	SI16	0x00 0x00	RW	Antivignette coefficients for Red color channel. (ST algorithm AV2x2)
0x02f1	LO					
0x02f2	HI	R_Y_Coeff	SI16	0x00 0x00	RW	
0x02f3	LO					
0x02f4	HI	R_X2_Coeff	SI16	0x00 0x00	RW	
0x02f5	LO					
0x02f6	HI	R_Y2_Coeff	SI16	0x00 0x00	RW	
0x02f7	LO					
0x02f8	HI	R_XY_Coeff	SI16	0x00 0x00	RW	
0x02f9	LO					
0x02fa	HI	R_X2Y_Coeff	SI16	0x00 0x00	RW	
0x02fb	LO					
0x02fc	HI	R_XY2_Coeff	SI16	0x00 0x00	RW	
0x02fd	LO					
0x02fe	HI	R_X2Y2_Coeff	SI16	0x00 0x00	RW	
0x02ff	LO					

0x0300	HI	GB_X_Coeff	SI16	0x00 0x00	RW	Antivignette coefficients for Green-in-Blue color channel. (ST algorithm AV2x2)
0x0301	LO					
0x0302	HI	GB_Y_Coeff	SI16	0x00 0x00	RW	
0x0303	LO					
0x0304	HI	GB_X2_Coeff	SI16	0x00 0x00	RW	
0x0305	LO					
0x0306	HI	GB_Y2_Coeff	SI16	0x00 0x00	RW	
0x0307	LO					
0x0308	HI	GB_XY_Coeff	SI16	0x00 0x00	RW	
0x0309	LO					
0x030a	HI	GB_X2Y_Coeff	SI16	0x00 0x00	RW	
0x030b	LO					
0x030c	HI	GB_XY2_Coeff	SI16	0x00 0x00	RW	
0x030d	LO					
0x030e	HI	GB_X2Y2_Coeff	SI16	0x00 0x00	RW	
0x030f	LO					
0x0310	HI	B_X_Coeff	SI16	0x00 0x00	RW	Antivignette coefficients for Blue color channel. (ST algorithm AV2x2)
0x0311	LO					
0x0312	HI	B_Y_Coeff	SI16	0x00 0x00	RW	
0x0313	LO					
0x0314	HI	B_X2_Coeff	SI16	0x00 0x00	RW	
0x0315	LO					
0x0316	HI	B_Y2_Coeff	SI16	0x00 0x00	RW	
0x0317	LO					
0x0318	HI	B_XY_Coeff	SI16	0x00 0x00	RW	
0x0319	LO					
0x031a	HI	B_X2Y_Coeff	SI16	0x00	RW	

0x031b	LO			0x00		
0x031c	HI	B_XY2_Coeff	SI16	0x00 0x00	RW	
0x031d	LO					
0x031e	HI	B_X2Y2_Coeff	SI16	0x00 0x00	RW	
0x031f	LO					

Table 37: AntiVignette_HostParameters - [0x02e0 - 0x031f]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0320		fEnable	C8	0x01	RW	Enable anti-vignetting: 0x00: FALSE 0x01: TRUE
0x0321		bNbOfPresets	UI8	0x00	RW	Specify number of presets.
0x0322		fAdaptiveAntiVignette ControlEnable	C8	0x00	RW	Enable adaptive anti-vignetting: 0x00: FALSE 0x01: TRUE
0x0323		-	-	-	-	Reserved.
0x0324	HI	fpRedRef0	FP16	0x00 0x00	RW	Normalized Red gain for the 1st color temperature reference. Work with **AdaptiveAntivignetteParameters0**.
0x0325	LO					
0x0326	HI	fpRedRef1	FP16	0x00 0x00	RW	Normalized Red gain for the 2nd color temperature reference. Work with **AdaptiveAntivignetteParameters1**.
0x0327	LO					
0x0328	HI	fpRedRef2	FP16	0x00 0x00	RW	Normalized Red gain for the 3rd color temperature reference. Work with **AdaptiveAntivignetteParameters2**.
0x0329	LO					
0x032a	HI	fpRedRef3	FP16	0x00 0x00	RW	Normalized Red gain for the 4th color temperature reference. Work with **AdaptiveAntivignetteParameters3**.
0x032b	LO					

Table 38: AntiVignette_Controls - [0x0320 - 0x032b]

6.3.21 ColorMatrixDamper

Index	Byte	Register name	Data type	Default	Type	Comment
0x0337		fAdaptiveColorMatrix Enable	C8	0x00	RW	Enable adaptive color matrix: 0x00: FALSE 0x01: TRUE

Table 39: ColorMatrixDamper - [0x0337]

6.3.22 sRGBColorMatrixHost

Index	Byte	Register name	Data type	Default	Type	Comment
0x0340	HI	fpGInR	FP16	0xbc 0x43	RW	Green to Red channel ratio. Default: -0.565
0x0341	LO					
0x0342	HI	fpBInR	FP16	0xba 0x58	RW	Blue to Red channel ratio. Default: -0.293
0x0343	LO					
0x0344	HI	fpRInG	FP16	0xba 0xb4	RW	Red to Green channel ratio. Default: -0.338
0x0345	LO					
0x0346	HI	fpBInG	FP16	0xb8 0x46	RW	Blue to Green channel ratio. Default: -0.142
0x0347	LO					
0x0348	HI	fpRInB	FP16	0xb5 0x75	RW	Red to Blue channel ratio. Default: -0.054
0x0349	LO					
0x034a	HI	fpGInB	FP16	0xbb 0xf0	RW	Green to Blue channel ratio. Default: -0.492
0x034b	LO					

Table 40: sRGBColorMatrixHost - [0x0340 - 0x034b]

6.3.23 SpecialEffectControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0380		fNegative	C8	0x00	RW	Negative effect: 0x00: FALSE 0x01: TRUE

0x0381		fSolarising	C8	0x00	RW	Solarizing effect: 0x00: FALSE 0x01: TRUE
0x0382		fSketch	C8	0x00	RW	Sketch effect: 0x00: FALSE 0x01: TRUE
0x0383		-	-	-	-	Reserved.
0x0384		bColorEffect	C8	0x00	RW	Pre-defined color effect : 0x00 = ColorEffect_Normal 0x01 = ColorEffect_RedOnly 0x02 = ColorEffect_YellowOnly 0x03 = ColorEffect_GreenOnly 0x04 = ColorEffect_BlueOnly 0x05 = ColorEffect_BlackNWhite 0x06 = ColorEffect_Sepia 0x07 = ColorEffect_Antique 0x08 = ColorEffect_Aqua 0x09 = ColorEffect_ManuMatrix When using “ColorEffect_ManuMatrix”, the desired color matrix can be set through registers.

Table 41: SpecialEffectControls - [0x0380 - 0x0384]

6.3.24 sRGBColorMatrix0

Index	Byte	Register name	Data type	Default	Type	Comment
0x03e0~ 0x03eb		sRGBColorMatrix0 registers	FP16	-	RW	RGB color matrix referencing the 1st color temperature with defined **fpNormRedGain0**. Work with adaptive color matrix algorithm. Registers follow similar structure as but with different addresses.
0x03ec	HI	fpNormRedGain0	FP16	0x39 0x7b	RW	Normalized red gain. Default: 0.2175
0x03ed	LO					

Table 42: sRGBColorMatrix0 - [0x03e0 - 0x03ed]

6.3.25 sRGBColorMatrix1

Index	Byte	Register name	Data type	Default	Type	Comment
0x03f0~ 0x03fb		sRGBColorMatrix1 registers	FP16	-	RW	RGB color matrix referencing the 2nd color temperature with defined **fpNormRedGain1**. Work with adaptive color matrix algorithm. Registers follow similar structure as but with different addresses.
0x03fc	HI	fpNormRedGain1	FP16	0x3a 0x22	RW	Normalized red gain. Default: 0.2666
0x03fd	LO					

Table 43: sRGBColorMatrix1 - [0x03f0 - 0x03fd]

6.3.26 sRGBColorMatrix2

Index	Byte	Register name	Data type	Default	Type	Comment
0x0400~ 0x040b		sRGBColorMatrix2 registers	FP16	-	RW	RGB color matrix referencing the 3rd color temperature with defined **fpNormRedGain2**. Work with adaptive color matrix algorithm. Registers follow similar structure as but with different addresses.
0x040c	HI	fpNormRedGain2	FP16	0x3a 0xd6	RW	Normalized red gain. Default: 0.3545
0x040d	LO					

Table 44: sRGBColorMatrix2 - [0x0400 - 0x040d]

6.3.27 sRGBColorMatrix3

Index	Byte	Register name	Data type	Default	Type	Comment
0x0410~ 0x041b		sRGBColorMatrix3 registers	FP16	-	RW	RGB color matrix referencing the 4th color temperature with defined **fpNormRedGain3**. Work with adaptive color matrix algorithm. Registers follow similar structure as but with different addresses.
0x041c	HI	fpNormRedGain3	FP16	0x3b 0x5b	RW	Normalized red gain. Default: 0.4194
0x041d	LO					

Table 45: sRGBColorMatrix3 - [0x0410 - 0x041d]

6.3.28 AdaptiveAntiVignetteParameters0

Index	Byte	Register name	Data type	Default	Type	Comment
0x0420~ 0x045f		AdaptiveAntiVignette Parameters0	SI16	-	RW	Anti-vignette parameters correspond to the 1st color temperature with defined **fpRedRef0**. Work with adaptive anti-vignette algorithm. Registers follow similar structure as but with different addresses.

Table 46: AdaptiveAntiVignetteParameters0 - [0x0420 - 0x045f]

6.3.29 AdaptiveAntiVignetteParameters1

Index	Byte	Register name	Data type	Default	Type	Comment
0x0460~ 0x049f		AdaptiveAntiVignette Parameters1	SI16	-	RW	Anti-vignette parameters correspond to the 2nd color temperature with defined **fpRedRef1**. Work with adaptive anti-vignette algorithm. Registers follow similar structure as but with different addresses.

Table 47: AdaptiveAntiVignetteParameters1 - [0x0460 - 0x049f]

6.3.30 AdaptiveAntiVignetteParameters2

Index	Byte	Register name	Data type	Default	Type	Comment
0x04a0~ 0x04df		AdaptiveAntiVignette Parameters2	SI16	-	RW	Anti-vignette parameters correspond to the 3rd color temperature with defined **fpRedRef2**. Work with adaptive anti-vignette algorithm. Registers follow similar structure as but with different addresses.

Table 48: AdaptiveAntiVignetteParameters2 - [0x04a0 - 0x04df]

6.3.31 AdaptiveAntiVignetteParameters3

Index	Byte	Register name	Data type	Default	Type	Comment
0x04e0~ 0x051f		AdaptiveAntiVignette Parameters3	SI16	-	RW	Anti-vignette parameters correspond to the 4th color temperature with defined **fpRedRef3**. Work with adaptive anti-vignette algorithm. Registers follow similar structure as but with different addresses.

Table 49: AdaptiveAntiVignetteParameters3 - [0x04e0 - 0x051f]

6.3.32 AV_Unity_Offset

Index	Byte	Register name	Data type	Default	Type	Comment
0x0560		Unity_Offset_Generic	SI8	0x00	RW	Unity offset for weighting generation. Range: +/-127
0x0561		Unity_Offset_P0	SI8	0x00	RW	Unity offset for weighting generation. Range: +/-127 Work with **AdaptiveAntivignetteParameters0**.
0x0562		Unity_Offset_P1	SI8	0x00	RW	Unity offset for weighting generation. Range: +/-127 Work with **AdaptiveAntivignetteParameters1**.

0x0563		Unity_Offset_P2	SI8	0x00	RW	Unity offset for weighting generation. Range: +/-127 Work with **AdaptiveAntivignetteParameters2**.
0x0564		Unity_Offset_P3	SI8	0x00	RW	Unity offset for weighting generation. Range: +/-127 Work with **AdaptiveAntivignetteParameters3**.

Table 50: AV_Unity_Offset - [0x0560 - 0x0564]

6.3.33 OTPControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x05a8		bOTPCommand	C8	0x00	RWS	OTP operation command: 0x00: OTP_CMD_IDLE 0x01: OTP_CMD_PROGRAM 0x02: OTP_CMD_READ 0x03: OTP_CMD_EMPTY_CHECK
0x05a9		bOTPStatus	C8	0x20	RO	OTP operation states: [Program and Read operation] 0x10: STATUS_BUSY 0x20: STATUS_READY [Empty check] 0x20: STATUS_PASS 0x30: STATUS_FAIL
0x05aa		ucNumberOf32BitsWords	UI8	0x80	RWS	Number of 32bit words to write/read. Range: 1~64 Default: 128
0x05ab		ucStartAddress	UI8	0x00	RWS	Base address of data transfer. Range: 0~63
0x7300		OTP_pdn	C8	0x00	RWS	Bit[0] Power down OTP (active low): 0: Power down mode 1: Non power down mode
0x7301~ 0x732b		-	-	-	-	Reserved.
0x732c	HI	selectwlbl_pulse_h	UI16	0x00 0x01	RWS	SELECTWLBL pulse high duration
0x732d	LO					
0x732e~ 0x732f		-	-	-	-	Reserved.
0x7330	HI	selectwlbl_pulse_l	UI16	0x00	RWS	SELECTWLBL pulse low duration

0x7331	LO			0x01		
0x7332~ 0x7333		-	-	-	-	Reserved.
0x7334		selectwlbl_hvpulse_r	UI8	0x01	RWS	Time between SELECTWLBL and the rise of HVPULSE.
0x7335~ 0x7337		-	-	-	-	Reserved.
0x7338	HI	hvpulse_h	UI16	0x00 0x01	RWS	HVPULSE pulse high duration.
0x7339	LO					
0x733a~ 0x733b		-	-	-	-	Reserved.
0x733c		hvpulse_selectwlbl_f	UI8	0x01	RWS	Time between HVPULSE and the fall of SELECTWLBL.

Table 51: OTPControls- [0x05a8 - 0x05ab, 0x7300 - 0x733c]

6.3.34 OTP_Buffer

]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0e00~ 0x0eff		OTP buffer registers	UI8	-	RW	A mirror of 2Kbit OTP content in sensor internal buffer. Data is transferred during sensor power up.

Table 52: OTP_Buffer - [0x0e00 - 0x0eff]

6.3.35 TestPattern

Index	Byte	Register name	Data type	Default	Type	Comment
0x05d8		fEnable_TestPattern	C8	0x00	RW	Enable test pattern: 0x00: FALSE 0x01: TRUE
0x05d9		bTest_Pattern	C8	0x00	RW	Test pattern 0x00: No test pattern 0x01: Horizontal grey scale 0x02: Vertical grey scale 0x03: Diagonal grey scale 0x04: PN28 0x05: PN9 0x06: Solid color 0x07: Color bars 0x08: Graduated color bars
0x4304	HI	uwTestdata_Red	UI16	0x00	RW	Test data used for Solid color test

0x4305	LO			0x00		pattern. Replace Red pixel data. Range: 0~1023
0x4306~ 0x4307		-	-	-	-	Reserved.
0x4308	HI	uwTestdata_GreenR	UI16	0x00 0x00	RW	Test data used for Solid color test pattern. Replace Green in Red pixel data. Range: 0~1023
0x4309	LO					
0x430a~ 0x430b		-	-	-	-	Reserved.
0x430c	HI	uwTestdata_Blue	UI16	0x00 0x00	RW	Test data used for Solid color test pattern. Replace Blue pixel data. Range: 0~1023
0x430d	LO					
0x430e~ 0x430f		-	-	-	-	Reserved.
0x4310	HI	uwTestdata_GreenB	UI16	0x00 0x00	RW	Test data used for Solid color test pattern. Replace Green in Blue pixel data. Range: 0~1023
0x4311	LO					

Table 53: TestPattern- [0x05d8, 0x05d9, 0x4304 - 0x4311]

6.3.36 ContrastStretchControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x05e8		fEnable	C8	0x00	RW	Enable contrast stretching 0x00: FALSE 0x01: TRUE
0x05e9	HI	fpGainCeiling	FP16	0x3f 0x00	RW	Maximum allowed gain. Default: 1.5
0x05ea	LO					
0x05eb		bBlackOffsetCeiling	UI8	0x19	RW	Maximum allowed black offset. Default: 25
0x05ec	HI	fpWhitePixTarget	FP16	0x3c 0x00	RW	Number of pixels in percentage for upper stretching limit. Default: 0.5%
0x05ed	LO					
0x05ee	HI	fpBlackPixTarget	FP16	0x39 0x33	RW	Number of pixels in percentage for lower stretching limit. Default: 0.2%
0x05ef	LO					

Table 54: CSControls - [0x05e8 - 0x05ef]

6.3.37 ContrastStretchStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x05f8		fEnabled	C8	0x00	RO	Contrast stretching enabled status: 0x00: FALSE 0x01: TRUE
0x05f9	HI	fpTotalPixel	FP16	0x00 0x00	RO	Number of pixels accumulated within the image.
0x05fa	LO					
0x05fb	HI	udwWTarget	UI32	0x00 0x00 0x00 0x00	RO	Number of pixels cut off on the high tones.
0x05fc	3rd					
0x05fd	2nd					
0x05fe	LO					
0x05ff	HI	udwBTarget	UI32	0x00 0x00 0x00 0x00	RO	Number of pixels cut off on the low tones.
0x0600	3rd					
0x0601	2nd					
0x0602	LO					
0x0603	HI	fpGain	FP16	0x00 0x00	RO	Contrast stretching strength
0x0604	LO					
0x0605		bBlackOffset	UI8	0x00	RO	Lower limit of histogram
0x0606		bWhiteLimit	UI8	0x00	RO	Upper limit of histogram.

Table 55: CSStatus - [0x05f8 - 0x0606]

6.3.38 PresetControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0638		fPresetLoaderEnable	C8	0x00	RWS	Enable loading of OTP preset 0x00: FALSE 0x01: TRUE
0x0639		fIndividualPreset	C8	0x00	RWS	Disable/Enable individual preset: Bit[0]: Antivignette preset Bit[1]: White balance preset Bit[4]: VCM preset 0: Disable 1: Enable

Table 56: PresetControls - [0x0638 - 0x0639]

6.3.39 JPEGControlParameters

Index	Byte	Register name	Data type	Default	Type	Comment
0x0649		bStatus	UI8	0x00	RO	Count the number of corrupted JPEG frames. This value is reset to zero when good JPEG frame is output.
0x064a		bRestart	UI8	0xFF	RW	Specify the number of bytes to restart JPEG decoding if error occured.
0x064b		bHiSqueezeValue	UI8	0x05	RW	Squeeze factor for high quality. Range: 5 (highest quality) ~ 255 (lowest quality)
0x064c		bMedSqueezeValue	UI8	0x18	RW	Squeeze factor for medium quality. Default: 24
0x064d		bLowSqueezeValue	UI8	0x28	RW	Squeeze factor for low quality. Default: 40
0x064e	HI	uwLineLength	UI16	0x02 0x00	RWS	Set how many bytes of JPEG data in each Packet (line), must be equal or less than **uwThres**. Default: 512
0x064f	LO					
0x0650		bClockRatio	UI8	0x03	RWS	JPEG output clock ratio: 0x01: clock / 1 0x02: clock / 2 0x03: clock / 3 0x04: clock / 4 0x06: clock / 6 0x08: clock / 8
0x0651	HI	uwThres	UI16	0x02 0x06	RWS	Set how many bytes of JPEG data in buffer before sending, must be equal or larger than **uwLineLength**. Default: 518
0x0652	LO					
0x0653	HI	dwByteSent	UI32	0x00 0x00 0x00 0x00	RO	Number of JPEG data (in bytes) are sent.
0x0654	3rd					
0x0655	2nd					
0x0656	Lo					

Table 57: JPEGControlParameters - [0x0649 - 0x0656]

6.3.40 AFStatsControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x065a		bWindowsSystem	C8	0x00	RW	Specifies different statistics zones: 0x00: 7 zones system 0x01: 1 zone system
0x065b		bHRatio_Num	UI8	0x01	RW	Horizontal width of Window-Of-Interest (WOI) with respect to maximum array size. Default: 1/6 WOI is defined with registers **uwFaceLocationXStart**, **uwFaceLocationYStart**, **uwFaceLocationXSize**, and **uwFaceLocationYSize** in
0x065c		bHRatio_Den	UI8	0x06	RW	
0x065d		bVRatio_Num	UI8	0x01	RW	Vertical height of Window-Of-Interest (WOI) with respect to maximum array size. Default: 1/9 WOI is defined with registers **uwFaceLocationXStart**, **uwFaceLocationYStart**, **uwFaceLocationXSize**, and **uwFaceLocationYSize** in
0x065e		bVRatio_Den	UI8	0x09	RW	

Table 58: AFStatsControls - [0x065a - 0x065e]

6.3.41 AFStatsStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x066b		bWindowsSystem	C8	0x00	RO	Selected window system: 0x00: 7 zones system 0x01: 1 zone system
0x066c		bActiveZonesCounter	UI8	0x07	RO	Number of active zones.
0x066d		bHRatio_Num	UI8	0x01	RO	Horizontal width of Window-Of-Interest (WOI) with respect to maximum array size. Default: 1/6
0x066e		bHRatio_Den	UI8	0x06	RO	
0x066f		bVRatio_Num	UI8	0x01	RO	Vertical height of Window-Of-Interest

0x0670		bVRatio_Den	UI8	0x09	RO	(WOI) with respect to maximum array size. Default: 1/9
0x0671	HI	uwWOI_Width	UI16	0x0a 0x06	RO	Horizontal width of WOI Default: 2566
0x0672	LO					
0x0673	HI	uwWOI_Height	UI16	0x07 0x85	RO	Vertical height of WOI Default: 1925
0x0674	LO					
0x0675	HI	uwAFZones_Width	UI16	0x01 0xab	RO	Horizontal width of a zone Default: 427
0x0676	LO					
0x0677	HI	uwAFZones_Height	UI16	0x00 0xd5	RO	Vertical height of a zone Default: 213
0x0678	LO					

Table 59: AFStatsStatus - [0x066b - 0x0678]

6.3.42 FLADriverLowLevelParameters

Index	Byte	Register name	Data type	Default	Type	Comment
0x06cd	HI	AF_OTP_ uwHostDefMacro	UI16	0x00 0x00	RWS	Host defined lens Macro position for VCM driver Range: 0~1023 codes
0x06ce	LO					
0x06cf	HI	AF_OTP_ uwHostDefInfinity	UI16	0x00 0x00	RWS	Host defined lens Infinity position for VCM driver Range: 0~1023 codes
0x06d0	LO					
0x06d1~ 0x06d3		-	-	-	-	Reserved.
0x06d4		AF_OTP_ fHostEnableOTPRead	C8	0x00	RWS	Enable/Disable VCM driver operating range (Macro / Infinity position) to be read from OTP: 0x00: OTP_READ_ENABLE 0x01: OTP_READ_DISABLE
0x06d5	HI	AF_VCM_ uwLowLevelMacroPos	UI16	0x00 0x00	RWS	Contain the final low level (VCM driver) Macro position to be used in the AF algorithm. Value is obtained from **AF_OTP_uwHostDefMacro** or OTP content.
0x06d6	LO					
0x06d7	HI	AF_VCM_	UI16	0x00	RWS	Contain the final low level (VCM

0x06d8	LO	uwLowLevelInfinityPos		0x00		driver) Infinity position to be used in the AF algorithm. Value is obtained from **AF_OTP_uwHostDefInfinity** or OTP content.
0x06d9~ 0x06de		-	-	-	-	Reserved.
0x06df	HI	uwLowLevelHorMacro	UI16	0x00 0x00	RWS	Macro position when VCM module is placed horizontally. Value could come from OTP content.
0x06e0	LO					
0x06e1	HI	uwLowLevelHorInfinity	UI16	0x00 0x00	RWS	Infinity position when VCM module is placed horizontally. Value could come from OTP content.
0x06e2	LO					

Table 60: FLADriverLowLevelParameters - [0x06cd - 0x06e2]

6.3.43 FLADriverStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x06f0	HI	wLensPositionStatus	UI16	0x01 0xFC	RO	Current DAC value of VCM driver. Default: 508
0x06f1	LO					
0x06f2		fLensIsMoving	C8	0x00	RO	Lens moving status: 0x00: FALSE 0x01: TRUE
0x06f3~ 0x06f6		-	-	-	-	Reserved.
0x06f7		bCycles	UI8	0x00	RO	8-bit counter to indicate proper VCM driver operation.

Table 61: FLADriverStatus - [0x06f0 - 0x06f7]

6.3.44 FLADriverControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0700	HI	wTargetPosition	UI16	0x00 0x00	RW	Targeted DAC value of VCM driver. Work with **FocusControls -> bLensCommand** (LA_CMD_GOTO_TARGET_POSITION)
0x0701	LO					

Table 62: FLADriverControls - [0x0700 - 0x0701]

6.3.45 FocusControls

Index	Byte	Register name	Data type	Default	Type	Comment
xx0709		bRange	C8	0x00	RW	Operating ranges: 0x00: FOCUS_RANGE_FULLRANGE 0x01: FOCUS_RANGE_LANDSCAPE 0x02: FOCUS_RANGE_MACRO
0x070a		bMode	C8	0x00	RW	Focusing modes: 0x00: FC_TLI_MODE_MANUAL_FOCUS 0x01: FC_TLI_MODE_AF_ CONTINUOUS_FOCUS 0x03: FC_TLI_MODE_AF_ SINGLE_FOCUS_DOUBLE_PASS_HCS
0x070b		bAFCommand	C8	0x00	RW	Auto focus commands: 0x00: AF_TLI_CMD_NULL 0x01: AF_TLI_CMD_RELEASED_BUTTON 0x02: AF_TLI_CMD_HALF_BUTTON 0x03: AF_TLI_CMD_TAKE_SNAPSHOT 0x04: AF_TLI_CMD_REFOCUS
0x070c		bLensCommand	C8	0x00	RW	Manual focus commands: 0x00: LA_CMD_NULL 0x01: LA_CMD_MOVE_STEP_TO_INFINITY 0x02: LA_CMD_MOVE_STEP_TO_MACRO 0x03: LA_CMD_GOTO_INFINITY 0x04: LA_CMD_GOTO_MACRO 0x05: LA_CMD_GOTO_RECOVERY 0x07: LA_CMD_GOTO_TARGET_POSITION 0x0C: LA_CMD_GOTO_HYPERFOCAL
0x070d		bManualStep_Size	UI8	0x14	RW	Specify the step size during manual focusing. Default: 20
0x070e~ 0x0713		-	-	-	-	Reserved.
0x0714		bFaceLocationControl Enable	C8	0x00	RW	Enable various statistics gathering from face location specified by **uwFaceLocationXStart**, **uwFaceLocationYStart**, **uwFaceLocationXSize**, and **uwFaceLocationYSize**. Bit[0]: Auto Focus statistics Bit[1]: Auto Exposure statistics Bit[2]: Auto White Balance statistics 0: FALSE 1: TRUE
0x0715	HI	uwFaceLocationXStart	UI16	0x00 0x00	RW	Specify the first column of output image for statistics gathering.
0x0716	LO					
0x0717	HI	uwFaceLocationXSize	UI16	0x00	RW	Specify the number of columns for

0x0718	LO			0x00		statistics gathering. Column begins with value set in register **uwFaceLocationXStart**.
0x0719	HI	uwFaceLocationYStart	UI16	0x00	RW	Specify the first row of output image for statistics gathering.
0x071a	LO			0x00		
0x071b	HI	uwFaceLocationYSize	UI16	0x00	RW	Specify the number of rows for statistics gathering. Row begins with value set in register **uwFaceLocationYStart**.
0x071c	LO			0x00		

Table 63: FocusControls - [0x0709 - 0x071c]

6.3.46 FocusStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x0720		bModeStatus	C8	0x00	RO	Selected focusing modes: 0x00: FC_TLI_MODE_MANUAL_FOCUS 0x01: FC_TLI_MODE_AF_ CONTINUOUS_FOCUS 0x03: FC_TLI_MODE_AF_ SINGLE_FOCUS_DOUBLE_PASS_HCS
0x0721		bAFCommandStatus	C8	0x00	RO	Current auto focus command: 0x00: AF_TLI_CMD_NULL 0x01: AF_TLI_CMD_RELEASED_BUTTON 0x02: AF_TLI_CMD_HALF_BUTTON 0x03: AF_TLI_CMD_TAKE_SNAPSHOT 0x04: AF_TLI_CMD_REFOCUS
0x0722		bLensCommandStatus	C8	0x00	RO	Current manual focus command: 0x00: LA_CMD_NULL 0x01: LA_CMD_MOVE_STEP_TO_INFINITY 0x02: LA_CMD_MOVE_STEP_TO_MACRO 0x03: LA_CMD_GOTO_INFINITY 0x04: LA_CMD_GOTO_MACRO 0x05: LA_CMD_GOTO_RECOVERY 0x07: LA_CMD_GOTO_TARGET_POSITION 0x0C: LA_CMD_GOTO_HYPERFOCAL
0x0723		fAutoFocusEnabled	C8	0x00	RO	Auto focus enabled status: 0x00: FALSE 0x01: TRUE
0x0724		bRange	C8	0x00	RO	Selected operating range: 0x00: FOCUS_RANGE_FULLRANGE 0x01: FOCUS_RANGE_LANDSCAPE 0x02: FOCUS_RANGE_MACRO
0x0725		fIsStable	C8	0x01	RO	Signalling the VCM driver is stable: 0x00: FALSE 0x01: TRUE
0x0726~ 0x0728		-	-	-	-	Reserved.

0x0729		bCycles	UI8	0x00	RO	8-bit counter to indicate proper focusing operation.

Table 64:FocusStatus - [0x0720 - 0x0729]

6.3.47 FocusRangeConstants

Index	Byte	Register name	Data type	Default	Type	Comment
0x0730	HI	wFullRange_ LensMinPosition	UI16	0x00 0x00	RW	Host defined **Full Range** set: (minimum focus range)
0x0731	LO					
0x0732	HI	wFullRange_ LensMaxPosition	UI16	0x01 0xFF	RW	Host defined **Full Range** set: (maximum focus range) Default: 511
0x0733	LO					
0x0734	HI	wFullRange_ LensRecoveryPosition	UI16	0x01 0xFC	RW	Host defined **Full Range** set: (recovery position) Default: 508
0x0735	LO					
0x0736	HI	wLandscape_ LensMinPosition	UI16	0x00 0x00	RW	Host defined **Landscape Range** set: (minimum focus range)
0x0737	LO					
0x0738	HI	wLandscape_ LensMaxPosition	UI16	0x00 0xFA	RW	Host defined **Landscape Range** set: (maximum focus range) Default: 250
0x0739	LO					
0x073a	HI	wLandscape_ LensRecoveryPosition	UI16	0x00 0x00	RW	Host defined **Landscape Range** set: (recovery position)
0x073b	LO					
0x073c	HI	wMacro_ LensMinPosition	UI16	0x00 0xC8	RW	Host defined **Macro Range** set: (minimum focus range) Default: 200
0x073d	LO					
0x073e	HI	wMacro_ LensMaxPosition	UI16	0x01 0x90	RW	Host defined **Macro Range** set: (maximum focus range) Default: 400
0x073f	LO					
0x0740	HI	wMacro_ LensRecoveryPosition	UI16	0x01 0x2C	RW	Host defined **Macro Range** set: (recovery position) Default: 300
0x0741	LO					

Table 65: FocusRangeConstants - [0x0730 - 0x0741]

6.3.48 AutoFocusControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0756		bSelectedMultizone Behavior	C8	0x03	RW	Determine the processing method for the AF zones: 0x00: REGIONSELECTIONMETHOD_ AVERAGE 0x01: REGIONSELECTIONMETHOD_ MAXMEASURE 0x02: REGIONSELECTIONMETHOD_ MEASURERANGE 0x03: REGIONSELECTIONMETHOD_ AUTO
0x0757~ 0x0763		-	-	-	-	Reserved.
0x0764		fResetHCSPos	C8	0x00	RW	Enable the AF algorithm to start with the recovery position defined in : 0x00: FALSE 0x01: TRUE

Table 66: AutoFocusControls - [0x0756 - 0x0764]

6.3.49 AutoFocusConstants

Index	Byte	Register name	Data type	Default	Type	Comment
0x0770		bCoarseStep	UI8	0x00	RW	Specify the coarse step size (in codes) of the auto focus algorithm. The number of AF major steps can be determined by dividing the maximum focus range with this value.
0x0771		bFineStep	UI8	0x00	RW	Specify the fine step size (in codes) of the auto focus algorithm. The number of AF minor steps can be determined by dividing the **bCoarseStep** with this value.
0x0772		bFullSearchStep	UI8	0x00	RW	Specify the step size (in codes) of the auto focus algorithm during full search operation.

Table 67: AutoFocusConstants - [0x0770 - 0x0772]

6.3.50 AutoFocusStatus

Index	Byte	Register name	Data type	Default	Type	Comment
0x07a0		bCycles	UI8	0x00	RO	8-bit counter to indicate proper AF operation.
0x07a1~ 0x07ad		-	-	-	-	Reserved.
0x07ae		fInFocus	C8	0x00	RO	Signalling the completion of auto focus algorithm: 0x00: FALSE 0x01: TRUE

Table 68: AutoFocusStatus - [0x07a0 - 0x07ae]

6.3.51 AutoFocusWeightControls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0808		bWeight_0	UI8	0x01	RW	AF zone 0 weighting (center zone in the eye shape default configuration)
0x0809		bWeight_1	UI8	0x01	RW	AF zone 1 weighting (center-left zone in the eye shape default configuration)
0x080a		bWeight_2	UI8	0x01	RW	AF zone 2 weighting (center-right zone in the eye shape default configuration)
0x080b		bWeight_3	UI8	0x01	RW	AF zone 3 weighting (top-left zone in the eye shape default configuration)
0x080c		bWeight_4	UI8	0x01	RW	AF zone 4 weighting (top-right zone in the eye shape default configuration)
0x080d		bWeight_5	UI8	0x01	RW	AF zone 5 weighting (bottom-left zone in the eye shape default configuration)
0x080e		bWeight_6	UI8	0x01	RW	AF zone 6 weighting (bottom-right zone in the eye shape default configuration)
0x080f		bWeight_7	UI8	0x01	RW	AF zone 7 weighting (not used in the eye shape default configuration)

0x0810		bWeight_8	UI8	0x01	RW	AF zone 8 weighting (not used in the eye shape default configuration)
0x0811		bWeight_9	UI8	0x00	RW	AF zone 9 weighting (not used in the eye shape default configuration)

Table 69: AutoFocusWeightControls - [0x0808 - 0x0811]

6.3.52 EXIF_Controls

Index	Byte	Register name	Data type	Default	Type	Comment
0x0878		bInhibit_EXIF	C8	0x00	RW	Disable EXIF information: 0x00: FALSE 0x01: TRUE
0x0879	HI	Make_lower	UI32	0x00 0x00 0x00 0x00	RW	Manufacturer name (8 ASCII characters).
0x087a	3rd					
0x087b	2nd					
0x087c	LO					
0x087d	HI	Make_upper	UI32	0x00 0x00 0x00 0x00	RW	
0x087e	3rd					
0x087f	2nd					
0x0880	LO					
0x0881	HI	Model_lower	UI32	0x00 0x00 0x00 0x00	RW	Model name (8 ASCII characters).
0x0882	3rd					
0x0883	2nd					
0x0884	LO					
0x0885	HI	Model_upper	UI32	0x00 0x00 0x00 0x00	RW	
0x0886	3rd					
0x0887	2nd					
0x0888	LO					
0x0889	HI	Aptr_lower	UI32	0x00 0x00 0x00	RW	Denominator for aperture value.
0x088a	3rd					

0x088b	2nd			0x00		
0x088c	LO					
0x088d	HI	Aptr_upper	UI32	0x00 0x00 0x00 0x00	RW	Numerator for aperture value.
0x088e	3rd					
0x088f	2nd					
0x0890	LO					
0x0891		XRes	UI8	0x48	RW	Horizontal resolution in DPI Default: 72
0x0892		YRes	UI8	0x48	RW	Vertical resolution in DPI Default: 72

Table 70: EXIF_Controls - [0x0878 - 0x0892]

6.3.53 EXIF_OTP_Preset

Index	Byte	Register name	Data type	Default	Type	Comment
0x08a8	HI	Make_lower	UI32	0x00 0x00 0x00 0x00	RW	Manufacturer name (8 ASCII characters).
0x08a9	3rd					
0x08aa	2nd					
0x08ab	LO					
0x08ac	HI	Make_upper	UI32	0x00 0x00 0x00 0x00	RW	
0x08ad	3rd					
0x08ae	2nd					
0x08af	LO					
0x08b0	HI	Model_lower	UI32	0x00 0x00 0x00 0x00	RW	Model name (8 ASCII characters).
0x08b1	3rd					
0x08b2	2nd					
0x08b3	LO					
0x08b4	HI	Model_upper	UI32	0x00 0x00 0x00 0x00	RW	
0x08b5	3rd					
0x08b6	2nd					

0x08b7	LO					
0x08b8	HI	Aptr_lower	UI32	0x00 0x00 0x00 0x00	RW	Denominator for aperture value.
0x08b9	3rd					
0x08ba	2nd					
0x08bb	LO					
0x08bc	HI	Aptr_upper	UI32	0x00 0x00 0x00 0x00	RW	Numerator for aperture value.
0x08bd	3rd					
0x08be	2nd					
0x08bf	LO					
0x08c0		XRes	UI8	0x00	RW	Horizontal resolution in DPI
0x08c1		YRes	UI8	0x00	RW	Vertical resolution in DPI

Table 71: EXIF_OTP_Preset - [0x08a8 - 0x08c1]

Index	Byte	Register name	Data type	Default	Type	Comment
0x30c0	HI	sscg_mod_period	16UI	0x00 0x00	RW	Bit[12:0] 13-bit modulation period.
0x30c1	LO					
0x30c2~ 0x30c3	-	-	-	-	-	Reserved.
0x30c4	HI	sscg_inc_step	16UI	0x00 0x00	RW	Bit[14:0] 15-bit modulation depth
0x30c5	LO					
0x30c6~ 0x30c7	-	-	-	-	-	Reserved.
0x30c8		sscg_strb	8UI	0x00	RW	Trigger to strobe mod_period and inc_step and spread control together: 0x00: No strobe input 0x01: Asynchonous strobe input (0x01 -> 0x00)[8]
0x30c9~ 0x30cb	-	-	-	-	-	Reserved.

[8]Strobing signal needs at least two FBCLK (feedback clock of PLL) clock cycles where FBCLK = PLL output freq / PLL divider.

0x30cc		sscg_strb_bypass	8UI	0x00	RW	Strobe bypass: 0x00: No bypass 0x01: Bypass inputs without registering the strobe signal
0x30cd~ 0x30cf	-	-	-	-	-	Reserved.
0x30d0		sscg_spread_control	8UI	0x01	RW	Spread mode: 0x00: Center spread 0x01: Down spread
0x30d1~ 0x30d3	-	-	-	-	-	Reserved.
0x30d4		sscg_control	8UI	0x00	RW	Spread spectrum modulation: 0x00: Disable 0x01: Enable

Table 72: Spread spectrum clock generator settings - [0x30c0 - 0x30d4]

7 Test patterns

The test patterns are more suitable for some deterministic tests than real image data and are injected early in the sensor data path. The only exception to this is the PN9 test pattern that is intended to test sensor-host link integrity; the data in this pattern is not raw data and is injected into the data stream just prior to CSI framing.

Use of these full frame test patterns is controlled by the registers **fEnable_TestPattern** (0x05D8) and **bTest_Pattern** (0x05D9). The available modes are:

1 – Horizontal grey scale
2 – Vertical grey scale
3 – Diagonal grey scale
4 – PN28 pseudo random
5 – PN9 pseudo random
6 – Solid color
7 – 100% color bars
8 – Graduated color bars

In both the default parameter state and in any undefined parameter states, normal array data should be output rather than a test pattern. The individual test patterns are described later in this chapter.

7.1 100% Color Bars Pattern

In the '100% color bar' test pattern mode all pixel data is replaced with a raw version of an 8-bar color bar pattern. In each bar all pixels are either 0% or 100% full scale (for example, 100/0/100/0 bars).

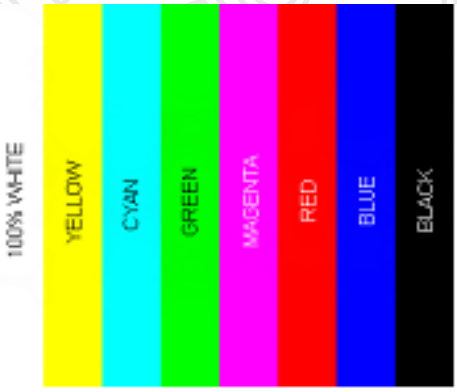


Figure 48 100% color bars

7.2 Graduated Color Bar

In the graduated color bar test pattern mode, all pixel data are replaced with a color bar that fades vertically from 100% color bars to mid grey. The graduated color bar pattern is designed to exercise more of the color space than 100% bar pattern. The following figure gives an indication of the pattern (although the pattern is generated as raw data).

Figure 49 Graduated color bars

The pattern is made up of eight vertical bars that fade vertically from one of the 100% color bar colors towards a mid-grey at the bottom. The bars follow the same order as standard color bars. Each of the bars is sub-divided vertically into a left hand side that contains a smooth gradient and a right hand size that contains a quaintest version.

The aim of the quaintest portion is to offer areas of flat-field raw data that should be large enough to result in known data values even after demoniac (independently of the demoniac algorithm). To ensure maximum dynamic range in the quaintest data, the LSBs of the quaintest data is generated by copying the MSBs of the unquantized data (rather than forcing them to 0). The pattern may roll over and repeat if the frame is long enough.

7.3 Horizontal Grey Scale

In this test pattern mode, each of the pixel data in same column is replaced with value which increment horizontally starting from 0 to the maximum pixel value of 1023. The test pattern is repeated when the number of columns is larger than the maximum pixel output.

Figure 50 Horizontal grey scale pattern

7.4 Vertical Grey Scale

In this test pattern mode, each of the pixel data in same row is replaced with value which increment vertically starting from 0 to the maximum value of 1023 (10bit). The test pattern is repeated when the number of rows is larger than the maximum pixel output.

Figure 51 Vertical grey scale pattern

7.5 Diagonal Grey Scale

In this test pattern mode, all pixel data is replaced with an incrementing value which filling the pixel array in diagonal direction, i.e. from top left to bottom right. The grey scale pattern increments from 0 to 1023 (10bit). The test pattern is repeated when there is a rollover on maximum pixel output.

Figure 52 Diagonal grey scale pattern

7.6 PN9 Mode

In the 'PN9' test pattern mode all data on all lines between FS and LS code and the LE or FE code is replaced with data from internally generated 511-bit pseudo-random 'PN9' sequence.

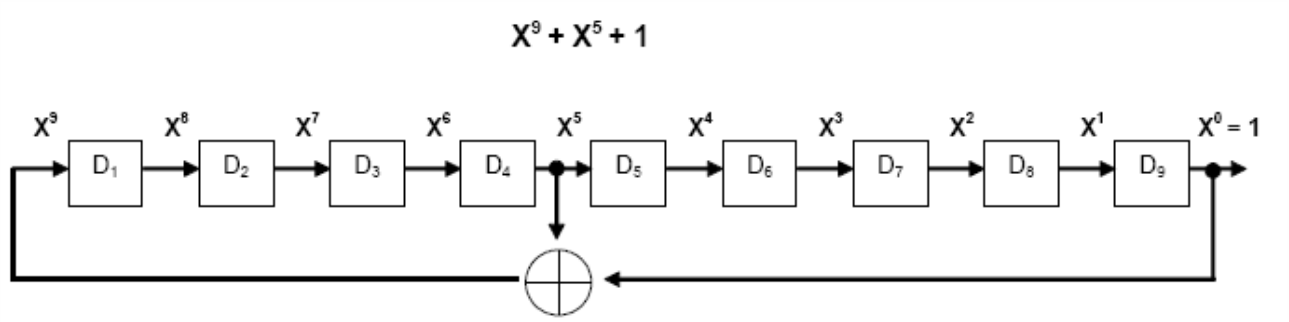


Figure 53 PN9 linear feedback filter

The PN9 test pattern is included to ease testing of sensor-link integrity (measurement of bit error rate etc). The standard PN9 linear feedback shift register with polynomial X^9+X^5+1 in Fibonacci-type notation is shown in **Figure** 53 PN9 linear feedback filter. The PN9 sequence generator is reset at the start of the frame, the sequence is then in a known state (0x1FF) at the first replaced pixel of each frame.

8 Electrical characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STO}	Storage temperature	-40	85	℃
AVDD	Analog power supplies	-0.5	3.3	V

Table 73: Absolute maximum ratings

Caution: Stress above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{AF}	Operating temperature, functional (Imaging sensor is electrically functional)	-30	25	70	°C
T_{AN}	Operating temperature, nominal (Imaging sensor produces acceptable images)	-25	25	55	°C
T_{AO}	Operating temperature, optimal (Imaging sensor produces optimal optical performance)	5	25	30	°C
IOVDD	Digital power supplies operating range	TBD	1.8	TBD	V
		TBD	2.6	TBD	V
AVDD	Analog power supplies operating range (@ module pin(6))	TBD	2.8	TBD	V

Table 74: Supply specifications

8.3 DC Electrical Characteristics

Note:1 *All values are typical values only and are not yet characterized.*

2 *Over operating conditions unless otherwise specified.*

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage		-0.3		0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output low voltage	I_{OL} < 2 mA I_{OL} < 4 mA			0.2 V_{DD} 0.4 V_{DD}	V
V_{OH}	Output high voltage	I_{OH}< 4 mA	0.8 V_{DD}			V
I_{IL}	Input leakage current Input pins I/O pins	0 < V_{IN} < V_{DD}			+/- 10 +/- 1	A A
C_{IN}	Input capacitance, SCL	T_A = 25 ℃, freq = 1 MHz			6	pF
C_{OUT}	Output capacitance	T_A = 25 ℃, freq = 1 MHz			6	pF
$C_{I/O}$	I/O capacitance, SDA	T_A = 25 ℃, freq = 1 MHz			8	pF

Table 75: DC electrical characteristics

Symbol	Description	Test conditions	I_{AVDD}	I_{IOVDD}		Units
			AVDD = 2.8V	IOVDD = 1.8V	IOVDD = 2.6V	
I_{PD}	Supply current in h/w standby	CE=0, CLK = 12 MHz	2.8	2	4.2	uA

Table 76: Current consumption in standby modes

Symbol	Mode	Resolution	I_{AVDD}	I_{IOVDD}		Units
			AVDD = 2.8V	IOVDD = 1.8V	IOVDD = 2.6V	
I_{run}	SR	5MP (full size, YCbYCr @ 7.5FPS)	50	48	66	mA
		5MP (full size, YUV JPEG @ 15 FPS)	54	92	88	mA

Table 77: ITU Current consumption in streaming modes[13]

Symbol	Mode	Resolution	I_{AVDD}	I_{IOVDD}		Units
			AVDD = 2.8V	IOVDD = 1.8V	IOVDD = 2.6V	
I_{run}	SR	5MP (full size)	56.5	48.4	48.8	mA

Table 78: CSI2-DL Current consumption in streaming modes[14]

8.4 External Clock

The HM5065 requires an external clock. This clock is a CMOS digital input. The clock input is fail-safe in power down mode and should be a DC coupled square wave.

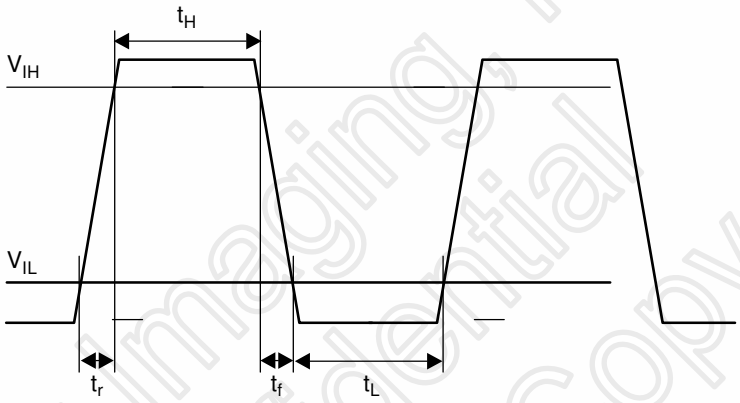


Figure 54 External PCLK timing

Parameter	Description	Range			Unit
		Min.	Typ.	Max.	
Freq.[15]	Clock frequency	6		27	MHz
V_{IH}	Clock input high level (Vdd = 1.8V range)	0.7 * Vdd			V
V_{IL}	Clock input low level (Vdd = 1.8V range)			0.3 * Vdd	V
V_{IH}	Clock input high level (Vdd = 2.8V range)	2.0			V
V_{IL}	Clock input low level (Vdd = 2.8V range)			0.8	V
t_r, t_f	Transition time	0.5		16	Ns
t_H, t_L	High, low period	10			Ns

Table 79: External clock

8.5 Serial Slave Interface

HM5065 contains an I²C-type interface using two signals: a bidirectional serial data line (SDA) and an input-only serial clock line (SCL). See *Section 3.11.2: PLL operation* for detailed description of protocol.

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs V_{DD} > 2 V V_{DD} < 2V	 N/A N/A	 N/A N/A	 0.05 V_{DD} 0.1 V_{DD}	 - -	 V V
V_{OL1} V_{OL3}	LOW level output voltage (open drain) at 3mA sink current V_{DD} > 2 V V_{DD} < 2V	 0 N/A	 0.4 N/A	 0 0	 0.4 0.2 V_{DD}	 V V
V_{OH}	HIGH level output voltage	N/A	N/A	0.8 V_{DD}		V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	-	250	20+0.1C_b[16]	250	Ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	N/A	N/A	0	50	Ns

Table 80: Serial interface voltage levels[18]

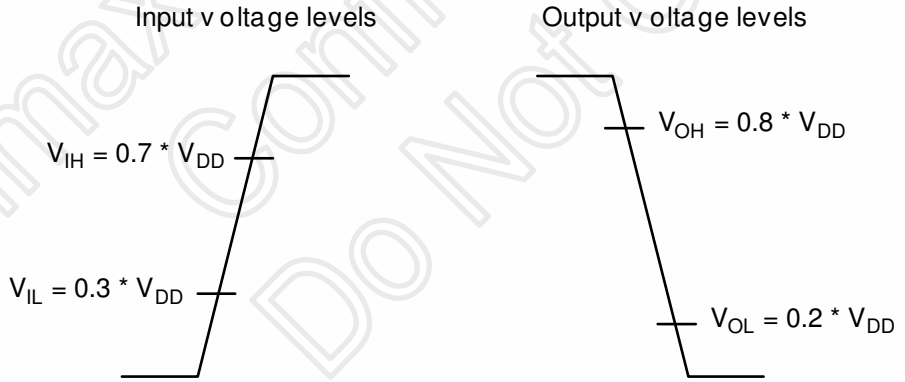
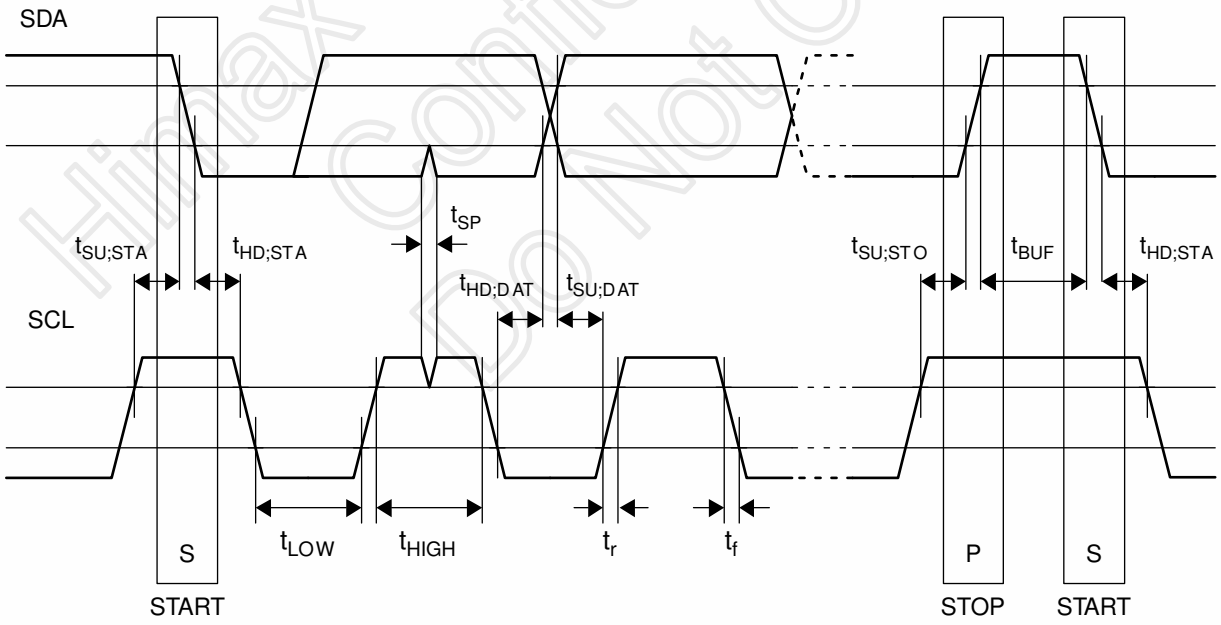


Figure 55 Voltage level specification

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for a repeated ***start***	4.0	-	0.6	-	µs

t_{LOW}	LOW period of SCL	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of SCL	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated ***start***	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time (1)	300	-	300	-	ns
$t_{SU;DAT}$	Data Set-up time (1)	250	-	100	-	ns
t_r	Rise time of SCL, SDA	-	1000	$20+0.1Cb^{8}$	300	ns
t_f	Fall time of SCL, SDA	-	300	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for a ***stop***	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a ***stop*** and a ***start***	4.7	-	1.3	-	µs
C_b	Capacitive Load for each bus line	-	400	-	400	pF
V_{nL}	Noise Margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	-	0.1 V_{DD}	-	V
V_{nH}	Noise Margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	-	0.2 V_{DD}	-	V

Table 81: Timing specification20



All values are referred to a V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD}

Figure 56 Timing specification

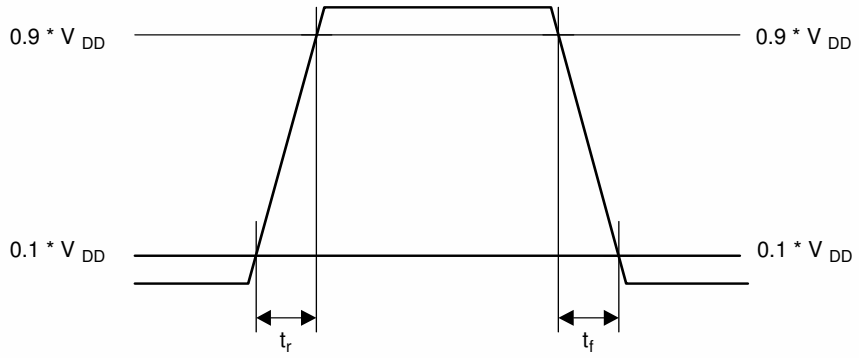


Figure 57 SDA/SCL rise and fall times

8.6 Parallel Data Interface Timing

HM5065 contains a parallel data output port (D[7:0]) and associated qualification signals (HSYNC, VSYNC, PCLK and FSO).

This port can be enabled and disabled (tri-stated) to facilitate multiple imaging sensor systems or bit-serial output configurations. The port is disabled (high impedance) on reset.

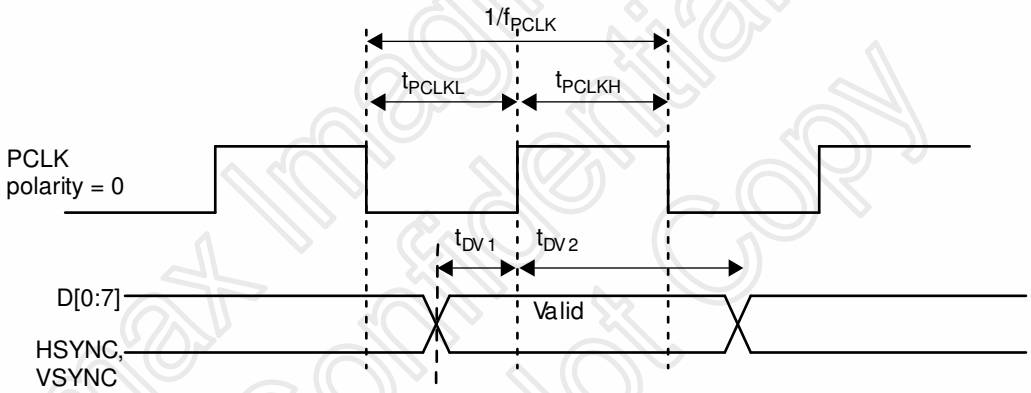


Figure 58 Parallel data output video timing

Symbol	Description	Min.	Max.	Unit
f_{PCLK}	PCLK frequency	2	80	MHz
t_{PCLKL}	PCLK low width	(1/2 * (1/fPCLK)) -1	(1/2 * (1/fPCLK)) +1	ns
t_{PCLKH}	PCLK high width	(1/2 * (1/fPCLK)) -1	(1/2 * (1/fPCLK)) +1	ns
t_{DV1}	Time between PCLK positive edge and data changing	3		ns
t_{DV2}	Time between data changing and PCLK positive	7		ns

Table 82: Parallel data interface timings

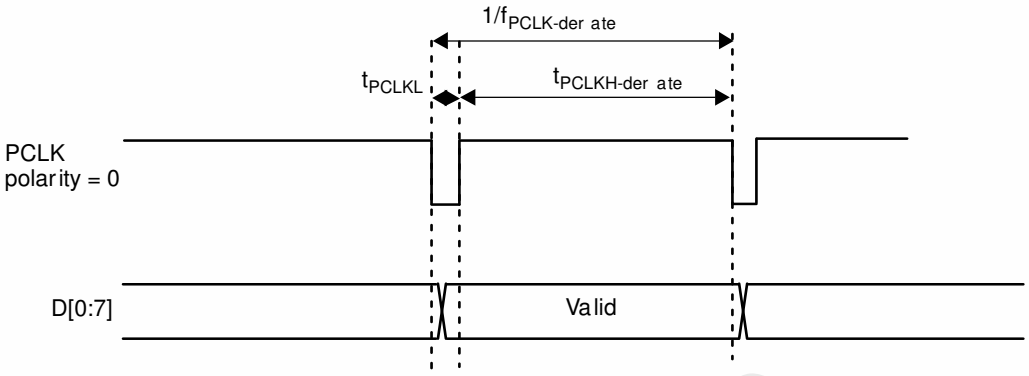


Figure 59 Parallel data output video timing 'n' times derated

Symbol	Description	Min.	Max.	Unit
$f_{PCLK\text{-}derate}$	PCLK frequency derated		f_{PCLK} / n	MHz
$t_{PCLKL\text{-}derate}$	PCLK low width derated	(1/2 * (1/fPCLK)) - 1	(1/2 * (1/fPCLK)) + 1	ns
$t_{PCLKH\text{-}derate}$	PCLK high width	((n-1) * fPCLK) + (1/2 * (1/fPCLK)) - 1	((n-1) * fPCLK) + (1/2 * (1/fPCLK)) + 1	ns

Table 83: Parallel data interface timings 'n' times derated

8.7 CSI Interface : DATA+, DATA-, CLK+, CLK-

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OD}	HS transmit differential voltage[21]	140	200	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
t_r and t_f	20% - 80% rise time and fall time	150		0.3UI[22]	ps

Table 84: CSI interface - DATA+, DATA-, CLK+, CLK- characteristics TBC

Note: *For further information on the sub-LVDS please refer to the specification document: MIPI Alliance Standard for D_PHY*

9 VCM Driver

The HM5065 has a fully integrated VCM driver. An external Voice Coil Motor/Actuator can be connected between VBAT and VCMOUT + VCMOUT (as shown in **Figure 60** VCM Driver circuit diagram). A DAC provides a precise voltage which is buffered by a VCCS controlled by an internal resistor R_{SENSE}.

Note: *The VCM NDRIFT circuit is internal to HM5065 and AF_VDD/VCM+ is not a sensor pin and must be supplied externally.*

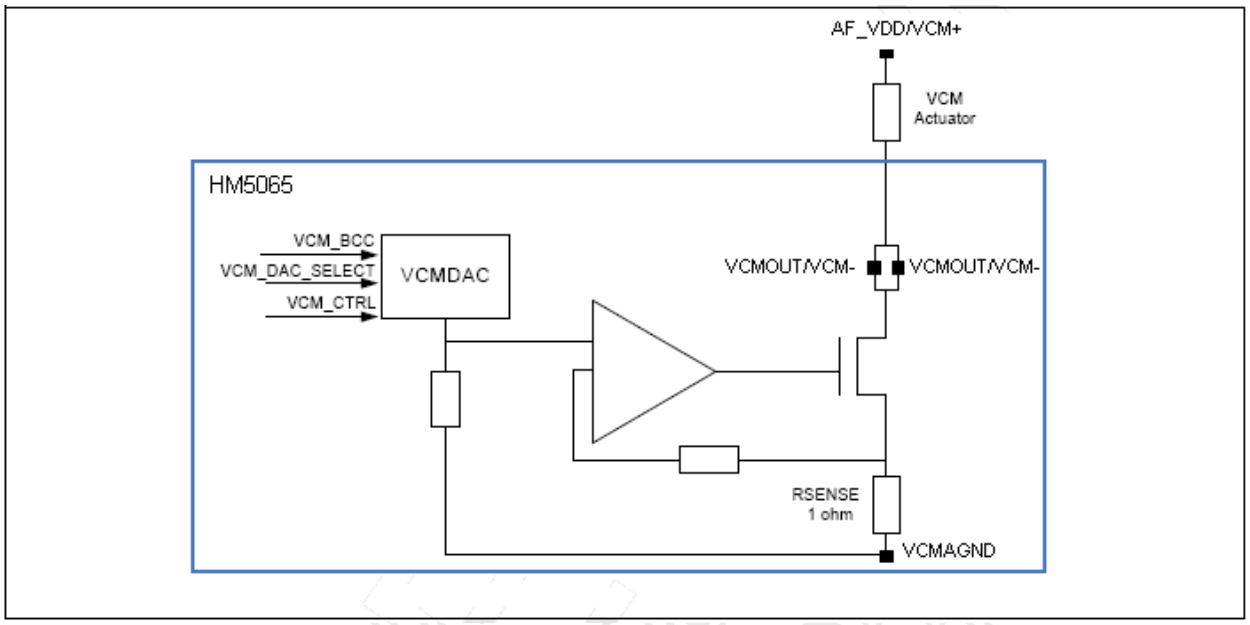


Figure 60 VCM Driver circuit diagram

If this feature is not used, VCMOUT and VCMOUT should be left unconnected. VCMAGND should remain grounded.

During normal sensor operation, the firmware registers dedicated to VCM operation (e.g. manual focus) can be accessed to control the VCM driver. Refer separate Autofocus application note for detail. However, specific low level hardware registers can also be used for debug purposes as described below.

The VCM is enabled by setting **vcm_ctrl** register (0x331e) to 0x3. In order to move the VCM/actuator, set 10bit register **vcm_bcc** (0x332a, 0x332b) to desired value and bit[3] of register **vcm_ctrl** is toggled once for the value to be effective. This can be realized by setting **vcm_ctrl** to 0x3, then 0xB, and then back to 0x3.

Note: *Please note that the acceptable input values are 0 (off) and 127-767.*

The DAC has 6 selectable ramp settings, giving the 6 linear scales shown in Figure 61 Typical VCM current vs. input BCC value. The 3 bit **vcm_dac_select** register (0x331F) allows selection of the desired ramp setting.

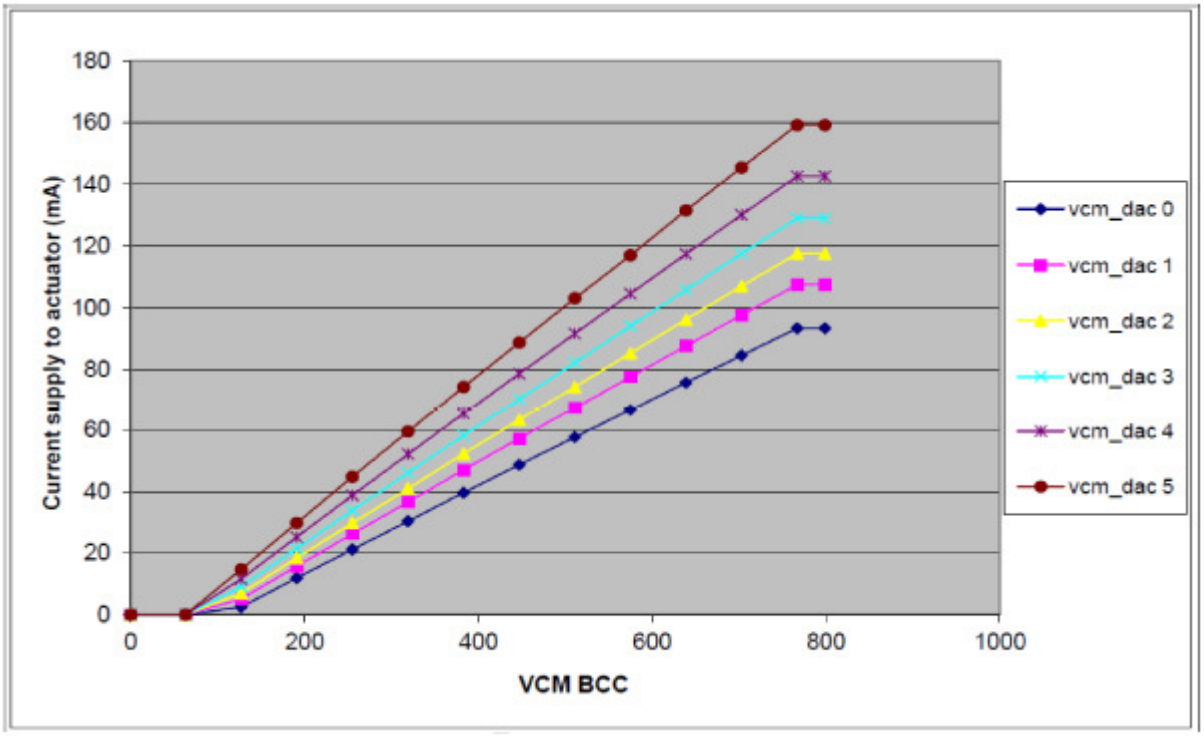


Figure 61 Typical VCM current vs. input BCC value

Note: *The VCM will continue to operate even when the sensor is in Software Standby.*

Parameter	Min.	Typ.	Max.	Unit
Voltage supply to VCM actuator (VBAT)		3	5	V
Relative accuracy (INL)	-1.5		+1.5	LSB
Differential Non-linearity (DNL)	-1		+1	LSB
Active DAC range	127		767	codes
Resolution[23]		0.25		mA/codes
Current range[24]	0	110	160	mA

Table 85 Supply specifications

10 One Time Programmable (OTP) memory

The HM5065 contains 2kbits of non-volatile memory. The purpose of the OTP is to store manufacturing specific data such as serial interface slave address, anti-vignetting parameters, VCM driver operating range, and part-to-part white balance correction.

Please contact Himax Imaging for additional information.

11 Acronyms and abbreviations

Acronym/ abbreviation	Definition
CCI	Camera control interface
CMI	Camera module integrator
CSI	Camera serial interface
DPCM	Differential pulse code modulation
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOF	End of frame
EOT	End of transmission
FE	Frame end
fps	Frames per second
FS	Frame start
HS	High speed; identifier for operation mode
HS-RX	High speed receiver (low-swing differential)
HS-TX	High speed transmitter (low-swing differential)
LE	Line end
LLP	Low level protocol
LS	Line start
LSB	Least significant byte
LP	Low power; identifier for operation mode
LP-RX	Low power receiver (large-swing single ended)
LP-TX	Low power transmitter (large-swing single ended)
LVDS	Low voltage differential signaling
Mbps	Megabits per second
MIPI	Mobile industry processor interface

MSB	Most significant byte
PCK	Pixel clock
PCM	Pulse code modulation
PF	Packet footer
PH	Packet header
PI	Packet identifier
PT	Packet type
PHY	Physical layer
PLL	Phase locked loop
RO	Read only
RW	Read/write
SCL	Serial clock (for CCI)
SDA	Serial data (for CCI)
SMIA	Standard mobile imaging architecture
SOT	Start of transmission
SOF	Start of frame
SSCG	Spread spectrum clock generator
SubLVDS	Sub-low voltage differential signaling
WDR	Wide dynamic reconstruct
ULPM	Ultra low power mode

Table 86: Acronyms and abbreviations

12 Chief ray angle (CRA)

Field (%)	Image height (mm)	CRA (degrees)
0	0.000	0.00
10	0.228	4.25
20	0.457	8.38
30	0.685	12.34
40	0.913	16.02
50	1.142	19.31
60	1.370	22.10
70	1.599	24.23
80	1.827	25.48
90	2.055	25.63
100	2.284	24.60

Table 87: Chief ray angle (CRA)

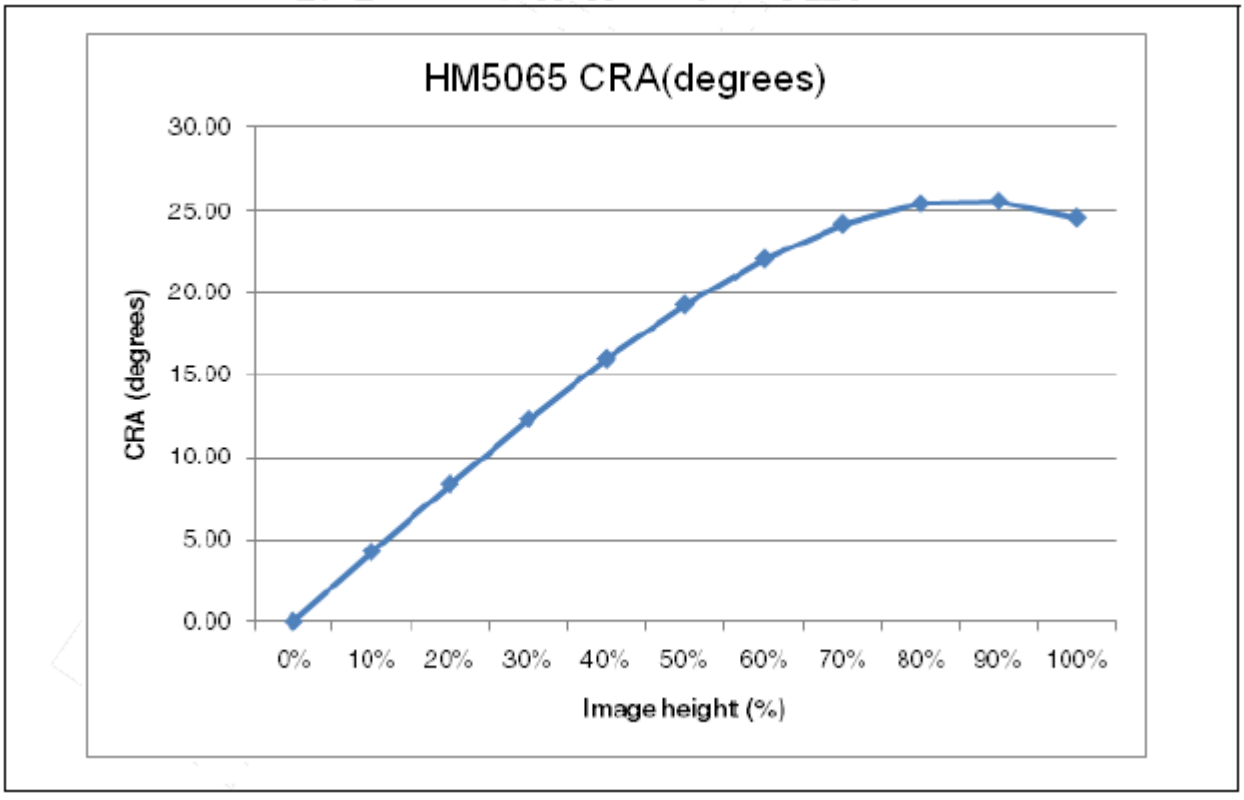


Figure 62 HM5065 chief ray angle (CRA)

The CRA characteristics of the lens should be within +/- 1 degree to ensure color accuracy and minimize noise and mosaic artifacts. The CRA curve is adapted to typical camera modules with low Z height, using typical 4P lens for mass production.

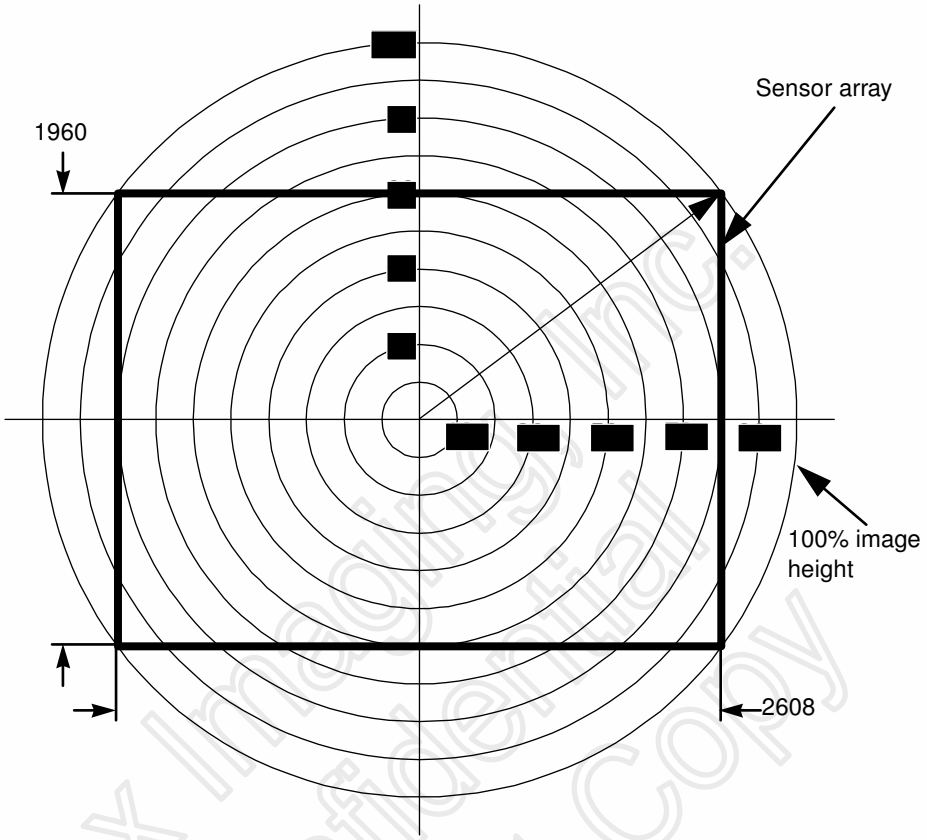


Figure 63 HM5065 sensor array and image height

Note: *Half the diagonal distance of the active sensor array (2608 x 1960) is 2.284 mm.*

13 Revision History

Release Version	Date	Status	Description
Rev 01	2012 / 03 / 01	Preliminary	Initial Document
Rev 02	2012 / 05 / 2	Preliminary	Add PLCC package information
Rev 03	2012 / 06 / 6	Preliminary	Add Data format and order information

14 Disclaimer

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