

# HM5118165A/AL Series

## 1,048,576-word × 16-bit Dynamic Random Access Memory

# HITACHI

Preliminary  
Rev. 0.0  
Mar. 20, 1995

The Hitachi HM5118165A/AL is a CMOS dynamic RAM organized 1,048,576-word × 16-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5118165A/AL offers Extended Data Out (EDO) Page Mode as a high speed access mode.

### Feature

- Single 5.0 V ( $\pm 10\%$ )
- High speed
  - Access time  
70 ns/ 80 ns (max)
- Low power dissipation
  - Active mode  
825 mW/715 mW (max)
  - Standby mode 11 mW (max)  
0.83 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
  - 1024 refresh cycles : 16 ms  
:128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)
- 2 $\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)

### Ordering Information

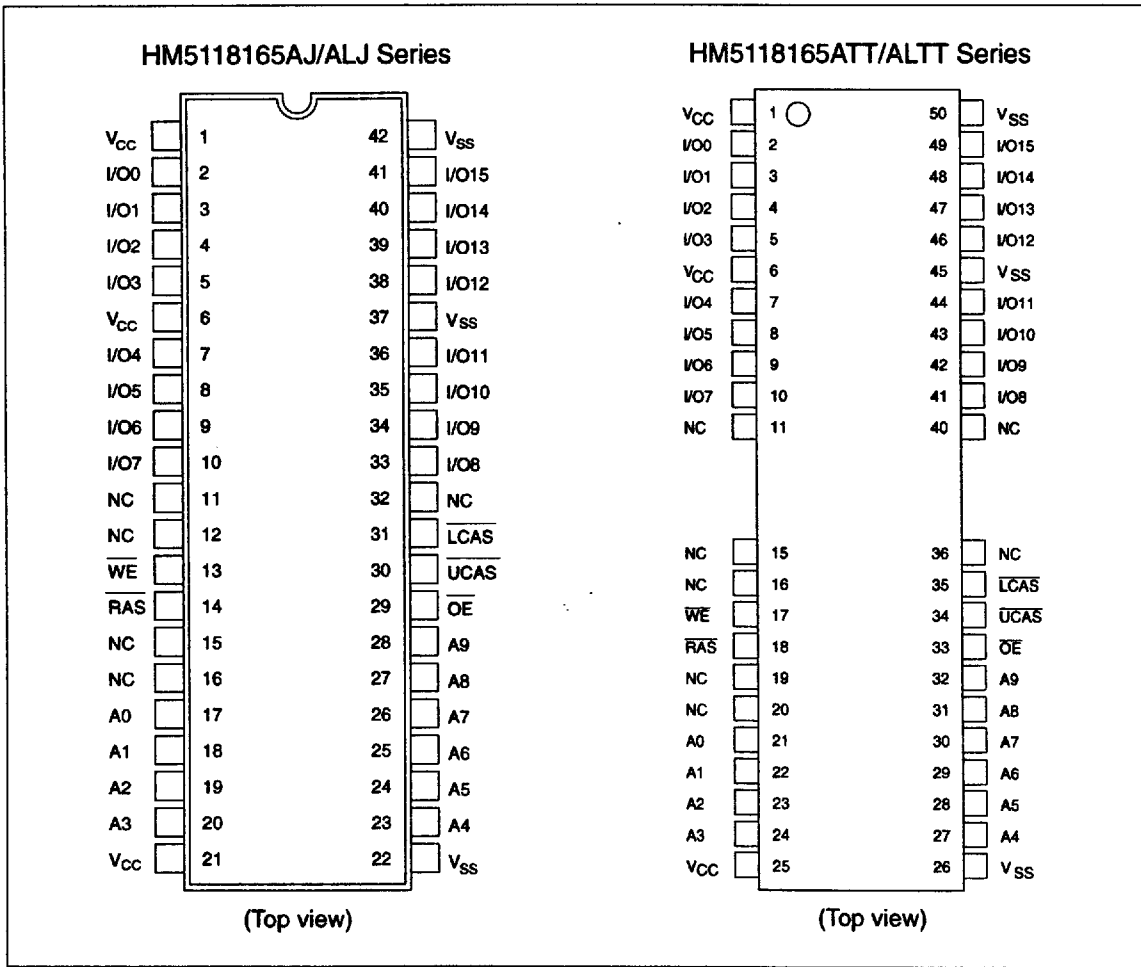
Type No.	Access time	Package
HM5118165AJ-7	70 ns	400-mil, 42-pin plastic SOJ (CP-42D)
HM5118165AJ-8	80 ns	
HM5118165ALJ-7	70 ns	400-mil, 50-pin plastic TSOP II (TTP-50/44DC)
HM5118165ALJ-8	80 ns	
HM5118165ATT-7	70 ns	400-mil, 50-pin plastic TSOP II (TTP-50/44DC)
HM5118165ATT-8	80 ns	
HM5118165ALTT-7	70 ns	400-mil, 50-pin plastic TSOP II (TTP-50/44DC)
HM5118165ALTT-8	80 ns	

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

RAS

Row address strobe



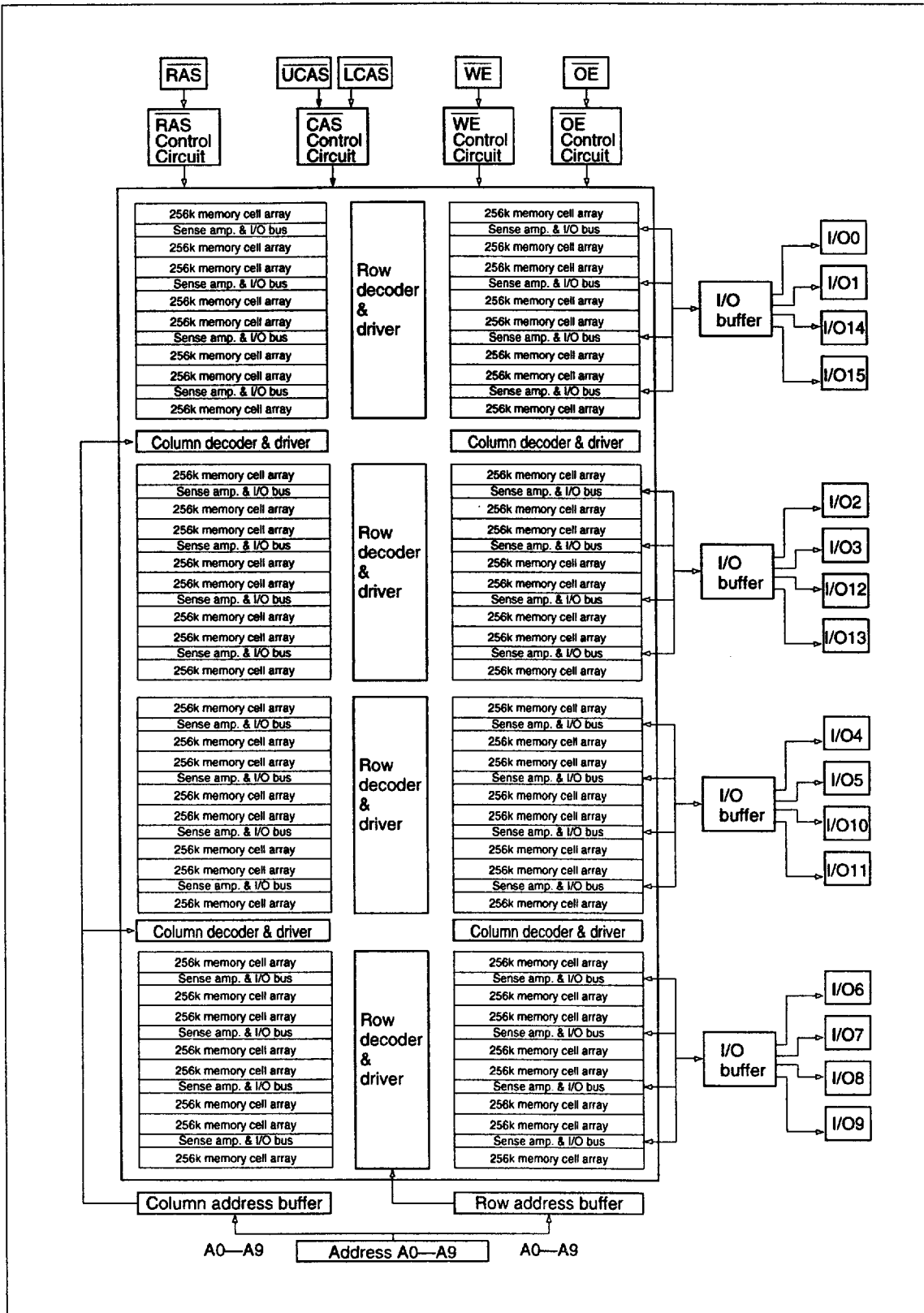
UCAS, LCAS	Column address strobe
WE	Read/Write enable
OE	Output enable

**Pin Arrangement**

**Pin Description**

Pin name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O0 to I/O15	Data input/data output

Pin name	Function
VCC	Power supply (+ 5.0 V)
VSS	Ground
NC	No connection



## Truth Table

Inputs					I/O		Operation	Notes
RAS	LCAS	UCAS	WE	OE	I/O0 - I/O7	I/O8 - I/O15		
H	H	H	H	H	High-Z	High-Z	Standby	1, 3
L	H	H	H	H	High-Z	High-Z	Refresh	1, 3
L	L	H	H	L	Dout	High-Z	Lower byte read	1, 3
L	H	L	H	L	High-Z	Dout	Upper byte read	1, 3
L	L	L	H	L	Dout	Dout	Word read	1, 3
L	L	H	L	H	Din	Don't care	Lower byte write	1, 2, 3
L	H	L	L	H	Don't care	Din	Upper byte write	1, 2, 3
L	L	L	L	H	Din	Din	Word write	1, 2, 3
L	L	L	H	H	High-Z	High-Z		1, 3
H to L	L	H	-	-	High-Z	High-Z	CBR refresh	1, 3
H to L	H	L	-	-	High-Z	High-Z	or Self refresh	
H to L	L	L	-	-	High-Z	High-Z		

Notes: 1. H: High(inactive) L: Low(active)

2.  $t_{WCS} \geq 0$  ns Early write cycle  
 $t_{WCS} < 0$  ns Delayed write cycle

3. Mode is determined by the OR function of the  $\overline{UCAS}$  and  $\overline{LCAS}$ . (Mode is set by the earliest of  $\overline{UCAS}$  and  $\overline{LCAS}$  active edge and reset by the latest of  $\overline{UCAS}$  and  $\overline{LCAS}$  inactive edge.)  
 However write OPERATION and output HIZ control are done independently by each  $\overline{UCAS}$ ,  $\overline{LCAS}$ .

ex. if  $\overline{RAS} = H$  to L,  $\overline{LCAS} = L$ ,  $\overline{UCAS} = H$ , then  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle is selected.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

**Recommended DC Operating Conditions (Ta = 0 to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Input high voltage	V <sub>IH</sub>	2.4	—	6.5	V	1
Input low voltage	V <sub>IL</sub>	-1.0	—	0.8	V	1

Note : 1. All voltage referred to V<sub>SS</sub>

**DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0 V)**

		HM5118165A/AL						
		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test condition	Notes
Operating current	I <sub>CC1</sub>	—	150	—	130	mA	t <sub>RC</sub> = min	1, 2
Standby current	I <sub>CC2</sub>	—	2	—	2	mA	TTL interface R <sub>AS</sub> , U <sub>CAS</sub> , L <sub>CAS</sub> = V <sub>IH</sub> , Dout = High-Z	
		—	1	—	1	mA	CMOS interface R <sub>AS</sub> , U <sub>CAS</sub> , L <sub>CAS</sub> ≥ V <sub>CC</sub> - 0.2V Dout = High-Z	
Standby current (L-version)		—	0.15	—	0.15	mA	CMOS interface R <sub>AS</sub> , U <sub>CAS</sub> , L <sub>CAS</sub> ≥ V <sub>CC</sub> - 0.2V Dout = High-Z	
R <sub>AS</sub> -only refresh current	I <sub>CC3</sub>	—	150	—	130	mA	t <sub>RC</sub> = min	2
Standby current	I <sub>CC5</sub>	—	5	—	5	mA	R <sub>AS</sub> = V <sub>IH</sub> U <sub>CAS</sub> , L <sub>CAS</sub> = V <sub>IL</sub> Dout = enable	1
C <sub>AS</sub> -before-R <sub>AS</sub> refresh current	I <sub>CC6</sub>	—	150	—	130	mA	t <sub>RC</sub> = min	
EDO page mode current	I <sub>CC7</sub>	—	165	—	150	mA	t <sub>HPC</sub> = min	1,3
Battery back up operating current (Stand by with CBR refresh) (L-version)	I <sub>CC10</sub>	—	0.5	—	0.5	mA	CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 125 μs t <sub>RAS</sub> ≤ 0.3 μs	

DC Characteristics (cont.)

Parameter	Symbol	HM5118165A/AL				Unit	Test condition	Notes
		-7		-8				
		Min	Max	Min	Max			
Self refresh mode current (L-version)	$I_{CC11}$	—	300	—	300	$\mu A$	CMOS interface $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS} \leq 0.2V$ Dout = High-Z	
Input leakage current	$I_{LI}$	-10	10	-10	10	$\mu A$	$0V \leq V_{in} \leq 7V$	
Output leakage current Dout = disable	$I_{LO}$	-10	10	-10	10	$\mu A$	$0V \leq V_{out} \leq 7V$	
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -2 mA	
Output low voltage	$V_{OL}$	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes : 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.  
 2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .  
 3. Address can be changed once or less while  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$

Capacitance ( $T_a = 25^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I1}$	—	5	pF	1
Input capacitance (Clocks)	$C_{I2}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

- Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$  to disable Dout.

AC Characteristics ( $T_a = 0$  to  $+70^\circ C$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ) \*1, \*2, \*3, \*19

Test Conditions

- Input rise and fall time: 2 ns
- Input levels:  $V_{IL} = 0V$ ,  $V_{IH} = 3.0V$
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output Load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM5118165A/AL				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	124	—	144	—	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	50	—	60	—	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	13	—	15	—	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	13	10000	15	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	13	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	45	20	53	ns	4
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	35	15	40	ns	5
$\overline{RAS}$ hold time	$t_{RSH}$	18	—	20	—	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	58	—	68	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	$t_{OED}$	18	—	20	—	ns	6
$\overline{OE}$ delay time from Din	$t_{DZO}$	0	—	0	—	ns	7
$\overline{CAS}$ delay time from Din	$t_{DZC}$	0	—	0	—	ns	7
Transition time (rise and fall)	$t_T$	2	50	2	50	ns	8

## Read Cycle

Parameter	Symbol	HM5118165A/AL				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	70	—	80	ns	9, 10
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	18	—	20	ns	10, 11, 18
Access time from address	$t_{\text{AA}}$	—	35	—	40	ns	10, 12, 18
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	18	—	20	ns	10
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	5	—	5	—	ns	13
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	70	—	80	—	ns	
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	ns	13
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	23	—	28	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	ns	14
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	—	15	ns	14
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	18	—	20	—	ns	6
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	3	—	3	—	ns	
Output buffer turn-off time to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	15	—	15	ns	
Output buffer turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WED}}$	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	18	—	20	—	ns	



## Write Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{WCS}$	0	—	0	—	ns	15
Write command hold time	$t_{WCH}$	13	—	15	—	ns	
Write command pulse width	$t_{WP}$	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	13	—	15	—	ns	
Data-in setup time	$t_{DS}$	0	—	0	—	ns	16
Data-in hold time	$t_{DH}$	13	—	15	—	ns	16

## Read-Modify-Write Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	175	—	199	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	95	—	107	—	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	43	—	47	—	ns	15
Column address to $\overline{WE}$ delay time	$t_{AWD}$	60	—	67	—	ns	15
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEh}$	18	—	20	—	ns	

## Refresh Cycle

Parameter	Symbol	HM5118165A/AL				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	$t_{\text{CSR}}$	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	$t_{\text{CHR}}$	10	—	10	—	ns	
$\overline{\text{WE}}$ setup time (CBR refresh cycle)	$t_{\text{WRP}}$	0	—	0	—	ns	
$\overline{\text{WE}}$ hold time (CBR refresh cycle)	$t_{\text{WRH}}$	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	$t_{\text{RPC}}$	0	—	0	—	ns	

## EDO Page Mode Cycle

Parameter	Symbol	HM5118165A/AL				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
EDO page mode cycle time	$t_{\text{HPC}}$	30	—	35	—	ns	26
EDO page mode $\overline{\text{RAS}}$ pulse width	$t_{\text{RASP}}$	—	100000	—	100000	ns	17
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPA}}$	—	40	—	45	ns	10, 18
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPRH}}$	40	—	45	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	$t_{\text{DOH}}$	5	—	5	—	ns	10, 18
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	$t_{\text{COL}}$	13	—	15	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	$t_{\text{COP}}$	5	—	5	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	$t_{\text{RCHC}}$	40	—	45	—	ns	

**EDO Page Mode Read-Modify-Write Cycle**

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	$t_{HPRWC}$	90	—	99	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	62	—	69	—	ns	15

**Refresh**

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	16	ms	1024 cycles

**Self-Refresh Mode**

		HM5118165AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	$t_{RASS}$	100	—	100	—	$\mu$ s	
$\overline{RAS}$ precharge time (self refresh)	$t_{RPS}$	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	$t_{CHS}$	-50	—	-50	—	ns	

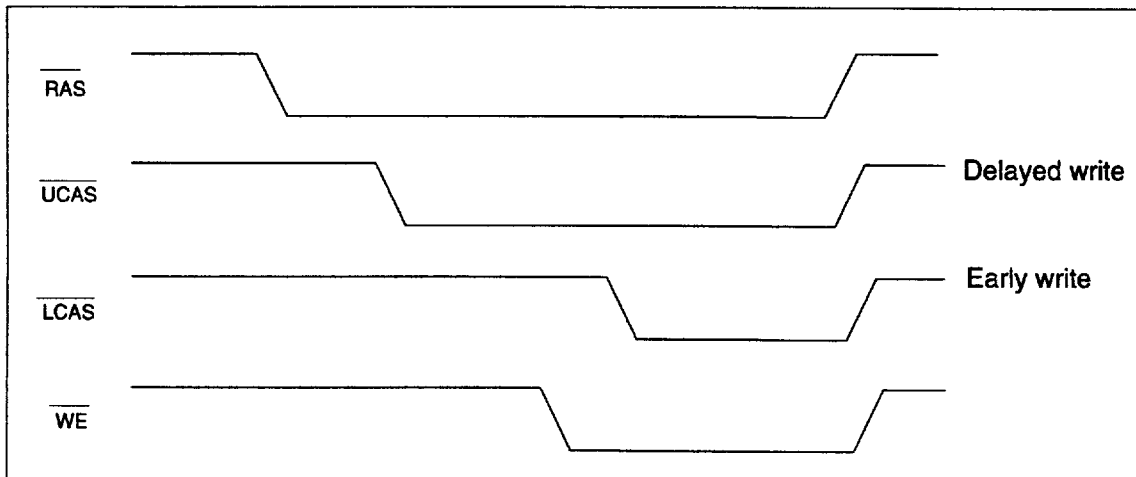
- Notes:
1. AC measurements assume  $t_T = 2$  ns.
  2. An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh).
  3. Only row address is indispensable on address A8, A9.
  4. Operation with the  $t_{\text{RCD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RCD}}$  (max) is specified as a reference point only; if  $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$ , then access time is controlled exclusively by  $t_{\text{CAC}}$ .
  5. Operation with the  $t_{\text{RAD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RAD}}$  (max) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
  6. Either  $t_{\text{OED}}$  or  $t_{\text{CDD}}$  must be satisfied.
  7. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
  8.  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  9. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
  10. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  11. Assumes that  $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$ .
  12. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ .
  13. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
  14.  $t_{\text{OFF}} (\text{max})$  and  $t_{\text{OEZ}} (\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  15.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ , or  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  16. These parameters are referred to  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
  17.  $t_{\text{RASP}}$  defines RAS pulse width in EDO page mode cycles.
  18. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{CPA}}$ .
  19. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the I/O pin will remain open circuit (high impedance); if  $t_{\text{OEH}} \leq t_{\text{CWL}}$ , invalid data will be out at each I/O.
  20. When both  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  go low at the same time, all 16-bits data are written into the device.  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  cannot be staggered within the same write/read cycles.
  21. All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
  22.  $t_{\text{ASC}}$ ,  $t_{\text{CAH}}$ ,  $t_{\text{RCS}}$ ,  $t_{\text{RCH}}$ ,  $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{CSR}}$  and  $t_{\text{RPC}}$  are determined by the earlier falling edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  23.  $t_{\text{CRP}}$ ,  $t_{\text{CHR}}$ ,  $t_{\text{ACP}}$  and  $t_{\text{CPW}}$  are determined by the later rising edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  24.  $t_{\text{CWL}}$ ,  $t_{\text{DH}}$ ,  $t_{\text{DS}}$  and  $t_{\text{CHS}}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  25.  $t_{\text{CPN}}$  and  $t_{\text{CP}}$  are determined by the time that both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.
  26.  $t_{\text{HPC}} (\text{min})$  can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of CAS cycle ( $t_{\text{CAS}} + t_{\text{CP}} + 2t_T$ ) becomes greater than the specified  $t_{\text{HPC}} (\text{min})$  value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
  27. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{\text{CC}}/V_{\text{SS}}$  line noise, which causes to degrade  $V_{\text{IH}} \text{ min}/V_{\text{IL}} \text{ max}$  level.
  28. Please do not use  $t_{\text{RASS}}$  timing,  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{\text{RASS}} \geq 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .

29. If you use distributed CBR refresh mode with 15.6  $\mu$ s interval in normal read/write cycle, CBR refresh should be executed within 15.6  $\mu$ s immediately after exiting from and before entering into self refresh mode.
30. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6  $\mu$ s interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
31. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

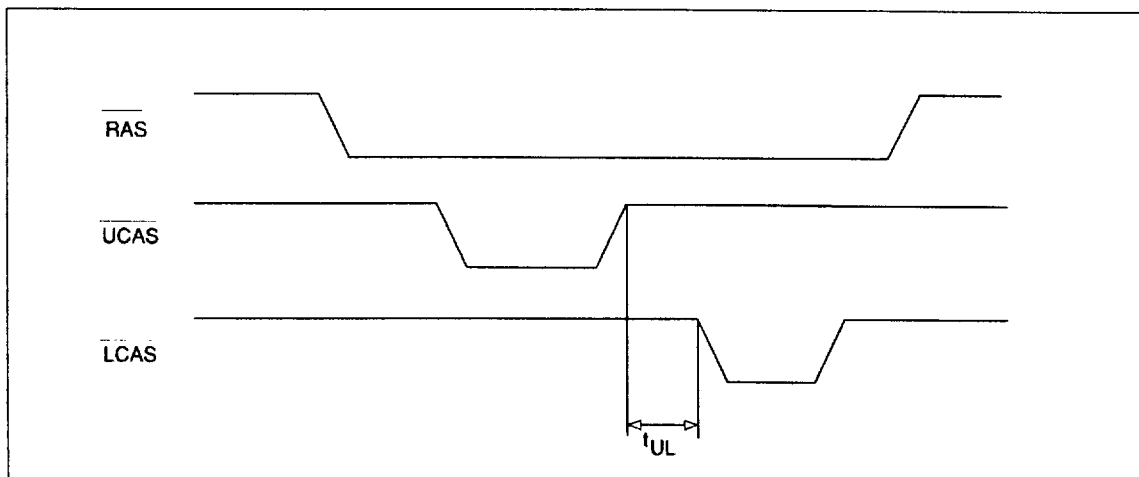
Notes concerning  $2\overline{\text{CAS}}$  control

Please do not separate the  $\overline{\text{UCAS/LCAS}}$  operation timing intentionally. However skew between  $\overline{\text{UCAS/LCAS}}$  are allowed under the following conditions.

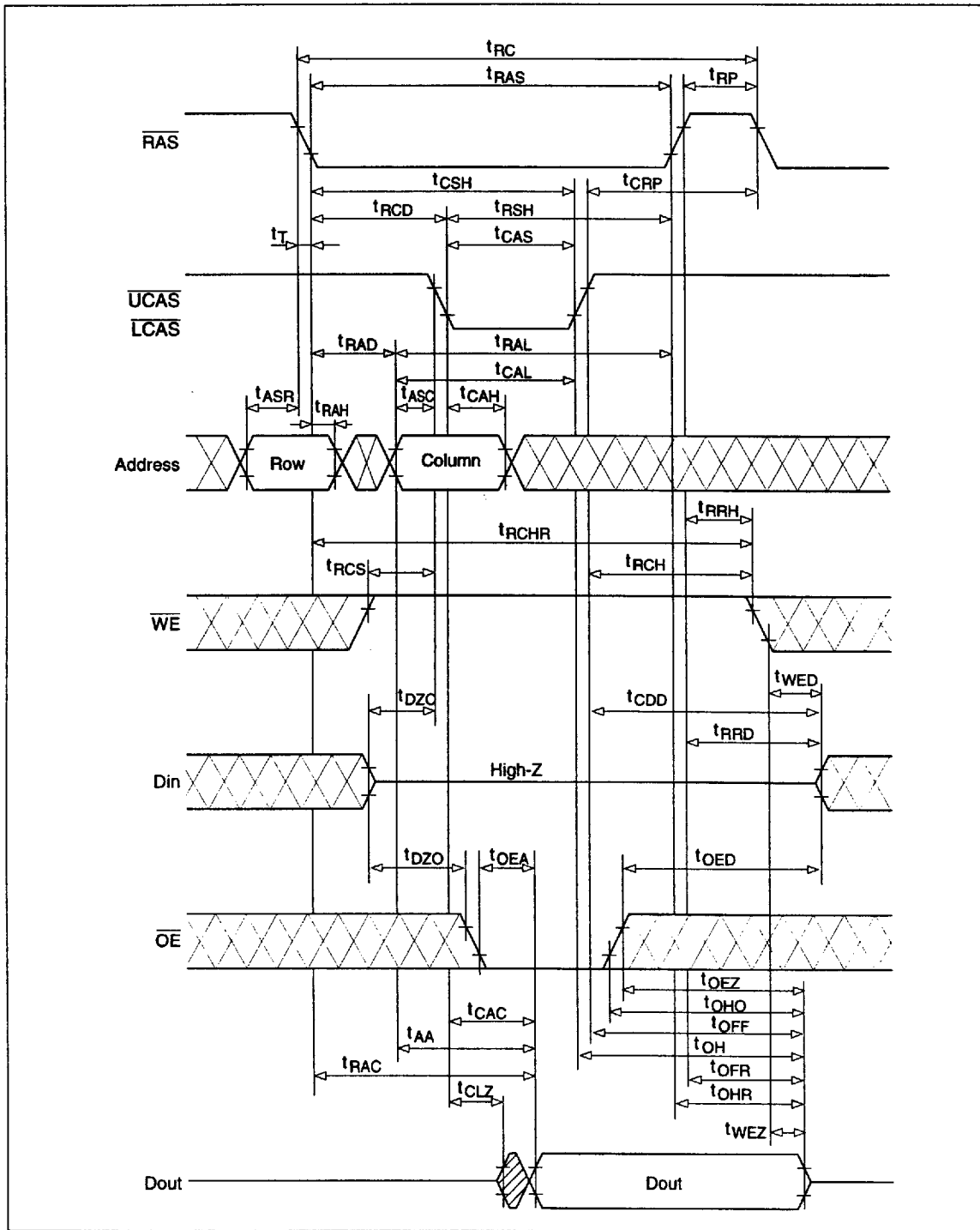
- (1) Each of the  $\overline{\text{UCAS/LCAS}}$  should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.




- (3) Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{\text{CP}} \leq t_{\text{UL}}$ ) is satisfied, EDO page mode can be performed.



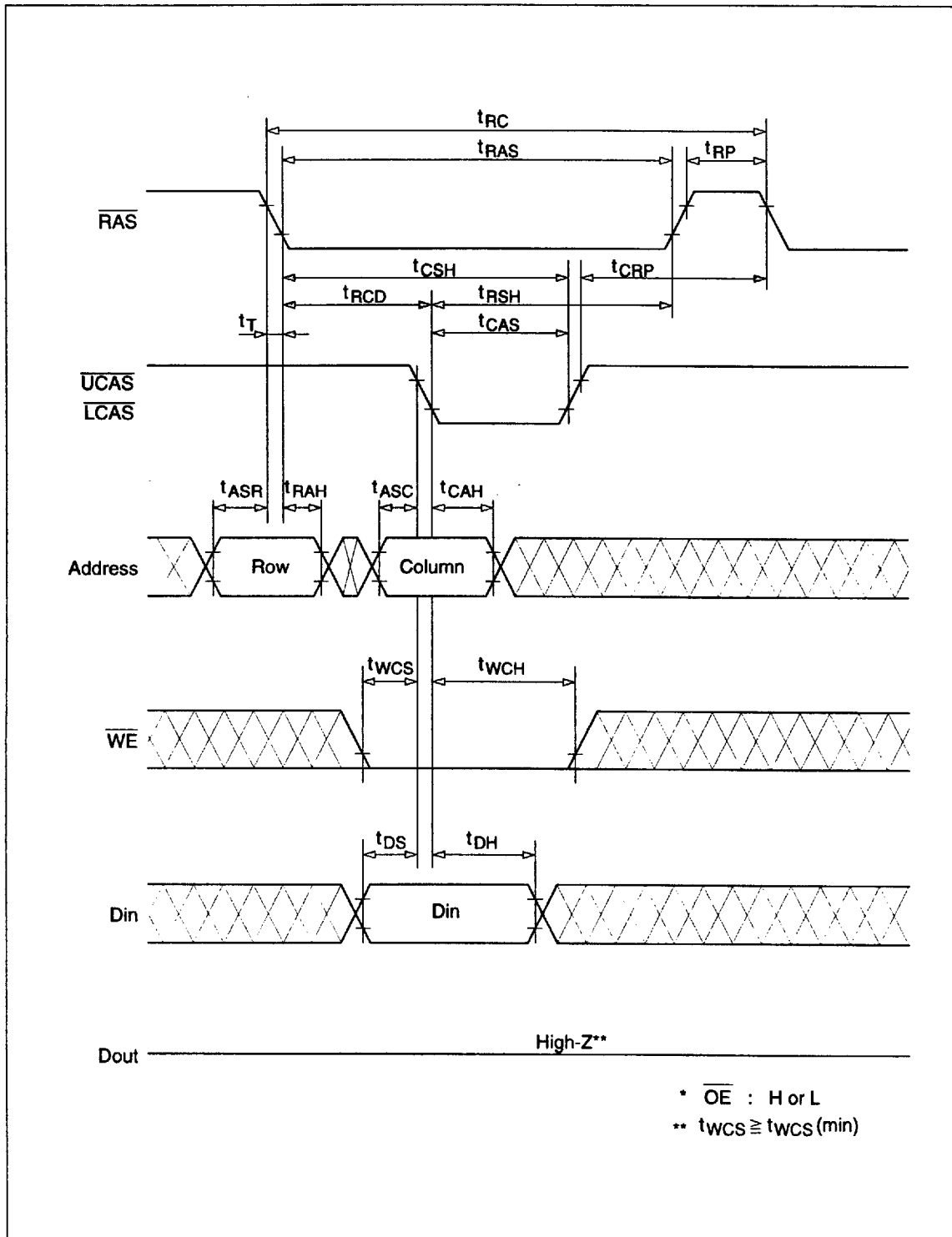
Timing Waveforms\*32  
Read Cycle



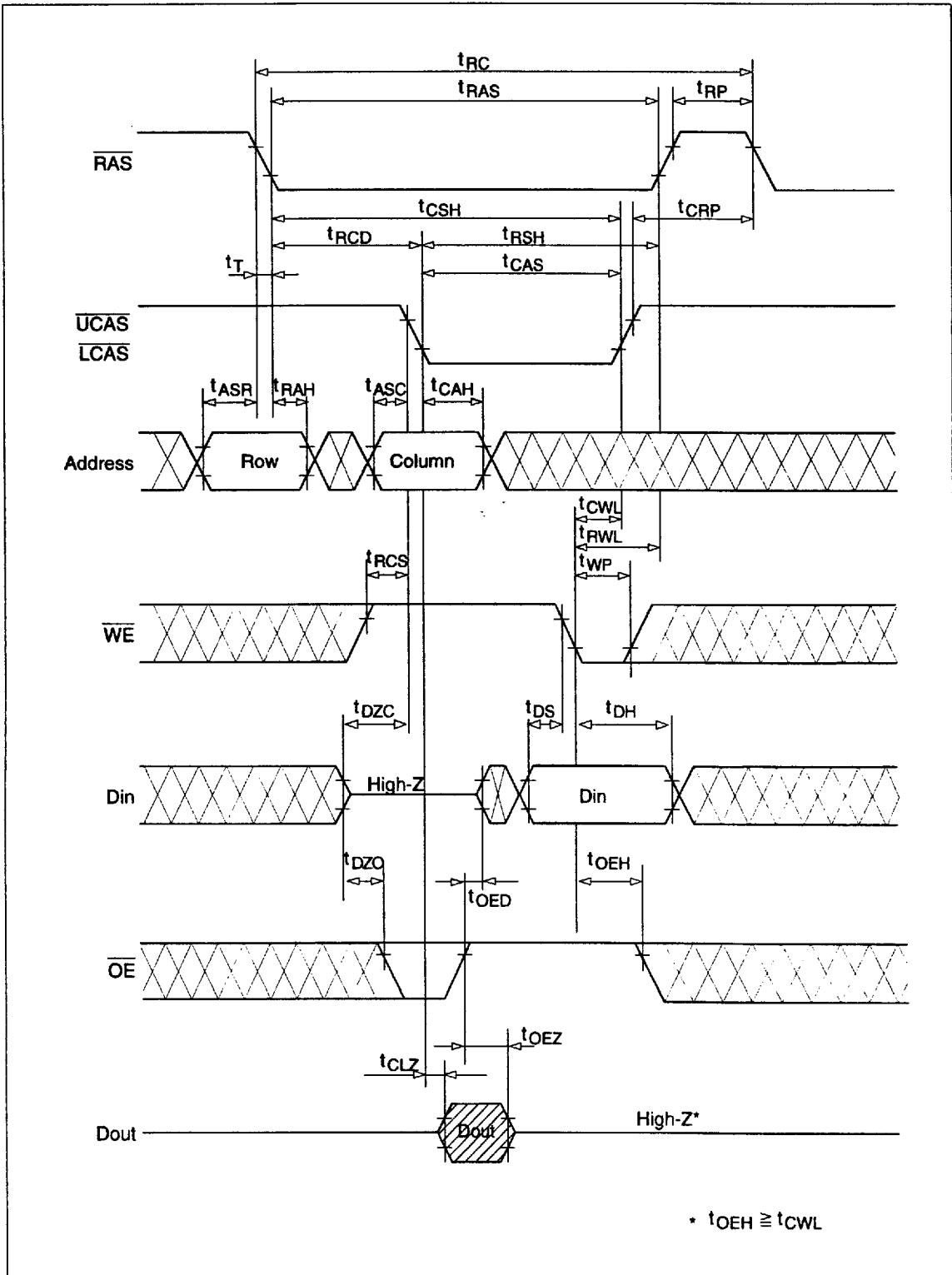
Note 32:  H or L (H:  $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ , L:  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$ )

 Invalid Dout

Early Write Cycle

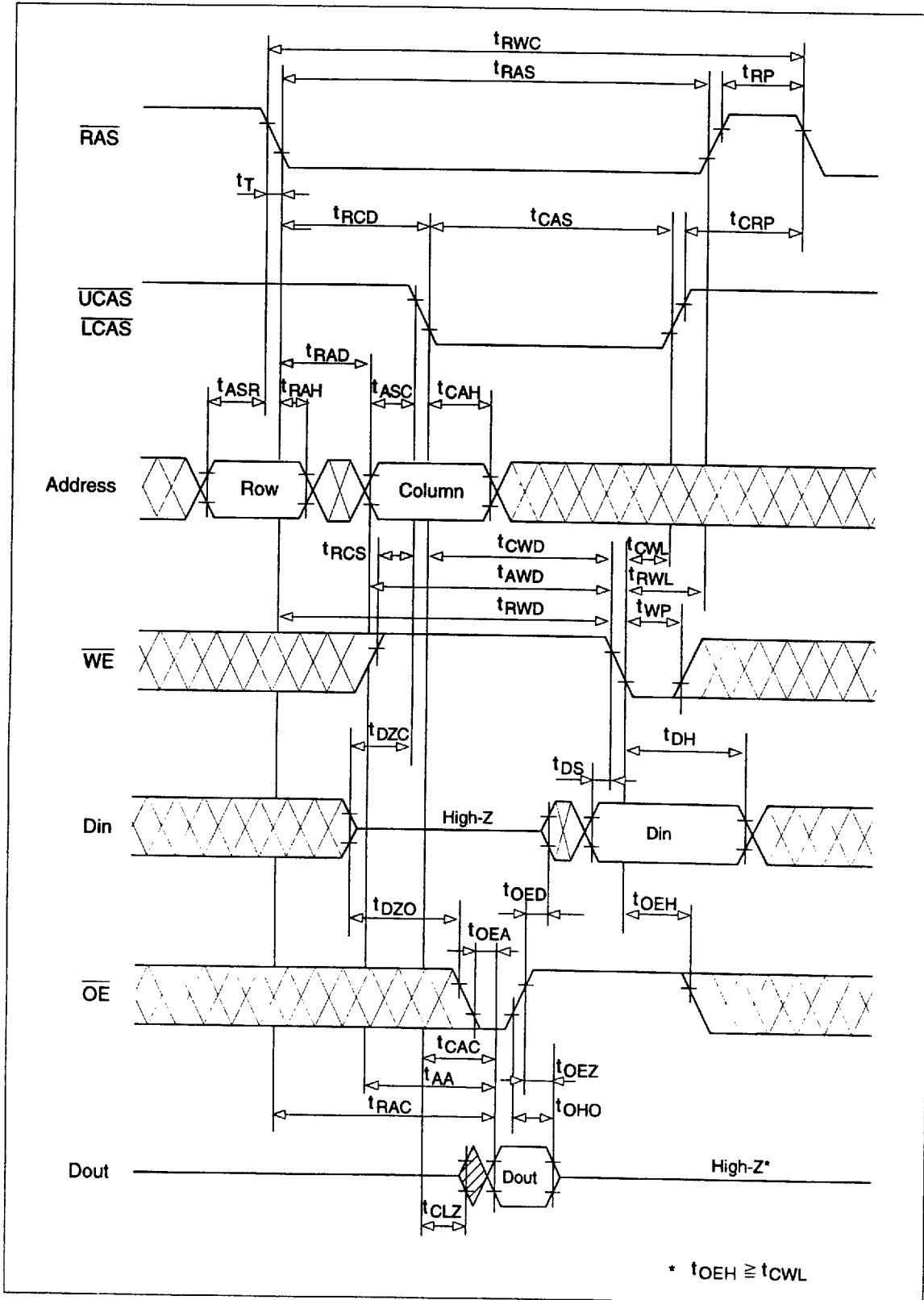


Delayed Write Cycle \*19



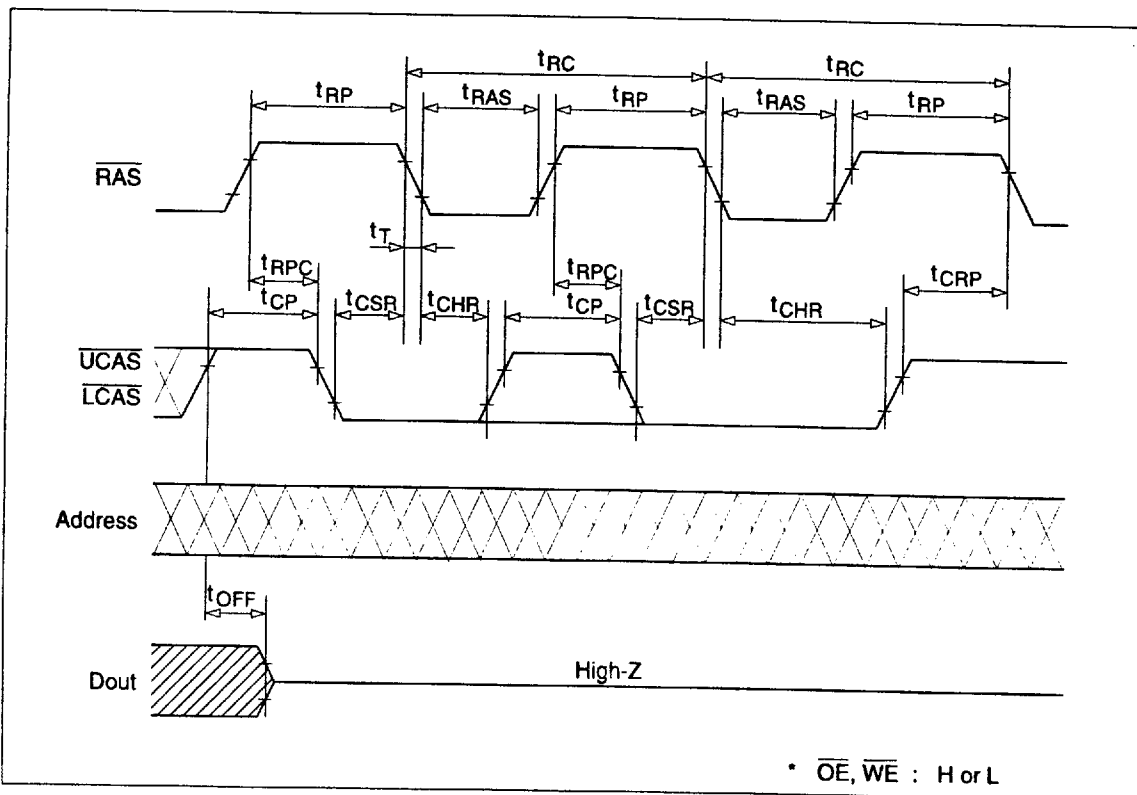
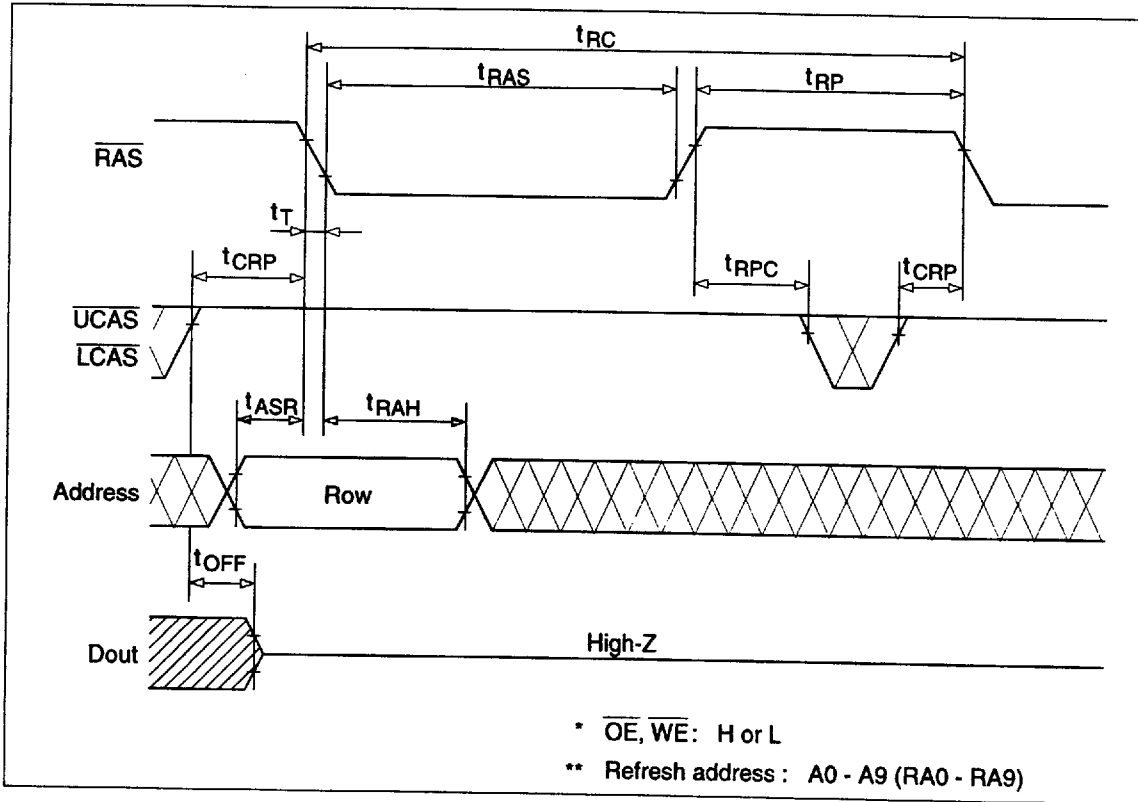


Read-Modify-Write Cycle \*19

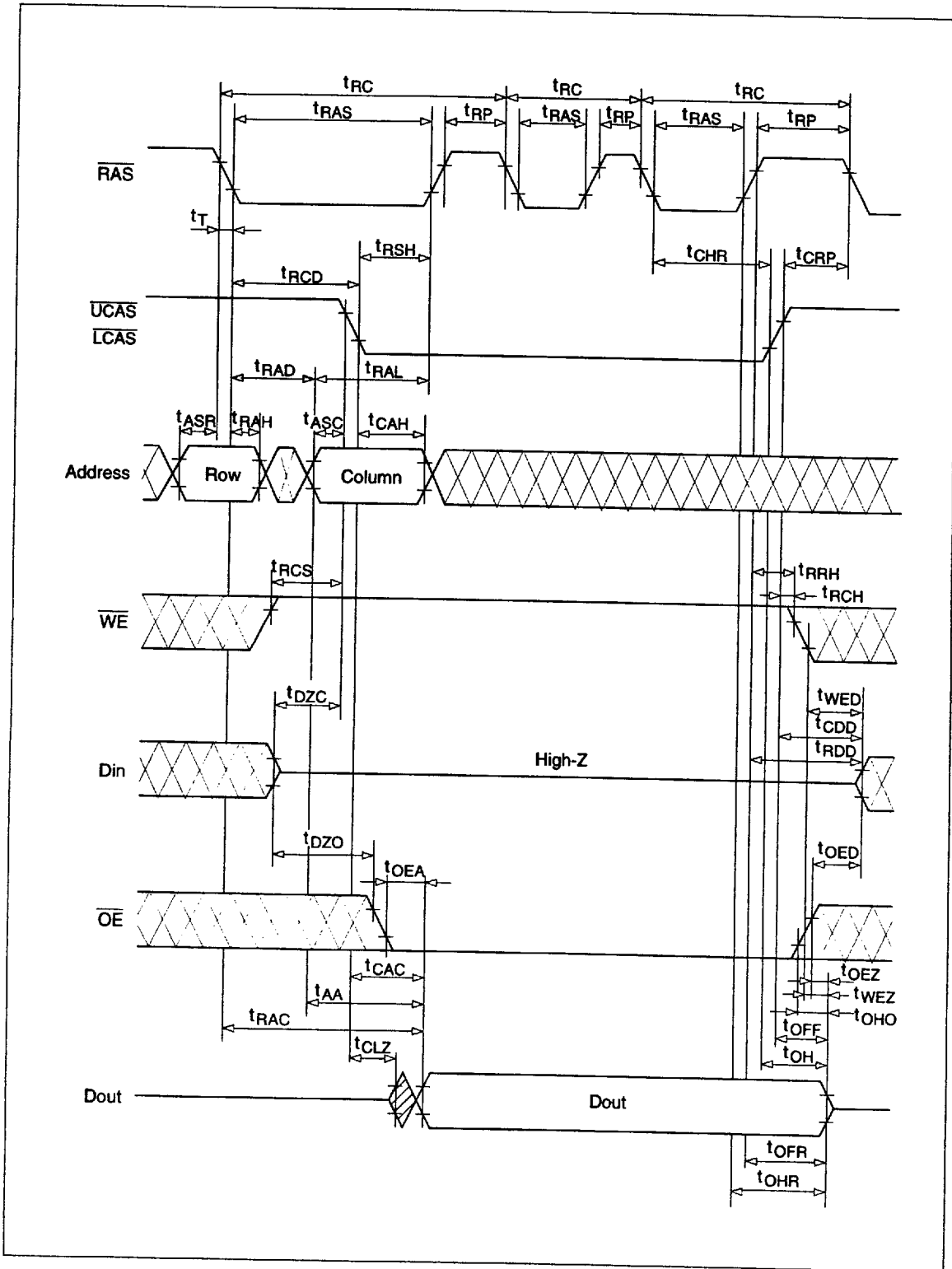


RAS-Only Refresh Cycle

CAS-Before-RAS Refresh Cycle



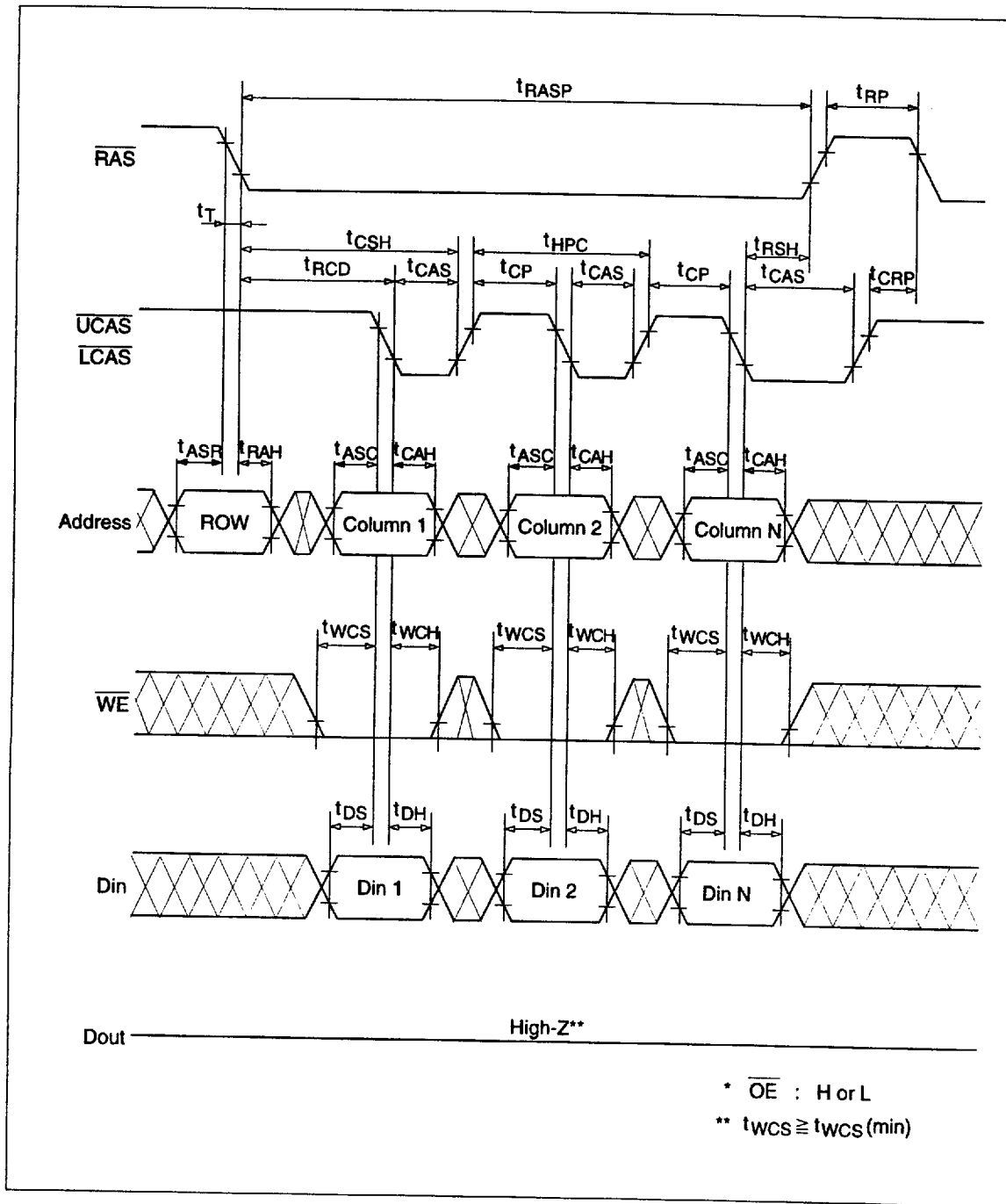
Hidden Refresh Cycle



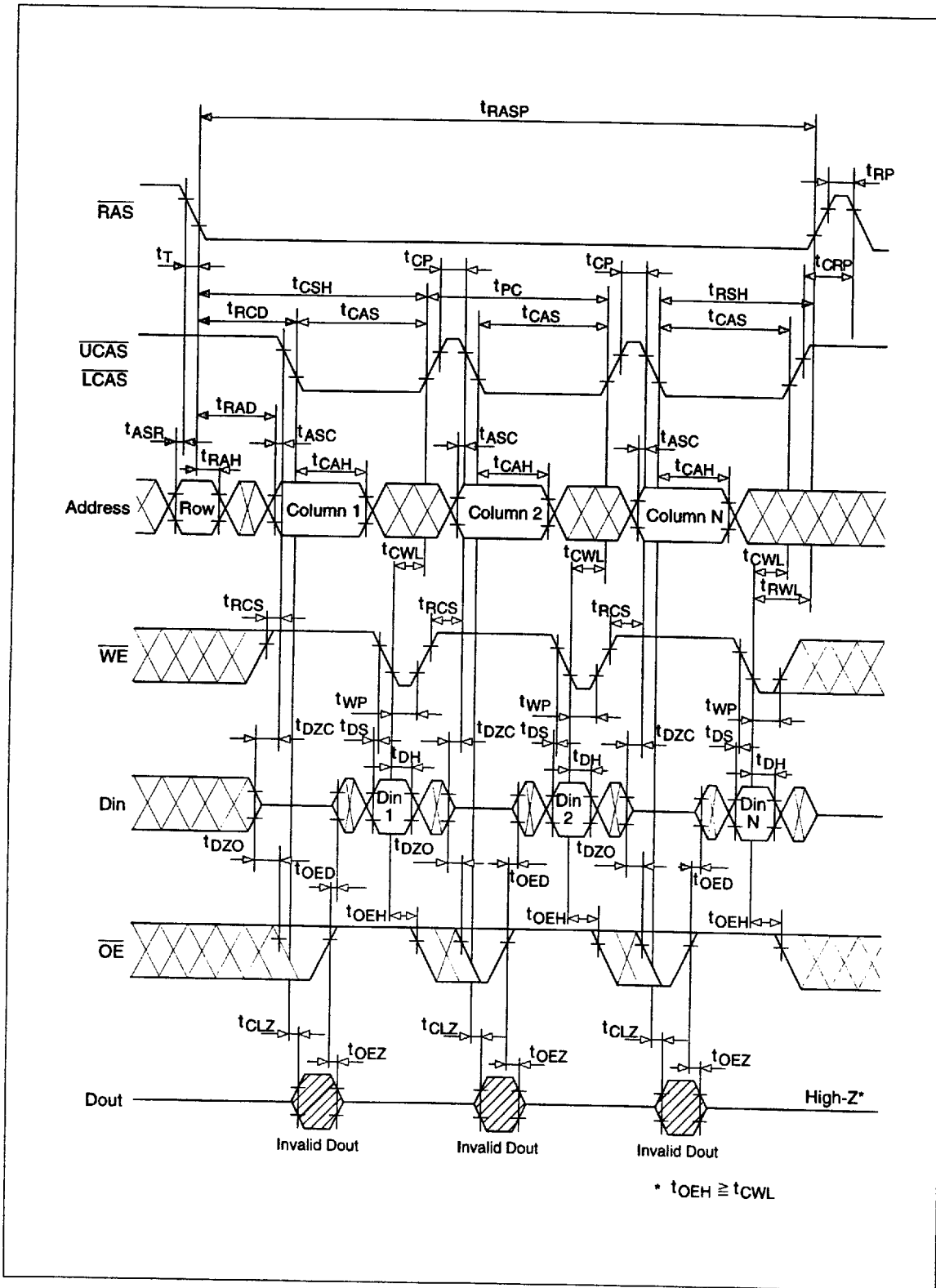




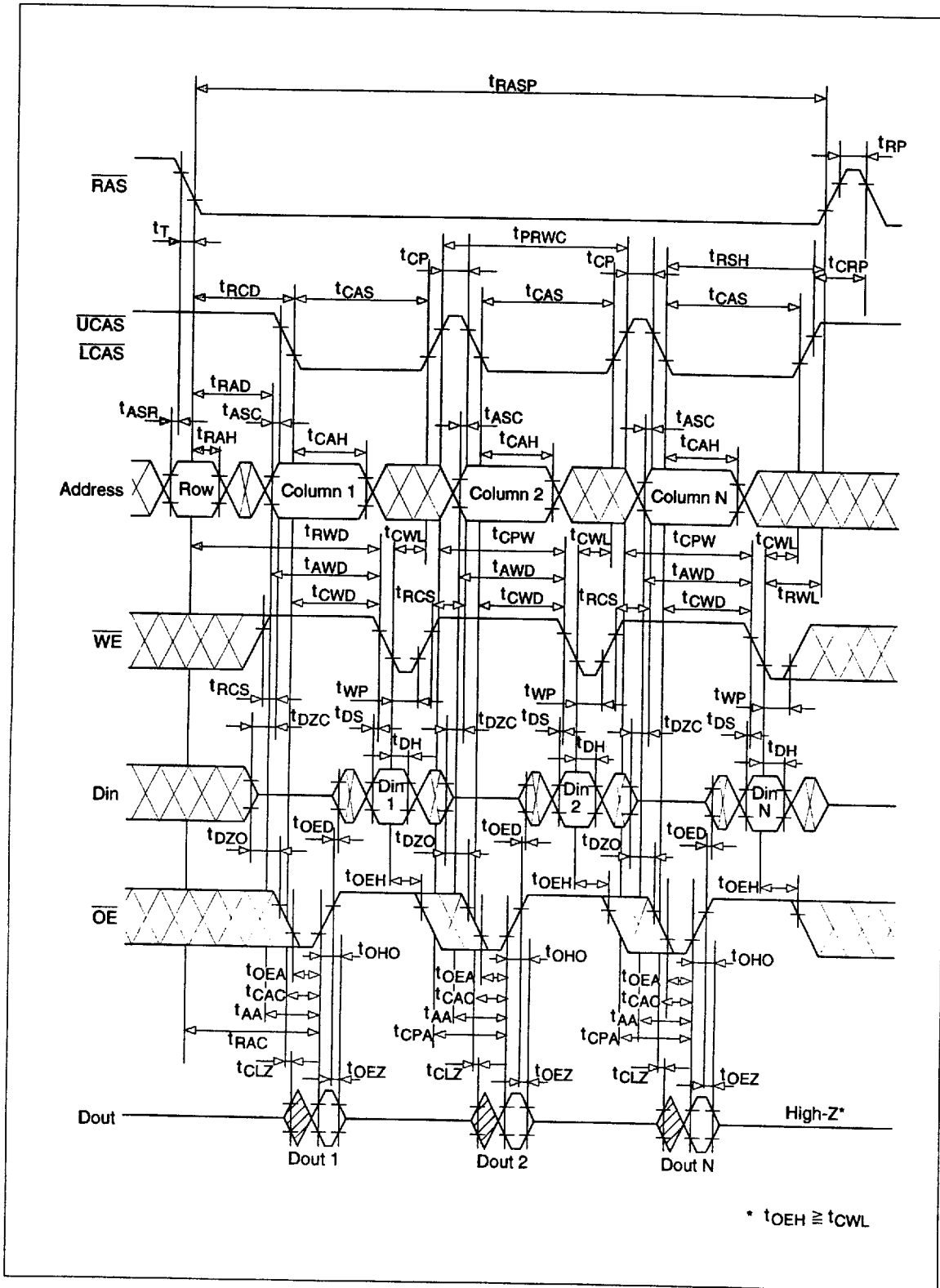
EDO Page Mode Early Write Cycle



EDO Page Mode Delayed Write Cycle \*19

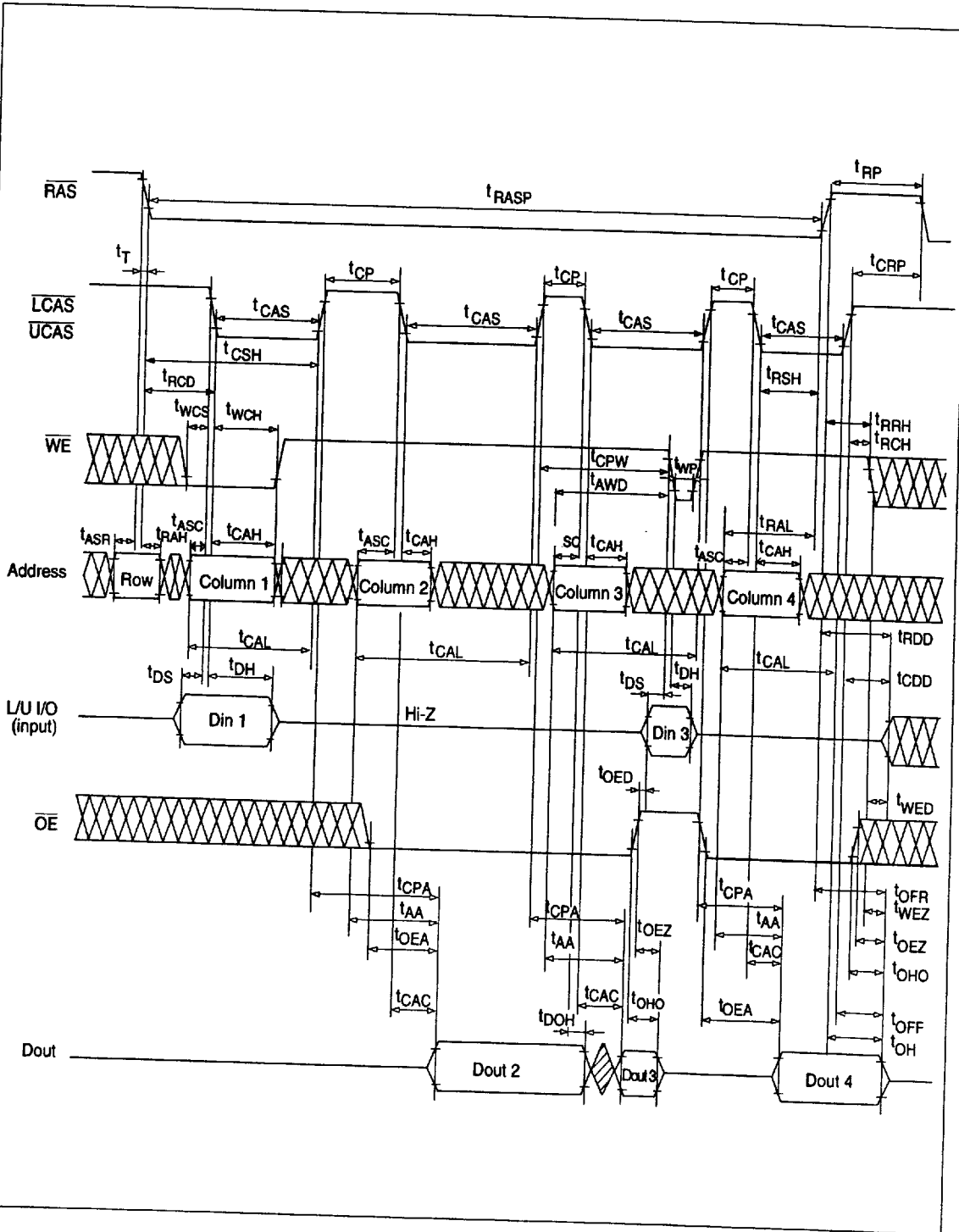


EDO Page Mode Read-Modify-Write Cycle\*19

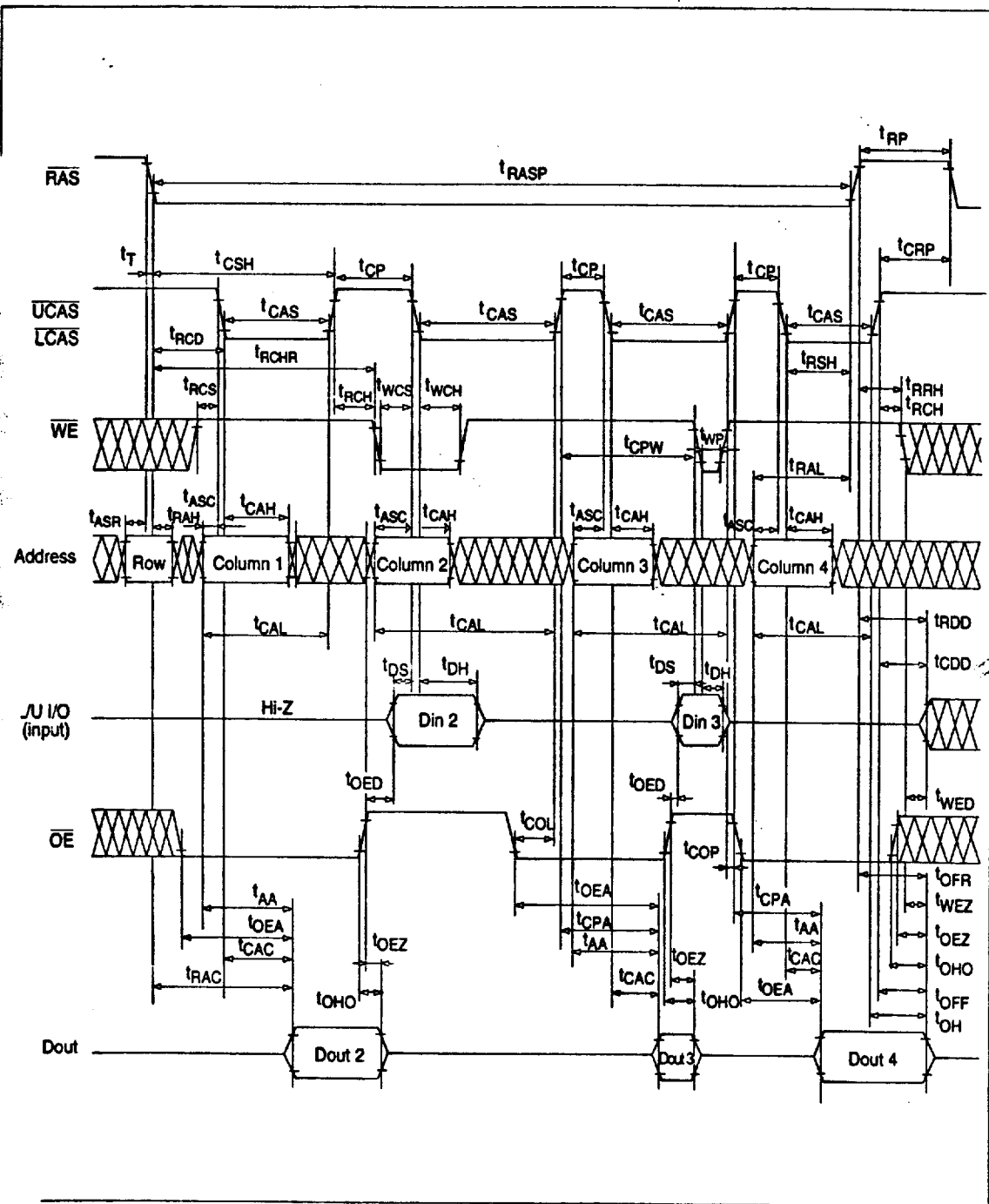




EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)



Self Refresh Cycle (L-version) \*28, 29, 30, 31

