HM51W4100B/BL Series — Preliminary

4,194,304-Word × 1-Bit Dynamic RAM

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM51W4100B/BL is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM51W4100B/BL has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51W4100B/BL offers fast page mode as a high speed access mode.

Multiplexed address input permits the HM51W4100B/BL to be packaged in 20-pin plastic TSOP II and 20-pin plastic TSOP II reverse type.

Features

- Single 3.3 V ± 0.3 V
- High speed
  - Access time
    60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode
    288 mW/252 mW/216 mW (max)
  - Standby mode 7.2 mW (max)
    0.36 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
  1,024 refresh cycles: 128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
  - Self refresh
- Test function
- Battery back up operation (L-version)
  - HM51W4100BL Series

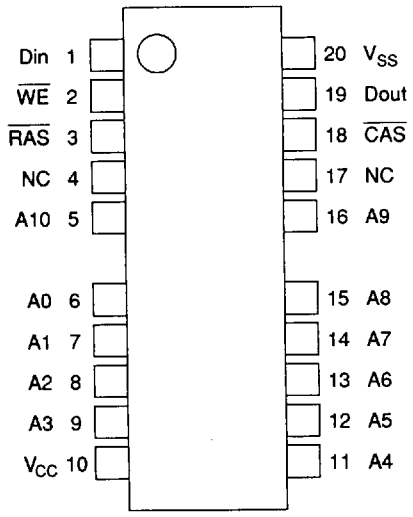
Ordering Information

Type No.	Access time	Package
HM51W4100BTT/BLTT-6	60 ns	20-pin plastic TSOP II (TTP-20D)
HM51W4100BTT/BLTT-7	70 ns	
HM51W4100BTT/BLTT-8	80 ns	
HM51W4100BRR/BLRR-6	60 ns	20-pin plastic TSOP II reverse type (TTP-20DR)
HM51W4100BRR/BLRR-7	70 ns	
HM51W4100BRR/BLRR-8	80 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

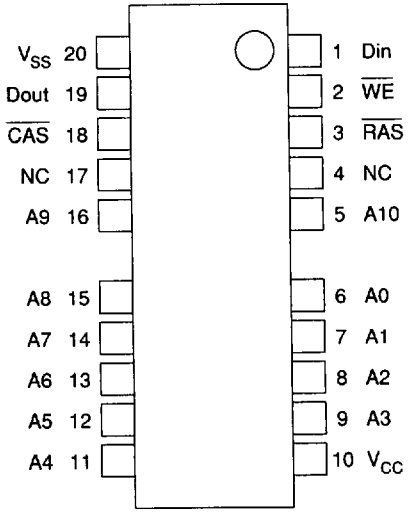
Pin Arrangement

HM51W4100BTT/BLTT Series



(Top View)

HM51W4100BRR/BLRR Series



(Top View)

Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe

Pin name	Function
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power
V_{SS}	Ground
NC	No connection

Block Diagram