

HM51W4170A/AL Series

Preliminary**262,144-Word x 16-Bit Dynamic Random Access Memory****DESCRIPTION**

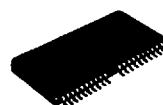
The Hitachi HM51W4170A/AL are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM51W4170A/AL have realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM51W4170A/AL offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM51W4170A/AL to be packaged in standard 400 mil 40-pin plastic TSOP II.

Internal refresh timer enables self refresh operation.

FEATURES

- Single 3.3V (± 0.3 V)
- High Speed
 - Access Time 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
 - Active Mode 288 mW/234 mW/198 mW (max)
 - Standby Mode 7.2 mW (max)
 - 0.36 mW (max) (L-Version)
- Fast Page Mode Capability
- 1,024 Refresh Cycles (16 ms)
- (128 ms) (L-Version)
- 2 $\overline{\text{CAS}}$ Byte Control
- 2 Variations of Refresh
 - $\overline{\text{RAS}}$ Only Refresh
 - $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Battery Back-up Operation (L-Version)
- Self Refresh Operation

HM51W4170ATT/ALTT/ARR/ALRR Series

(TTP-40DB)

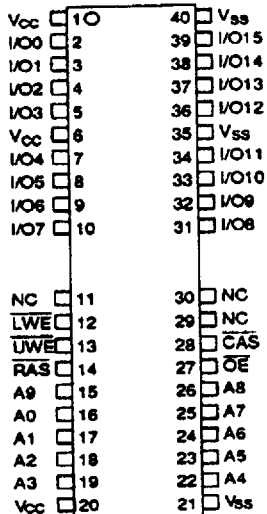
ORDERING INFORMATION

Part No.	Access Time	Package
HM51W4170ATT-7	70 ns	400 mil 40-pin Plastic TSOP II (TTP-40DB)
HM51W4170ATT-8	80 ns	
HM51W4170ATT-10	100 ns	
HM51W4170ALTT-7	70 ns	400 mil 40-pin Plastic TSOP II (TTP-40DB)
HM51W4170ALTT-8	80 ns	
HM51W4170ALTT-10	100 ns	
HM51W4170ARR-7	70 ns	400 mil 40-pin Plastic TSOP II (TTP-40DB)
HM51W4170ARR-8	80 ns	
HM51W4170ARR-10	100 ns	
HM51W4170ALRR-7	70 ns	400 mil 40-pin Plastic TSOP II (TTP-40DB)
HM51W4170ALRR-8	80 ns	
HM51W4170ALRR-10	100 ns	

HM51W4170A/AL Series

■ PIN OUT

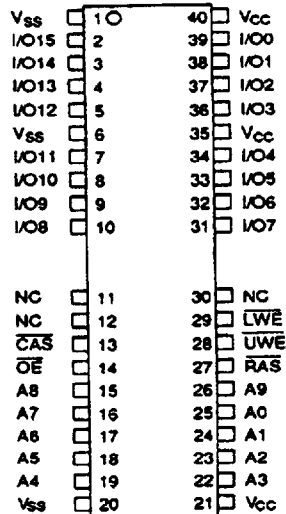
HM51W4170ATT/ALTT Series



(Top View)

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HM51W4170ARR/ALRR Series



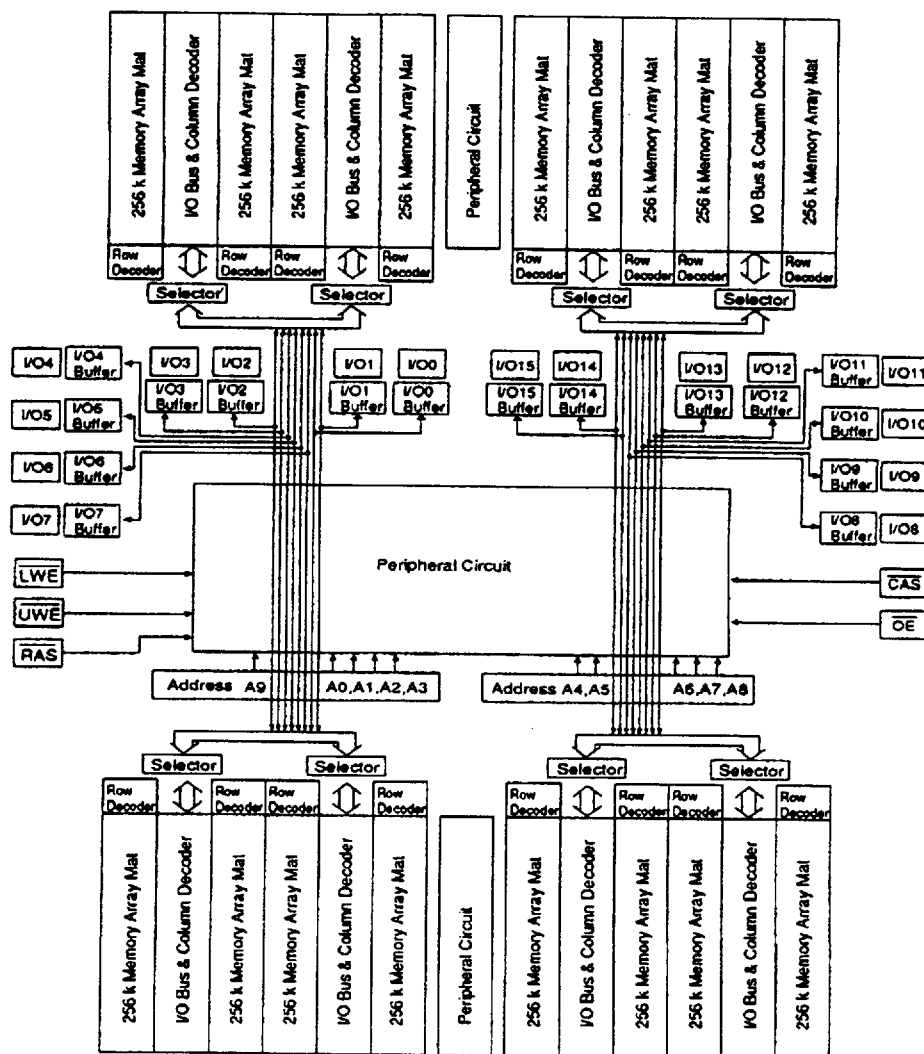
(Top View)

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■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₉	Address Input —Row Address A ₀ -A ₉ —Column Address A ₀ -A ₇ —Refresh Address A ₀ -A ₉
I/O ₀ -I/O ₁₅	Data-in/Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
UWE, LWE	Read/Write Enable
OE	Output Enable
V _{CC}	Power (+ 3.3V)
V _{SS}	Ground

■ BLOCK DIAGRAM



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HM51W4170A/AL Series

■ TRUTH TABLE

Inputs					I/O		Operation
RAS	LWE	UWE	CAS	OE	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	D _{out}	D _{out}	Word Read
L	L	H	L	H	D _{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{in}	Upper Byte Write
L	L	L	L	H	D _{in}	D _{in}	Word Write
L	H	H	L	H	High-Z	High-Z	
H to L	L	L	—	—	High-Z	High-Z	CBR Refresh or Self Refresh

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	- 0.5 to + 4.6	V
Supply Voltage Relative to V _{SS}	V _{CC}	- 0.5 to + 4.6	V
Short Circuit Output Current	I _{out}	50	mA
Power Dissipation	P _T	1.0	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage Temperature	T _{stg}	- 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)²

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{SS}	0	0	0	V	2
	V _{CC}	3.0	3.3	3.6	V	1, 2
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.3	V	1
Input Low Voltage	V _{IL}	- 0.3	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.

2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

• DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$)

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	80	—	65	—	55	mA	RAS Cycling CAS Cycling $t_{RC} = \text{Min}$	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface RAS, CAS = V_{IH} $D_{out} = \text{High-Z}$	
		—	1	—	1	—	1	mA	CMOS Interface RAS, CAS, $\overline{LWE}$, $\overline{UWE}$, $\overline{OE} \geq V_{CC} - 0.2\text{V}$ $D_{out} = \text{High-Z}$	
Standby Current (L-Version)		—	100	—	100	—	100	μA	CMOS Interface RAS, CAS, $\overline{OE}$, $\overline{LWE}$, $\overline{UWE} \geq V_{CC} - 0.2\text{V}$ $D_{out} = \text{High-Z}$	
RAS Only Refresh Current	I_{CC3}	—	75	—	62	—	45	mA	$t_{RC} = \text{Min}$	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	RAS = V_{IH} , CAS = V_{IL} , $D_{out} = \text{Enable}$	1
CAS Before RAS Refresh Current	I_{CC6}	—	75	—	62	—	45	mA	$t_{RC} = \text{Min}$	25
Fast Page Mode Current	I_{CC7}	—	95	—	80	—	75	mA	$t_{PC} = \text{Min}$	1, 3
Battery Back-up Current (Standby with CBR Refresh) (L-Version)	I_{CC10}	—	100	—	100	—	100	μA	Standby: CMOS Interface $D_{out} = \text{High-Z}$ CBR Refresh: $t_{RC} = 125 \mu\text{s}$ $t_{RAS} \leq 1 \mu\text{s}$, CAS = V_{IL} , $\overline{LWE}$, $\overline{UWE}$, $\overline{OE} = V_{IH}$	4
Self Refresh Mode Current	I_{CC11}	—	1	—	1	—	1	mA	CMOS Interface RAS, $\overline{CAS} \leq 0.2\text{V}$, $D_{out} = \text{High-Z}$	
Self Refresh Mode Current (L-Version)		—	100	—	100	—	100	μA	CMOS Interface RAS, $\overline{CAS} \leq 0.2\text{V}$, $D_{out} = \text{High-Z}$	
Input Leakage Current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{in} \leq 4.6\text{V}$	
Output Leakage Current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{out} \leq 4.6\text{V}$ $D_{out} = \text{Disable}$	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High $I_{out} = -2.0 \text{ mA}$	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low $I_{out} = 2.0 \text{ mA}$	

- Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed ≤ 1 time while RAS = V_{IL} .
 3. Address can be changed ≤ 1 time while $\overline{CAS} = V_{IH}$.
 4. $V_{IH} \geq V_{CC} - 0.2\text{V}$, $0 \leq V_{IL} \leq 0.2\text{V}$. Address can be changed ≤ 1 time while $\overline{CAS} = V_{IL}$.
 5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

HM51W4170A/AL Series

- **Capacitance** ($T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $CAS = V_{IH}$ to disable D_{out} .

- **AC Characteristics** ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$)^{1, 14, 15, 17, 18}

Test Conditions

- Input rise and fall times 5 ns
 • Input timing reference levels 0.8V, 2.0V
 • Output load 1 TTL Gate + C_L (100 pF)
 (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
RAS Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
RAS Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
CAS Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	22
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	19
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	19
RAS to CAS Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
RAS to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
RAS Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
CAS Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
OE to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
OE Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
CAS Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 26
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	4, 13, 26
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	5, 13, 26
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	22, 26
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	20
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	16, 19
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column Address to RAS Lead Time	t_{RAL}	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
CAS to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

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Write Cycle

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	tWCS	0	—	0	—	0	—	ns	10, 19
Write Command Hold Time	tWCH	15	—	15	—	20	—	ns	20
Write Command Pulse Width	tWP	10	—	10	—	20	—	ns	21
Write Command to $\overline{\text{RAS}}$ Lead Time	tRWL	20	—	20	—	25	—	ns	21
Write Command to $\overline{\text{CAS}}$ Lead Time	tCWL	20	—	20	—	25	—	ns	21
Data-in Setup Time	tDS	0	—	0	—	0	—	ns	11, 21
Data-in Hold Time	tDH	15	—	15	—	20	—	ns	11, 21
CAS to $\overline{\text{OE}}$ Delay Time	tCOD	—	0	—	0	—	0	ns	22

Read-Modify-Write Cycle

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	tRWC	180	—	200	—	245	—	ns	
RAS to $\overline{\text{WE}}$ Delay Time	tRWD	95	—	105	—	135	—	ns	10, 19
CAS to $\overline{\text{WE}}$ Delay Time	tCWD	45	—	45	—	60	—	ns	10, 19
Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	60	—	65	—	80	—	ns	10, 19
$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	tOEH	20	—	20	—	25	—	ns	21

Refresh Cycle

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	tCSR	10	—	10	—	10	—	ns	19
CAS Hold Time (CAS Before RAS Refresh Cycle)	tCHR	10	—	10	—	10	—	ns	20
RAS Precharge to CAS Hold Time	tRPC	10	—	10	—	10	—	ns	19
CAS Precharge Time in Normal Mode	tCPN	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	tPC	45	—	50	—	55	—	ns	
Fast Page Mode CAS Precharge Time	tCP	10	—	10	—	10	—	ns	
Fast Page Mode RAS Pulse Width	tRASC	—	100000	—	100000	—	100000	ns	12
Access Time from CAS Precharge	tACP	—	40	—	45	—	50	ns	13, 26
RAS Hold Time from CAS Precharge	tRHCP	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle CAS Precharge to $\overline{\text{WE}}$ Delay Time	tCPW	65	—	70	—	85	—	ns	21
Fast Page Mode Read-Modify-Write Cycle Time	tPCM	95	—	100	—	110	—	ns	

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Self Refresh Mode

Parameter	Symbol	HM51W4170A/AL-7		HM51W4170A/AL-8		HM51W4170A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
RAS Pulse Width (Self Refresh)	t_{RASS}	100	—	100	—	100	—	μs	
RAS Precharge Time (Self Refresh)	t_{RPS}	130	—	150	—	180	—	ns	
CAS Hold Time (Self Refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

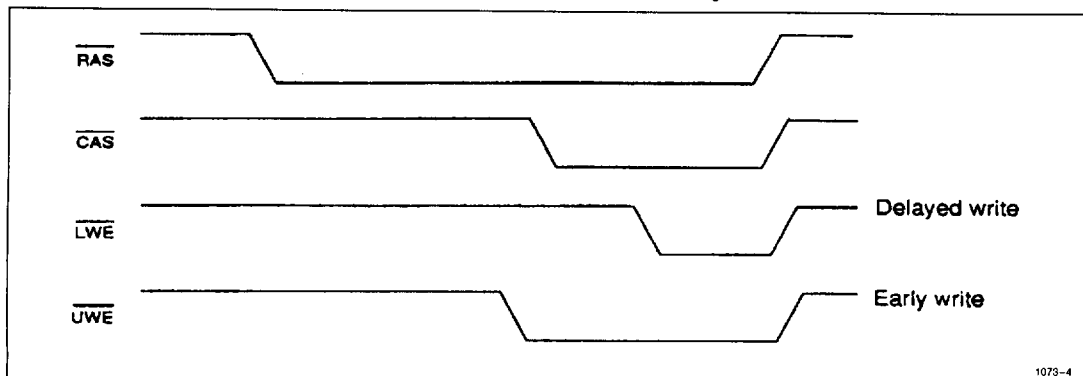
Notes: 1. AC measurements assume $t_T = 5$ ns.

- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 1 TTL load and 100 pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
- $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
- t_{RASC} defines RAS pulse width in fast page mode cycles.
- Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
- After power up pause for 100 μs , then DRAM initialization requires a minimum of eight $\overline{\text{RAS}}$ only refresh or eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles. If the user will implement $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ timing in their system, then the eight initialization cycles MUST be $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles.
- In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.
- A word of data can be written only when $\overline{\text{LWE}}$ and $\overline{\text{UWE}}$ go low at the same time. This implies that early write cycles cannot be combined with delayed write cycles in the same cycles because all data is latched at the fall of the first $\overline{\text{WE}}$. In other words, staggering the $\overline{\text{WE}}$ signals in one cycle is not permitted.
- t_{RCH} , t_{RHH} , t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are determined by the earlier falling edge of $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.
- t_{WCH} and t_{RCS} are determined by the later rising edge of $\overline{\text{UWE}}$ or $\overline{\text{LWE}}$.
- t_{WP} , t_{RWL} , t_{CWL} , t_{OEHL} , t_{DS} , t_{DH} and t_{CPW} should be satisfied by both $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$.
- When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH}(\text{min})/V_{IL}(\text{max})$ level.
- If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
- If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
- Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
- Measured with a load equivalent to 1 TTL load and 100 pF ($V_{OH} = 2.0V$, $V_{OL} = 0.8V$).

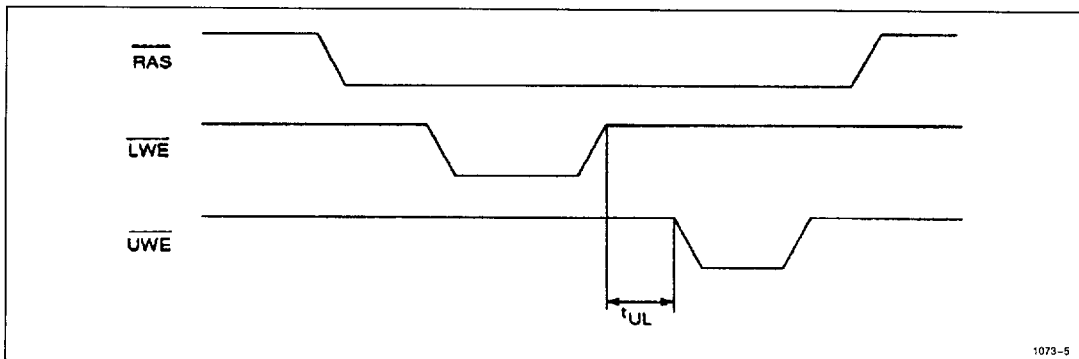
Notes Concerning 2WE Control

Please do not separate the $\overline{UWE}/\overline{LWE}$ operation timing intentionally. However skew between $\overline{UWE}/\overline{LWE}$ are allowed under the following conditions.

- (1) Each of the $\overline{UWE}/\overline{LWE}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.



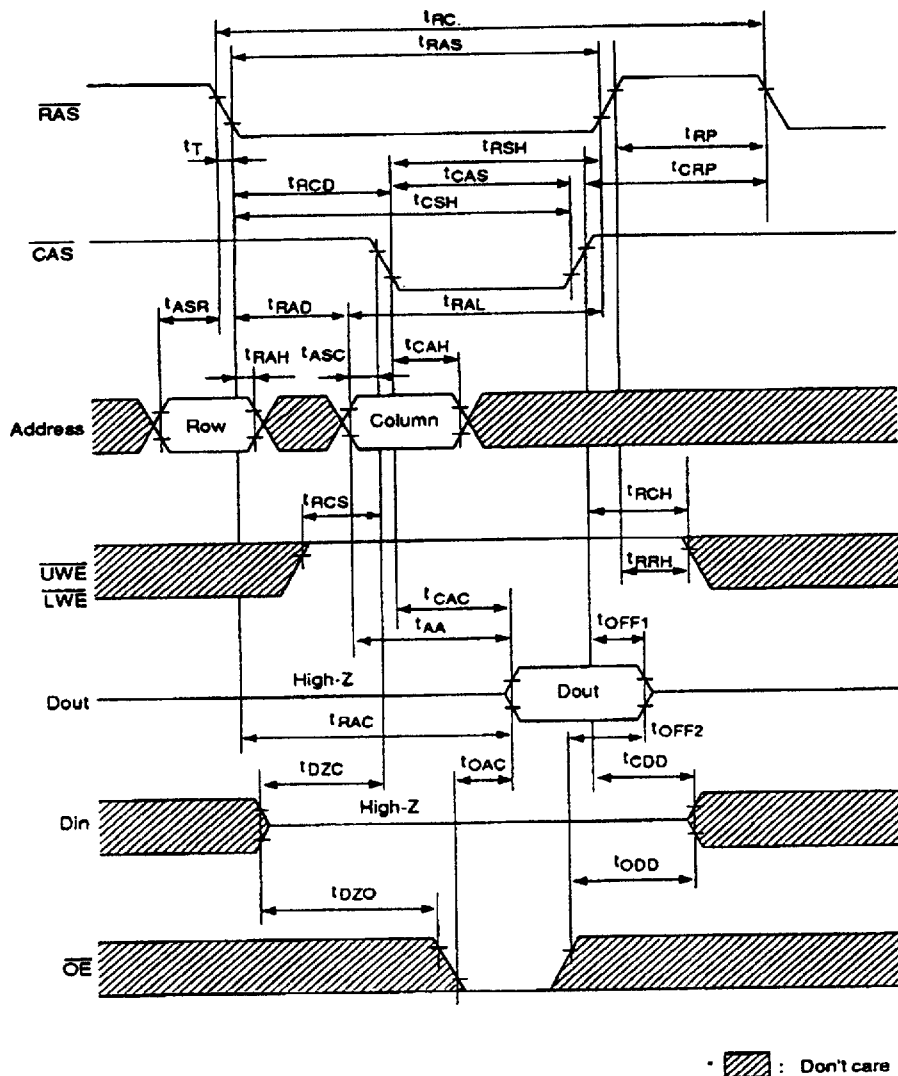
- (3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CPW} \leq t_{UL}$) is satisfied, fast page mode can be performed.



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■ TIMING WAVEFORMS

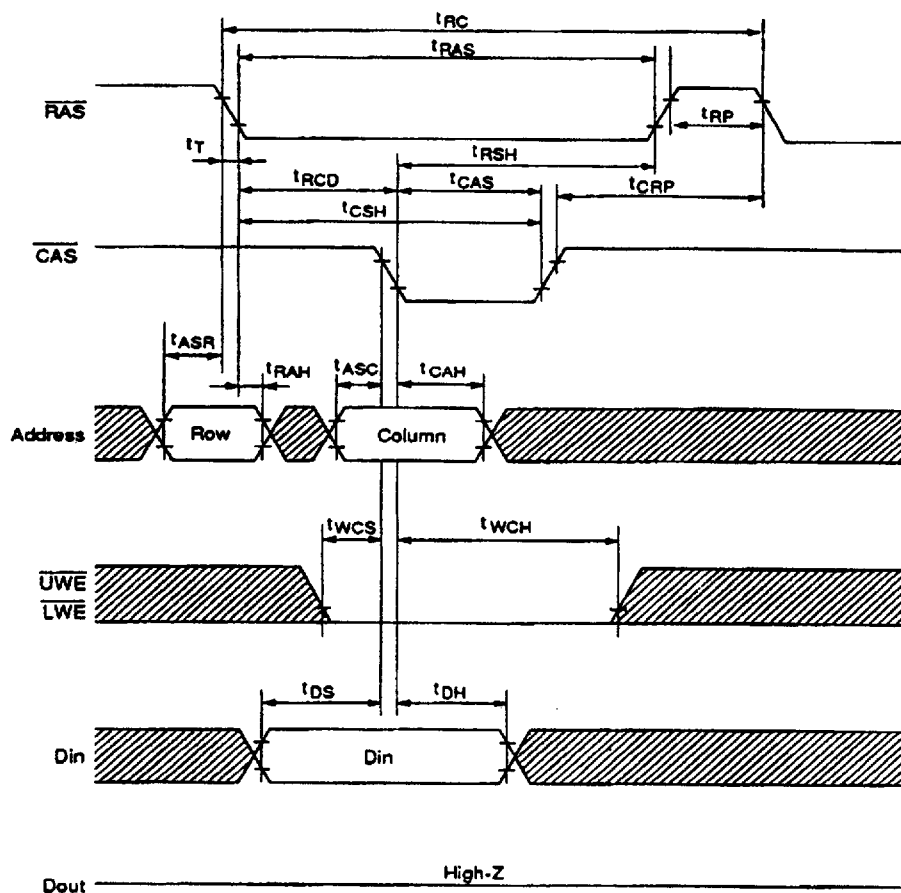
• Read Cycle



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• Early Write Cycle



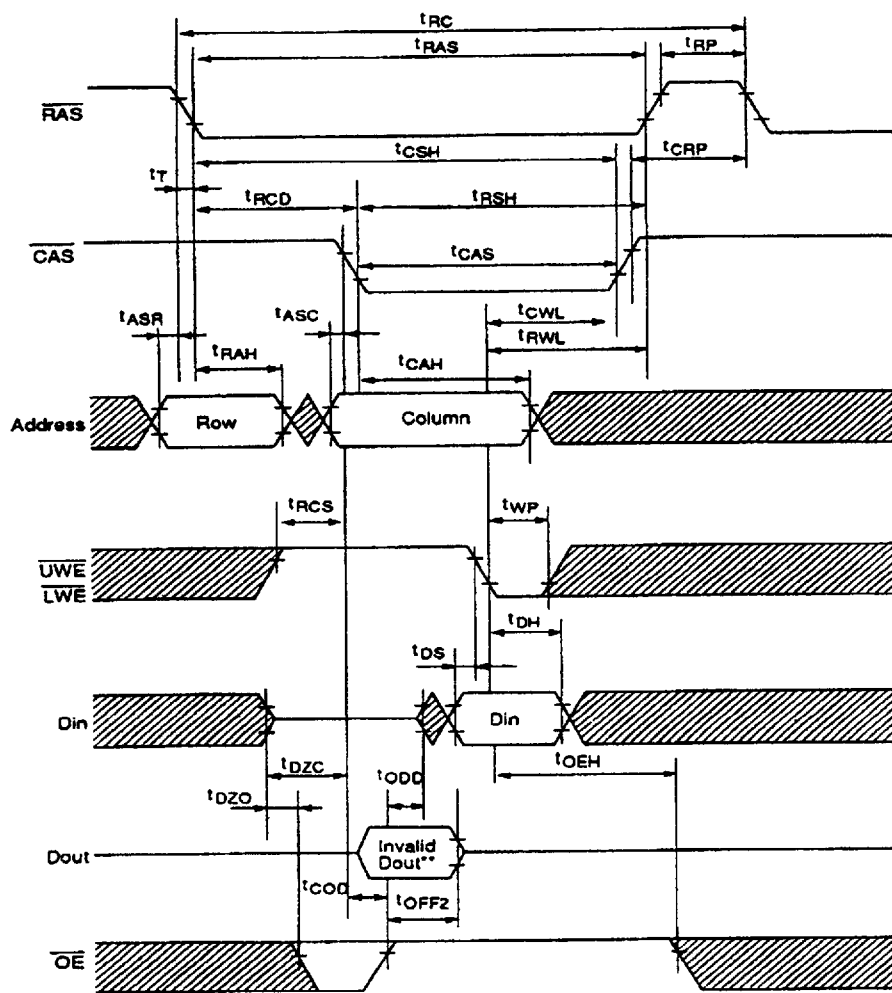
• : Don't care
 ** $\overline{OE}$: Don't care

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HM51W4170A/AL Series

• Delayed Write Cycle



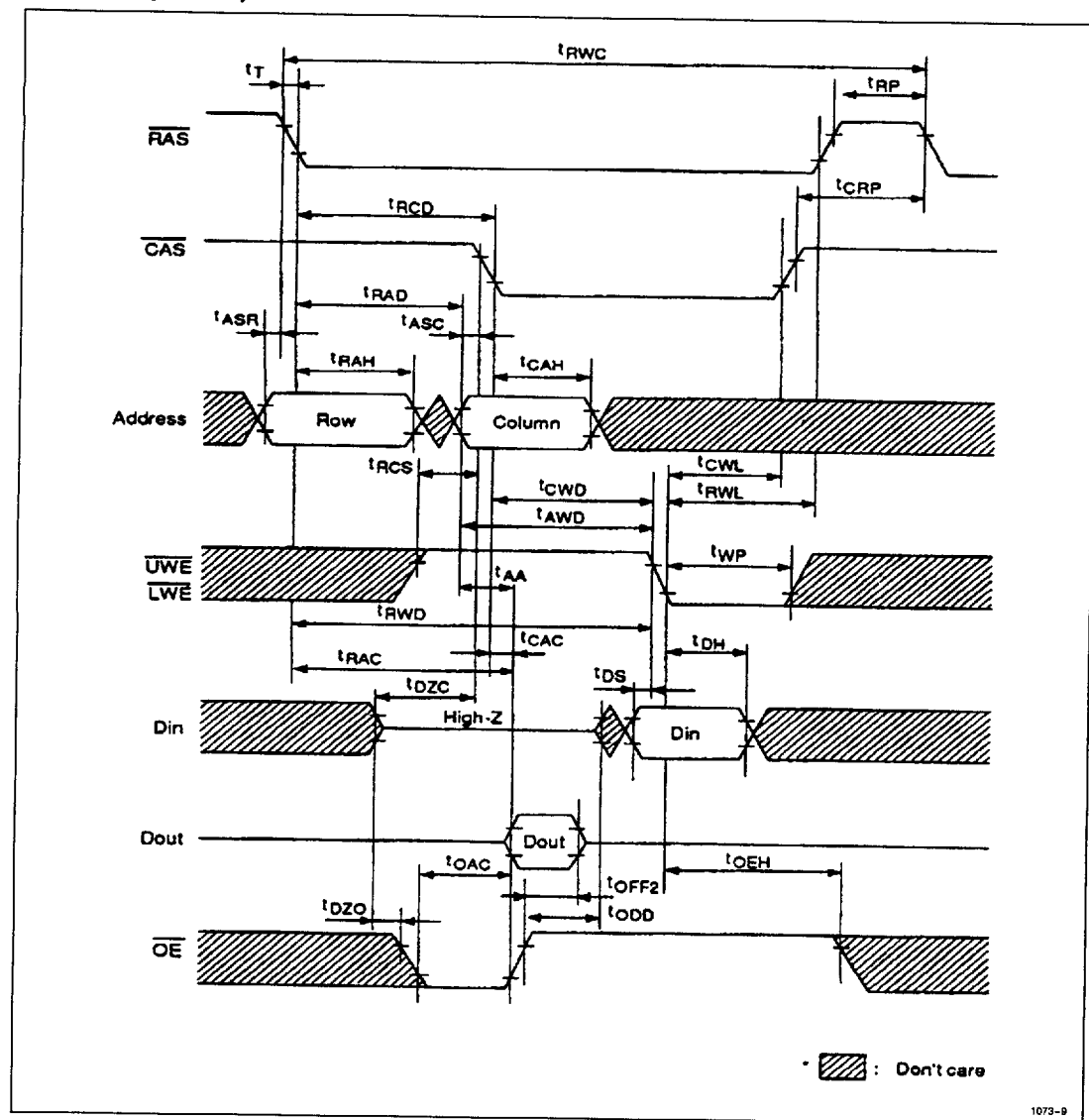
• : Don't care

** Do not enable $\overline{\text{Dout}}$ during delayed write cycle.

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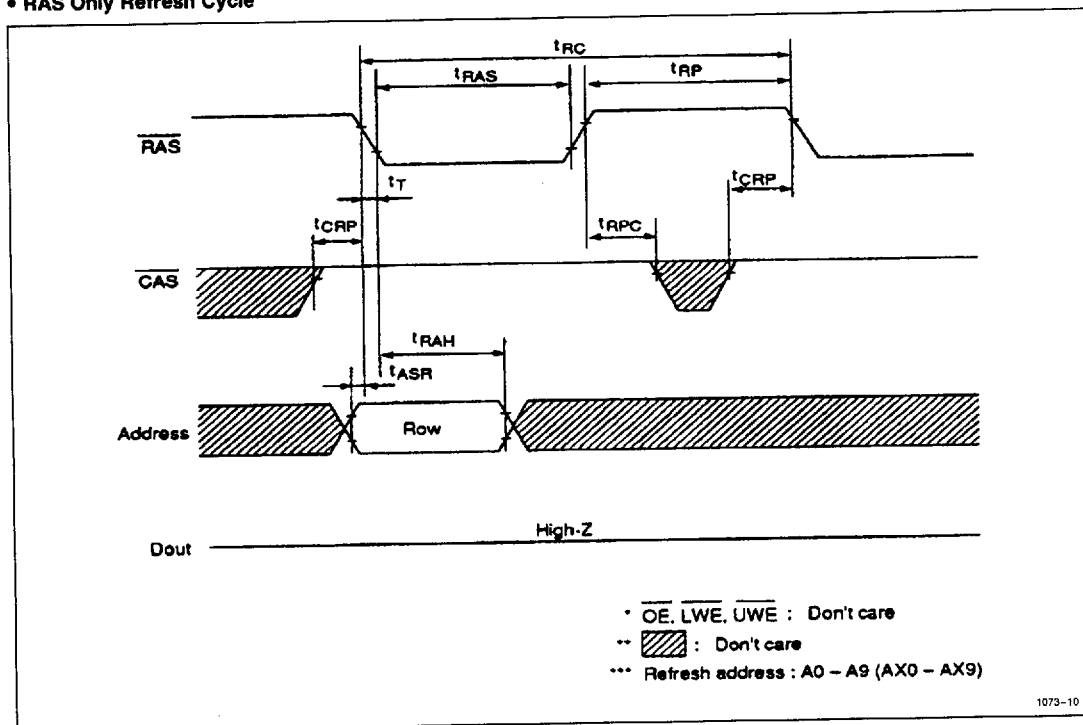
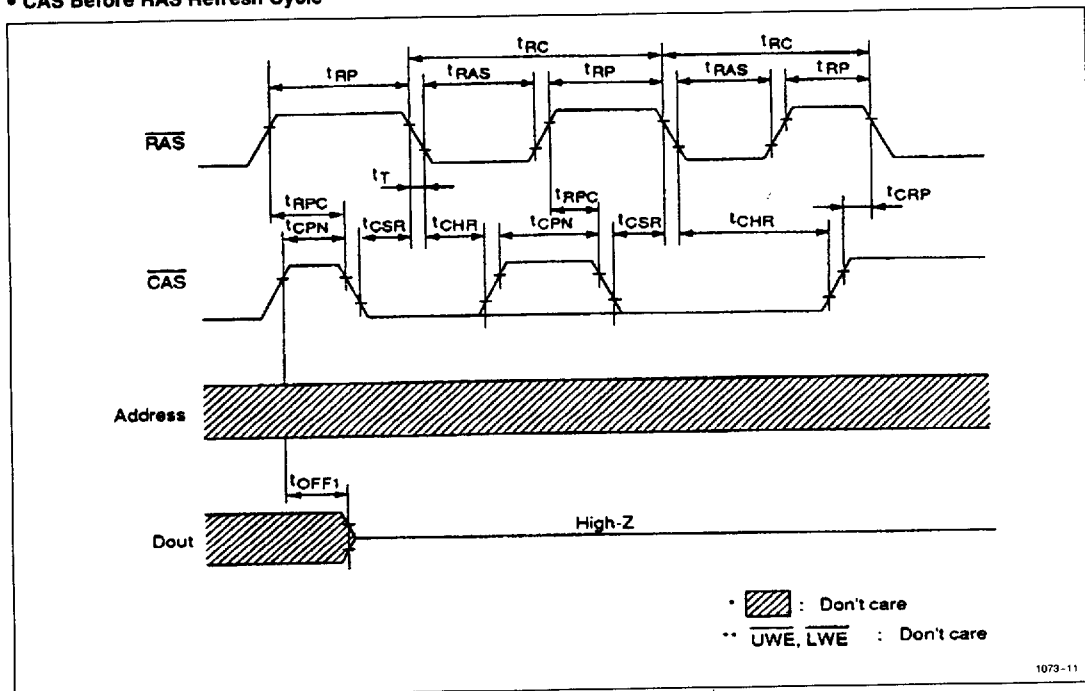
• Read-Modify-Write Cycle



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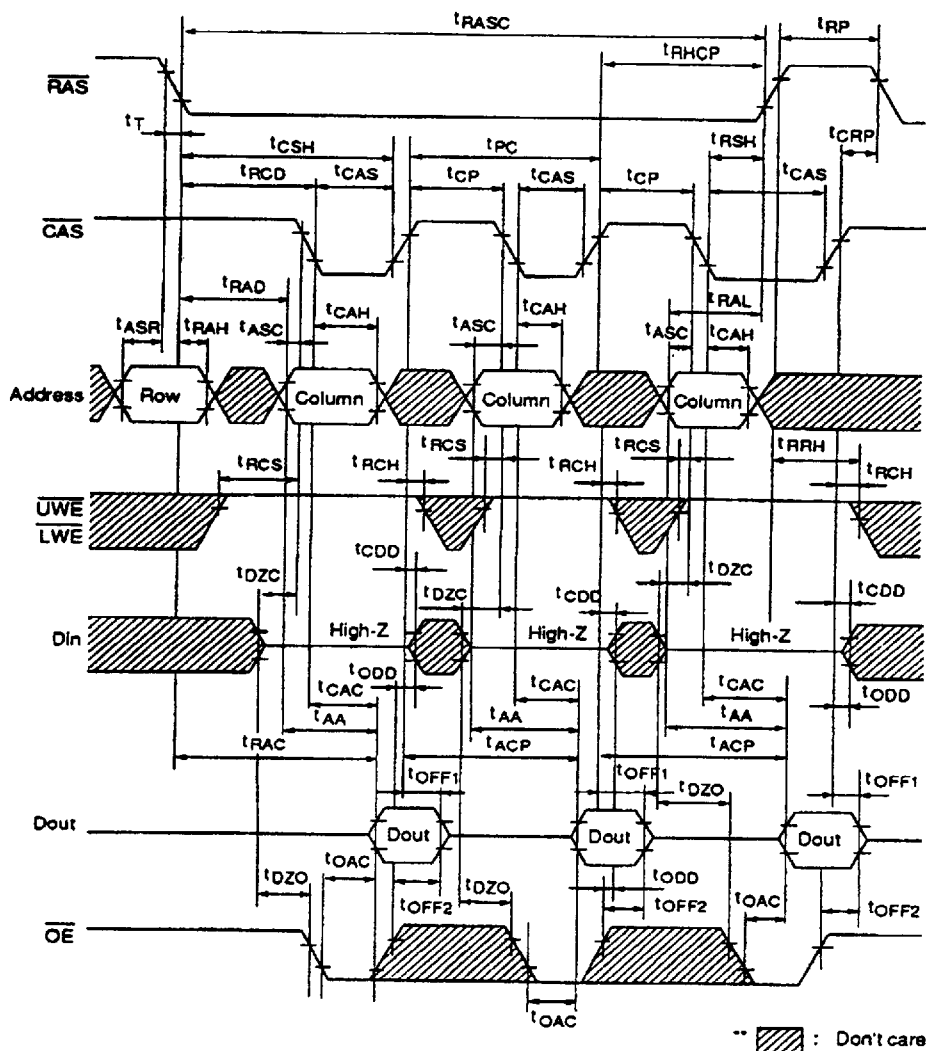
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HM51W4170A/AL Series

• $\overline{\text{RAS}}$ Only Refresh Cycle• $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

HITACHI®

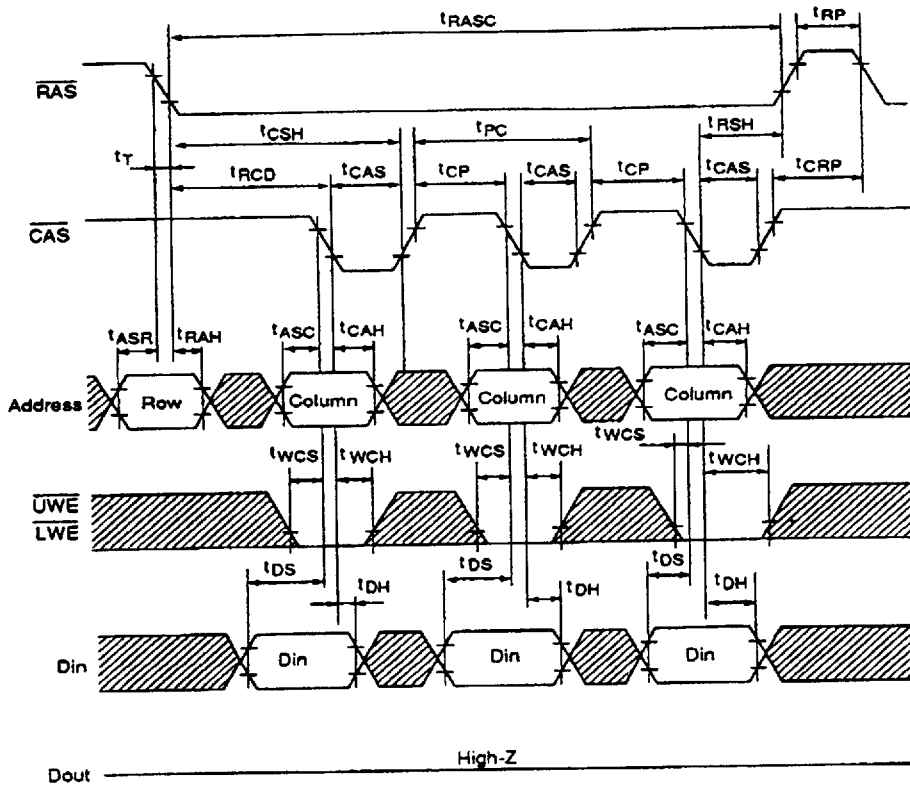
- **Fast Page Mode Read Cycle**



1073-12

HM51W4170A/AL Series

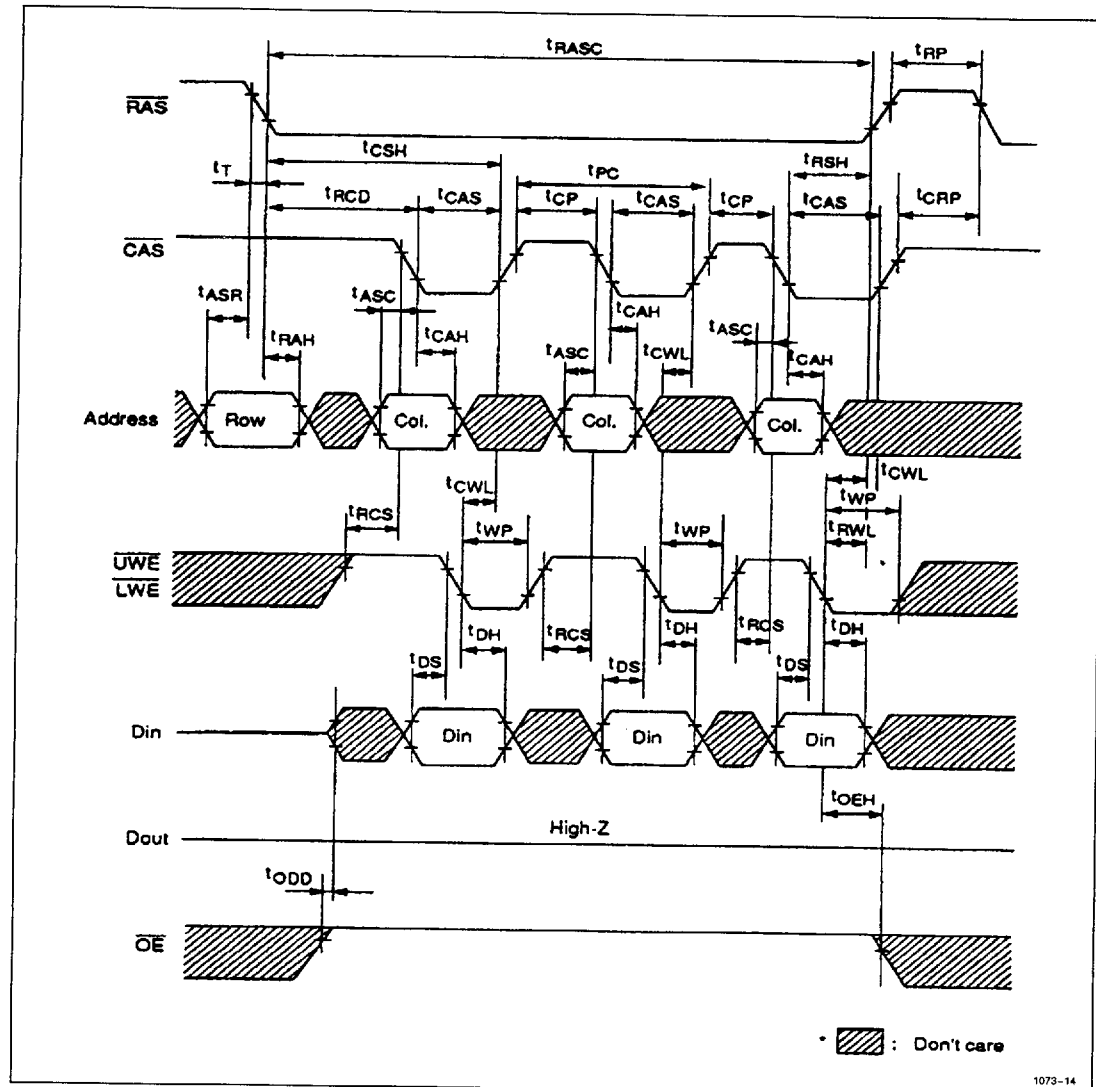
• Fast Page Mode Early Write Cycle

• $\overline{OE}$: Don't care

** : Don't care

1079-13

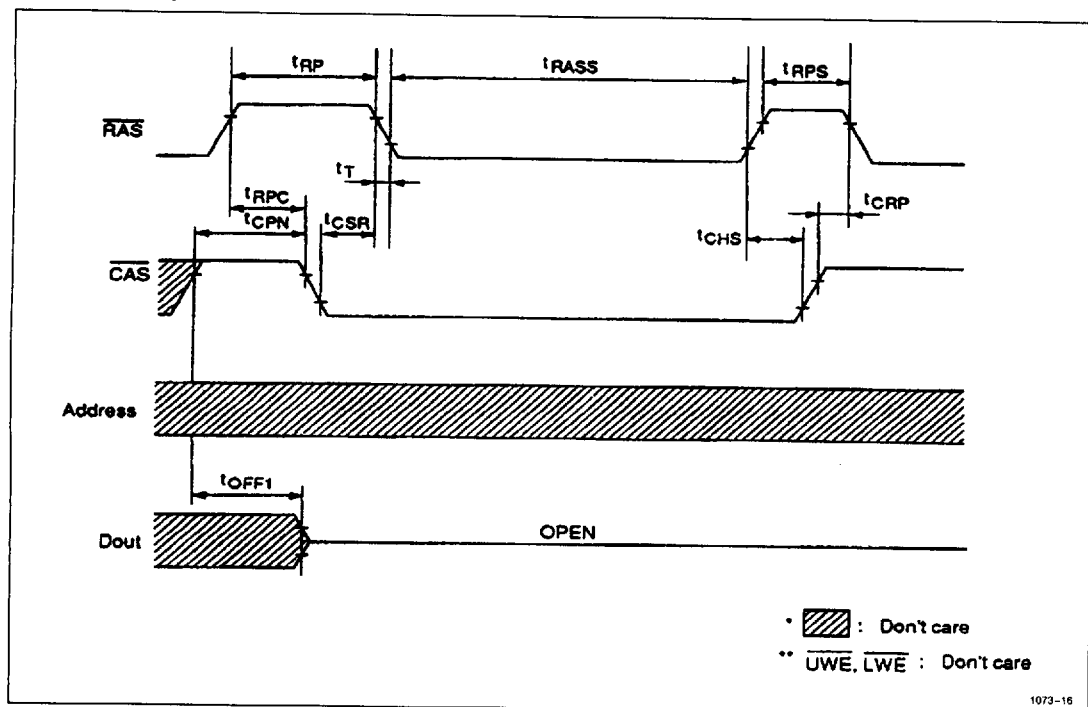
• Fast Page Mode Delayed Write Cycle



- **Fast Page Mode Read-Modify-Write Cycle**



• Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
2. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed with $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
3. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.