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# HM5225645F-B60

# HM5225325F-B60

256M LVTTL interface SDRAM  
100 MHz

1-Mword  $\times$  64-bit  $\times$  4-bank/2-Mword  $\times$  32-bit  $\times$  4-bank  
PC/100 SDRAM

# HITACHI

ADE-203-1014C (Z)  
Rev. 1.0  
Oct. 1, 1999

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## Description

The Hitachi HM5225645F is a 256-Mbit SDRAM organized as 1048576-word  $\times$  64-bit  $\times$  4-bank. The Hitachi HM5225325F is a 256-Mbit SDRAM organized as 2097152-word  $\times$  32-bit  $\times$  4-bank. All inputs and outputs are referred to the rising edge of the clock input. It is packaged in standard 108 bump BGA.

## Features

- Single chip wide bit solution ( $\times$  64/ $\times$  32)
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTL interface
- Extremely small foot print: 1.27 mm pitch
  - Package: BGA (BP-108)
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 4/8/full page)
  - Interleave (BL = 4/8)
- Programmable  $\overline{\text{CAS}}$  latency: 2/3
- Byte control by DQMB

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## HM5225645F-B60, HM5225325F-B60

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- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh
- Full page burst length capability
  - Sequential burst
  - Burst stop capability

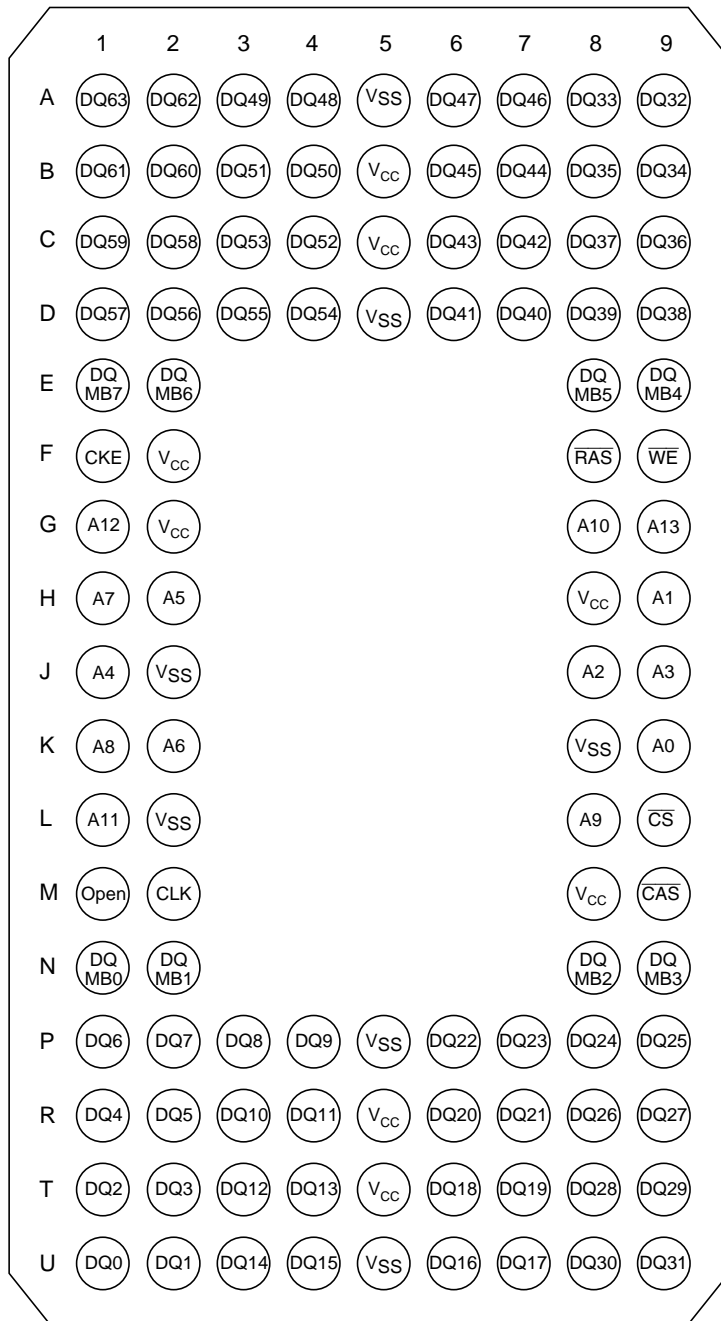
### Ordering Information

Type No.	Frequency	$\overline{\text{CAS}}$ latency	Package
HM5225645FBP-B60*	100 MHz	3	14 mm × 22 mm 108 bump BGA (BP-108)
HM5225325FBP-B60*	100 MHz	3	

Note: 66 MHz operation at  $\overline{\text{CAS}}$  latency = 2.

Pin Arrangement (HM5225645F)

108-bump BGA



(Top view)

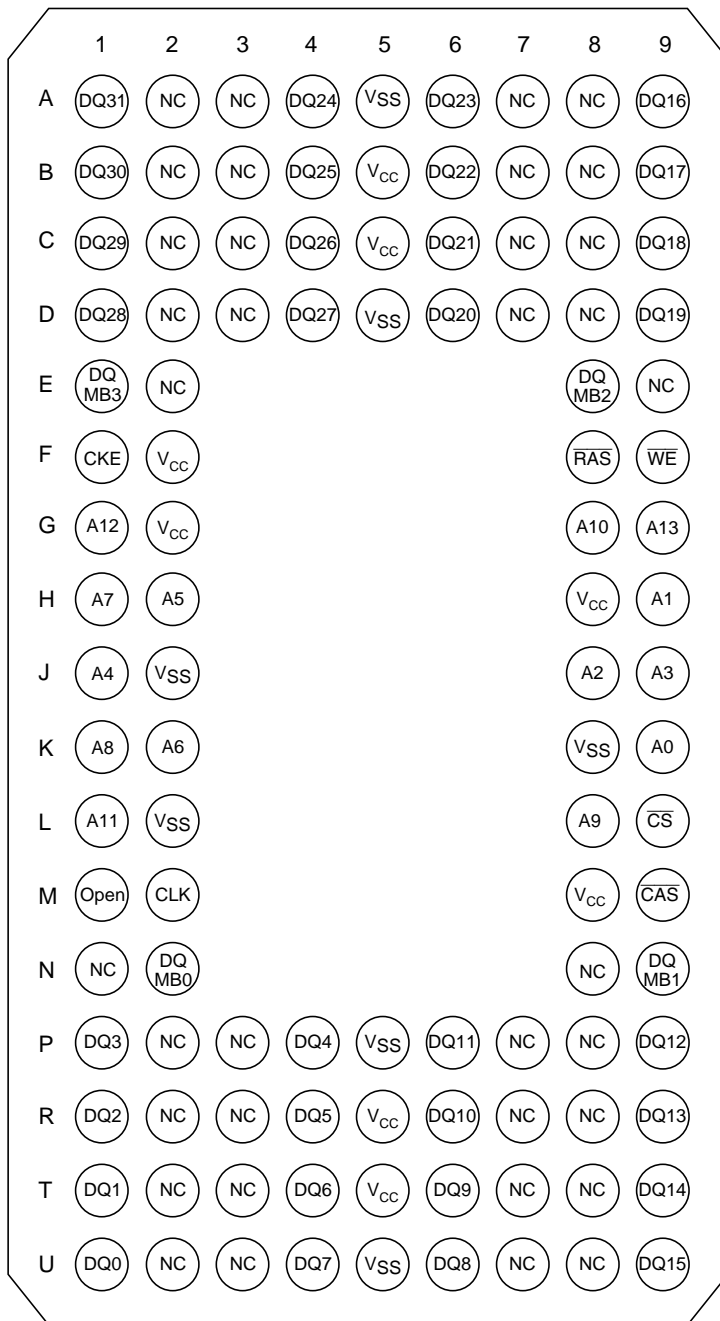
**Pin Description (HM5225645F)**

<b>Pin name</b>	<b>Function</b>
A0 to A13	Address input Row address A0 to A11 Column address A0 to A7 Bank select address A12/A13 (BS)
DQ0 to DQ63	Data-input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{RAS}}$	Row address strobe command
$\overline{\text{CAS}}$	Column address strobe command
$\overline{\text{WE}}$	Write enable
DQMB0 to DQMB7	Byte data mask* <sup>1</sup>
CLK	Clock input
CKE	Clock enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
Open	Open* <sup>2</sup>

- Note:
1. DQMB0: DQ0 to DQ7  
DQMB1: DQ8 to DQ15  
DQMB2: DQ16 to DQ23  
DQMB3: DQ24 to DQ31  
DQMB4: DQ32 to DQ39  
DQMB5: DQ40 to DQ47  
DQMB6: DQ48 to DQ55  
DQMB7: DQ56 to DQ63
  2. Don't connect. Internally connected with die.

Pin Arrangement (HM5225325F)

108-bump BGA



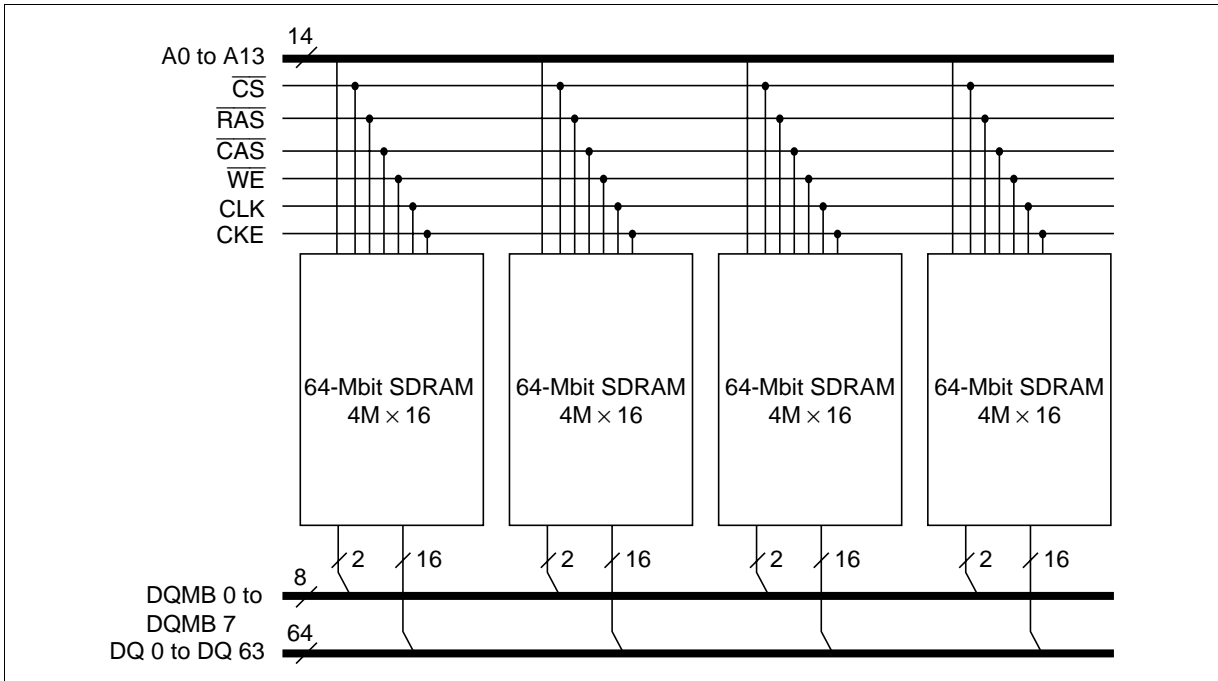
(Top view)

**Pin Description (HM5225325F)**

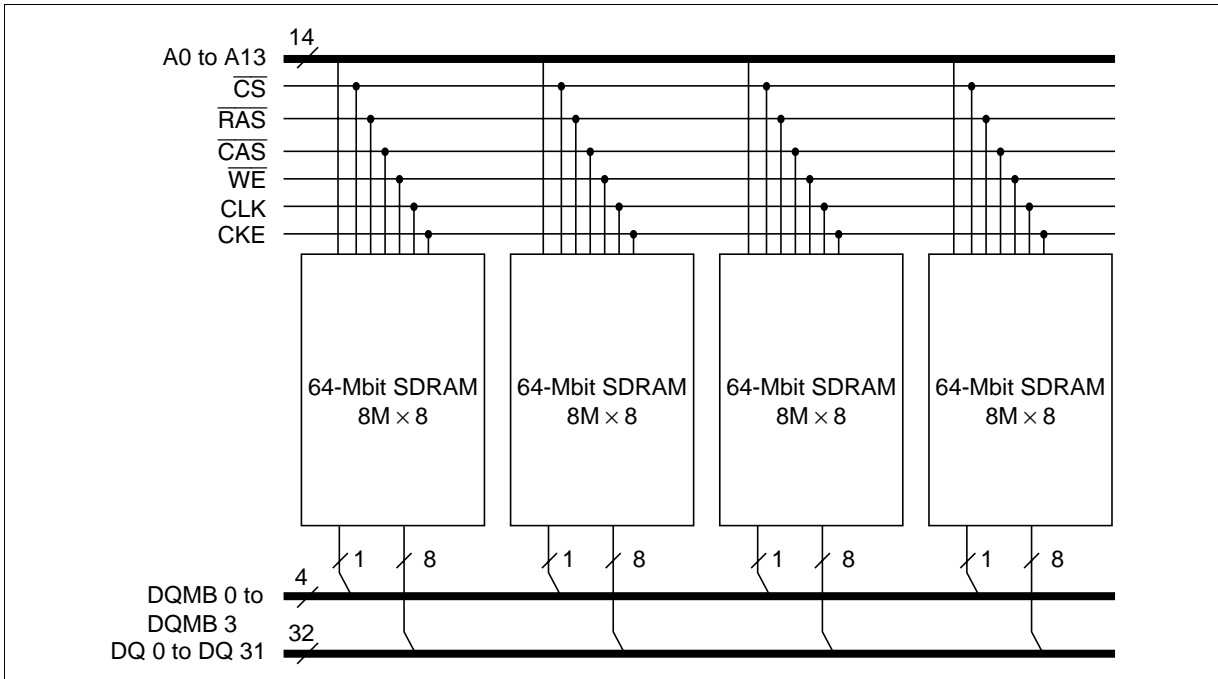
<b>Pin name</b>	<b>Function</b>
A0 to A13	Address input Row address A0 to A11 Column address A0 to A8 Bank select address A12/A13 (BS)
DQ0 to DQ31	Data-input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{RAS}}$	Row address strobe command
$\overline{\text{CAS}}$	Column address strobe command
$\overline{\text{WE}}$	Write enable
DQMB0 to DQMB3	Byte data mask*1
CLK	Clock input
CKE	Clock enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
Open	Open*2
NC	No connection*3

- Note:
1. DQMB0: DQ0 to DQ7  
DQMB1: DQ8 to DQ15  
DQMB2: DQ16 to DQ23  
DQMB3: DQ24 to DQ31
  2. Don't connect. Internally connected with die.
  3. Not internally connected with die.

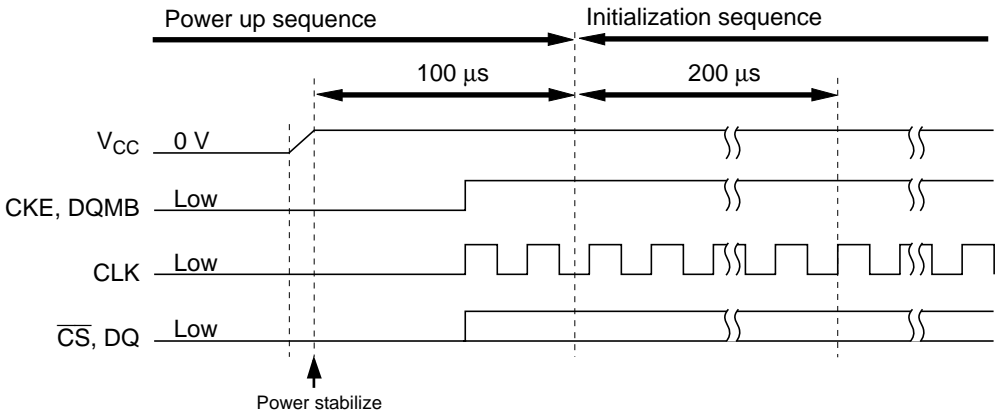
Block Diagram (HM5225645F)



Block Diagram (HM5225325F)



**Power-up Sequence and Initialization Sequence**



**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to $V_{CC} + 0.5$ ( $\leq 4.6$ (max))	V	1
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V	1
Short circuit output current	$I_{out}$	50	mA	
Operating temperature	$T_{opr}$	0 to +70 ( $T_j$ max = 110)	$^{\circ}$ C	
Storage temperature	$T_{stg}$	-55 to +125	$^{\circ}$ C	

Note: 1. Respect to  $V_{SS}$

**DC Operating Conditions** ( $T_{case} = 0$  to +70 $^{\circ}$ C [ $T_j$  max = 110 $^{\circ}$ C])

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	$V_{CC}$	3.0	3.6	V	1, 2
	$V_{SS}$	0	0	V	3
Input high voltage	$V_{IH}$	2.0	$V_{CC} + 0.3$	V	1, 4
Input low voltage	$V_{IL}$	-0.3	0.8	V	1, 5

- Notes: 1. All voltage referred to  $V_{SS}$   
 2. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
 3. The supply voltage with all  $V_{SS}$  pins must be on the same level.  
 4.  $V_{IH}$  (max) =  $V_{CC} + 2.0$  V for pulse width  $\leq 3$  ns at  $V_{CC}$ .  
 5.  $V_{IL}$  (min) =  $V_{SS} - 2.0$  V for pulse width  $\leq 3$  ns at  $V_{SS}$ .



## DC Characteristics

(T<sub>case</sub> = 0 to 70°C [T<sub>j</sub> max = 110°C]), V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V (HM5225645F)

Parameter	Symbol	HM5225645F		Unit	Test conditions	Notes
		Min	Max			
Operating current (CAS latency = 2)	I <sub>CC1</sub>	—	200	mA	Burst length = 1 t <sub>RC</sub> = min	1, 2, 3
(CAS latency = 3)	I <sub>CC1</sub>	—	220			
Standby current in power down	I <sub>CC2P</sub>	—	12	mA	CKE = V <sub>IL</sub> , t <sub>CK</sub> = 12 ns	6
Standby current in power down (input signal stable)	I <sub>CC2PS</sub>	—	8			
Standby current in non power down	I <sub>CC2N</sub>	—	64	mA	CKE, $\overline{\text{CS}}$ = V <sub>IH</sub> , t <sub>CK</sub> = 12 ns	4
Standby current in non power down (input signal stable)	I <sub>CC2NS</sub>	—	36			
Active standby current in power down	I <sub>CC3P</sub>	—	16	mA	CKE = V <sub>IL</sub> , t <sub>CK</sub> = 12 ns	1, 2, 6
Active standby current in power down (input signal stable)	I <sub>CC3PS</sub>	—	12			
Active standby current in non power down	I <sub>CC3N</sub>	—	80	mA	CKE, $\overline{\text{CS}}$ = V <sub>IH</sub> , t <sub>CK</sub> = 12 ns	1, 2, 4
Active standby current in non power down (input signal stable)	I <sub>CC3NS</sub>	—	60			
Burst operating current (CAS latency = 2)	I <sub>CC4</sub>	—	220	mA	t <sub>CK</sub> = min, BL = 4	1, 2, 5
(CAS latency = 3)	I <sub>CC4</sub>	—	270			
Refresh current	I <sub>CC5</sub>	—	380	mA	t <sub>RC</sub> = min	3
Self refresh current	I <sub>CC6</sub>	—	4			
Self refresh current (L-version)	I <sub>CC6</sub>	—	1.6	mA	V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V V <sub>IL</sub> ≤ 0.2 V	8
Input leakage current	I <sub>LI</sub>	-4	4			
Output leakage current	I <sub>LO</sub>	-6	6	μA	0 ≤ V <sub>out</sub> ≤ V <sub>CC</sub> DQ = disable	
Output high voltage	V <sub>OH</sub>	2.4	—			
Output low voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 4 mA	

# HM5225645F-B60, HM5225325F-B60

## DC Characteristics

(T<sub>case</sub> = 0 to 70°C [T<sub>j</sub> max = 110°C]), V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V (HM5225325F)

Parameter	Symbol	HM5225325F		Unit	Test conditions	Notes
		Min	Max			
Operating current (CAS latency = 2)	I <sub>CC1</sub>	—	180	mA	Burst length = 1 t <sub>RC</sub> = min	1, 2, 3
	(CAS latency = 3)	I <sub>CC1</sub>	—			
Standby current in power down	I <sub>CC2P</sub>	—	12	mA	CKE = V <sub>IL</sub> , t <sub>CK</sub> = 12 ns	6
Standby current in power down (input signal stable)	I <sub>CC2PS</sub>	—	8			
Standby current in non power down	I <sub>CC2N</sub>	—	64	mA	CKE, $\overline{\text{CS}} = V_{\text{IH}}$ , t <sub>CK</sub> = 12 ns	4
Standby current in non power down (input signal stable)	I <sub>CC2NS</sub>	—	36			
Active standby current in power down	I <sub>CC3P</sub>	—	16	mA	CKE = V <sub>IL</sub> , t <sub>CK</sub> = 12 ns	1, 2, 6
Active standby current in power down (input signal stable)	I <sub>CC3PS</sub>	—	12			
Active standby current in non power down	I <sub>CC3N</sub>	—	80	mA	CKE, $\overline{\text{CS}} = V_{\text{IH}}$ , t <sub>CK</sub> = 12 ns	1, 2, 4
Active standby current in non power down (input signal stable)	I <sub>CC3NS</sub>	—	60			
Burst operating current (CAS latency = 2)	I <sub>CC4</sub>	—	200	mA	t <sub>CK</sub> = min, BL = 4	1, 2, 5
(CAS latency = 3)	I <sub>CC4</sub>	—	250			
Refresh current	I <sub>CC5</sub>	—	380	mA	t <sub>RC</sub> = min	3
Self refresh current	I <sub>CC6</sub>	—	4			
Self refresh current (L-version)	I <sub>CC6</sub>	—	1.6	mA	V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V V <sub>IL</sub> ≤ 0.2 V	8
Input leakage current	I <sub>LI</sub>	-4	4			
Output leakage current	I <sub>LO</sub>	-6	6	μA	0 ≤ V <sub>out</sub> ≤ V <sub>CC</sub> DQ = disable	
Output high voltage	V <sub>OH</sub>	2.4	—			
Output low voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 4 mA	

- Notes:
1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  (max) is specified at the output open condition.
  2. One bank operation.
  3. Input signals are changed once per one clock.
  4. Input signals are changed once per two clocks.
  5. Input signals are changed once per four clocks.
  6. After power down mode, CLK operating current.
  7. After power down mode, no CLK operating current.
  8. After self refresh mode set, self refresh current.
  9. Input signals are  $V_{IH}$  or  $V_{IL}$  fixed.

## Capacitance ( $T_a = 25^\circ\text{C}$ , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (CLK)	$C_{i1}$	10	14	pF	1, 2, 4
Input capacitance (Input except DQM)	$C_{i2}$	10	14	pF	1, 2, 4
Input capacitance (DQM)	$C_{i3}$	2.5	5	pF	1, 2, 4
Output capacitance (DQ)	$C_o$	3	5	pF	1, 2, 3, 4

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
  2. Measurement condition:  $f = 1\text{ MHz}$ ,  $1.4\text{ V}$  bias,  $200\text{ mV}$  swing.
  3.  $DQMB = V_{IH}$  to disable Dout.
  4. This parameter is sampled and not 100% tested.

# HM5225645F-B60, HM5225325F-B60

## AC Characteristics

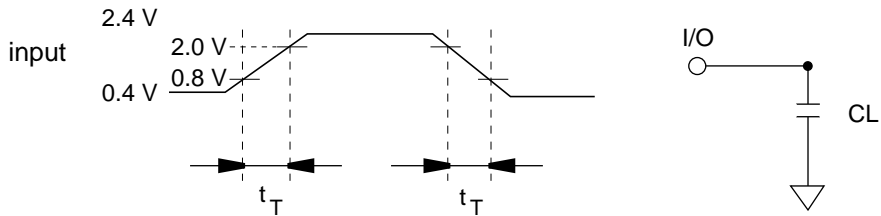
(T<sub>case</sub> = 0 to 70°C [T<sub>j</sub> max = 110°C]), V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V)

Parameter	HITACHI Symbol	PC/100 Symbol	HM5225645F/HM5225325F -B60			
			Min	Max	Unit	Notes
System clock cycle time ( $\overline{\text{CAS}}$ latency = 2)	t <sub>CK</sub>	Tclk	15	—	ns	1
( $\overline{\text{CAS}}$ latency = 3)	t <sub>CK</sub>	Tclk	10	—	ns	
CLK high pulse width	t <sub>CKH</sub>	Tch	3	—	ns	1
CLK low pulse width	t <sub>CKL</sub>	Tcl	3	—	ns	1
Access time from CLK ( $\overline{\text{CAS}}$ latency = 2)	t <sub>AC</sub>	Tac	—	8	ns	1, 2
( $\overline{\text{CAS}}$ latency = 3)	t <sub>AC</sub>	Tac	—	6	ns	
Data-out hold time	t <sub>OH</sub>	Toh	3	—	ns	1, 2
CLK to Data-out low impedance	t <sub>LZ</sub>		2	—	ns	1, 2, 3
CLK to Data-out high impedance ( $\overline{\text{CAS}}$ latency = 2, 3)	t <sub>HZ</sub>		—	6	ns	1, 4
Input setup time	t <sub>AS</sub> , t <sub>CS</sub> , t <sub>DS</sub> , t <sub>CES</sub>	Tsi	2	—	ns	1, 5, 6
CKE setup time for power down exit	t <sub>CESP</sub>	Tpde	2	—	ns	1
Input hold time	t <sub>AH</sub> , t <sub>CH</sub> , t <sub>DH</sub> , t <sub>CEH</sub>	Thi	1	—	ns	1, 5
Ref/Active to Ref/Active command period	t <sub>RC</sub>	Trc	70	—	ns	1
Active to Precharge command period	t <sub>RAS</sub>	Tras	50	120000	ns	1
Active command to column command (same bank)	t <sub>RCD</sub>	Trcd	20	—	ns	1
Precharge to active command period	t <sub>RP</sub>	Trp	20	—	ns	1
Write recovery or data-in to precharge lead time	t <sub>DPL</sub>	Tdpl	10	—	ns	1
Active (a) to Active (b) command period	t <sub>RRD</sub>	Trrd	20	—	ns	1
Transition time (rise and fall)	t <sub>T</sub>		1	5	ns	
Refresh period	t <sub>REF</sub>		—	64	ms	

- Notes:
1. AC measurement assumes  $t_T = 1$  ns. Reference level for timing of input signals is 1.5 V.
  2. Access time is measured at 1.5 V. Load condition is  $CL = 50$  pF.
  3.  $t_{LZ}$  (min) defines the time at which the outputs achieves the low impedance state.
  4.  $t_{HZ}$  (max) defines the time at which the outputs achieves the high impedance state.
  5.  $t_{CES}$  define CKE setup time to CLK rising edge except power down exit command.
  6.  $t_{AS}/t_{AH}$ : Address,  $t_{CS}/t_{CH}$ :  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{DQM}$ .  
 $t_{DS}/t_{DH}$ : Data-in,  $t_{CES}/t_{CEH}$ : CKE

## Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



# HM5225645F-B60, HM5225325F-B60

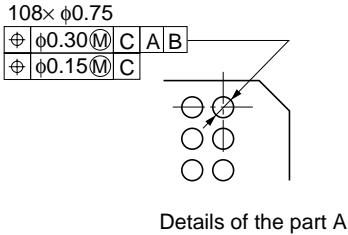
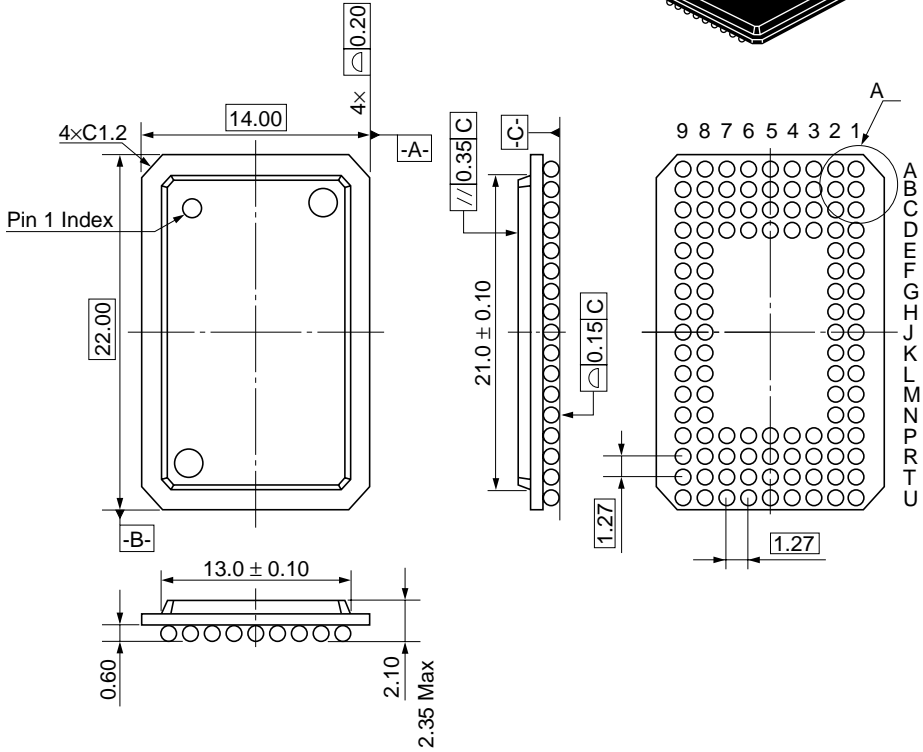
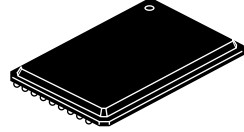
## Package Dimensions

HM5225645FBP Series

HM5225325FBP Series (BP-108)

Unit: mm

Preliminary



Hitachi Code	BP-108
JEDEC	—
EIAJ	—
Weight (reference value)	1.2 g

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**Hitachi, Ltd.**

Semiconductor & Integrated Circuits.  
 Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
 Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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**For further information write to:**

Hitachi Semiconductor  
 (America) Inc.  
 179 East Tasman Drive,  
 San Jose, CA 95134  
 Tel: <1> (408) 433-1990  
 Fax: <1>(408) 433-0223

Hitachi Europe GmbH  
 Electronic components Group  
 Dornacher Straße 3  
 D-85622 Feldkirchen, Munich  
 Germany  
 Tel: <49> (89) 9 9180-0  
 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
 Electronic Components Group.  
 Whitebrook Park  
 Lower Cookham Road  
 Maidenhead  
 Berkshire SL6 8YA, United Kingdom  
 Tel: <44> (1628) 585000  
 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
 16 Collyer Quay #20-00  
 Hitachi Tower  
 Singapore 049318  
 Tel: 535-2100  
 Fax: 535-1533

Hitachi Asia Ltd.  
 Taipei Branch Office  
 3F, Hung Kuo Building, No.167,  
 Tun-Hwa North Road, Taipei (105)  
 Tel: <886> (2) 2718-3666  
 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
 Group III (Electronic Components)  
 7/F., North Tower, World Finance Centre,  
 Harbour City, Canton Road, Tsim Sha Tsui,  
 Kowloon, Hong Kong  
 Tel: <852> (2) 735 9218  
 Fax: <852> (2) 730 0281  
 Telex: 40815 HITEC HX

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**Revision Record**

<b>Rev.</b>	<b>Date</b>	<b>Contents of Modification</b>	<b>Drawn by</b>	<b>Approved by</b>
0.0	Feb. 1, 1999	Initial issue	S. Hatano	S. Hatano
0.1	Feb. 19, 1999	Pin arrangement Correct pin No. to JEDEC standard Package dimension Correct illustration and indexes	S. Hatano	S. Hatano
0.2	Apr. 1, 1999	Ordering information Correct error of type No.	S. Hatano	S. Hatano
1.0	Oct. 1, 1999	Programmable $\overline{\text{CAS}}$ latency: 3 to 2/3 Ordering information Addition of note Pin description Addition of note 1 DC Characteristics (HM5225645F) $I_{\text{CC1}}$ max (CL = 2): 280 mA to 200 mA $I_{\text{CC1}}$ max (CL = 3): 300 mA to 220 mA $I_{\text{CC4}}$ max (CL = 2): 280 mA to 220 mA $I_{\text{CC4}}$ max (CL = 3): 360 mA to 270 mA $I_{\text{CC5}}$ max: 460 mA to 380 mA DC Characteristics (HM5225325F) $I_{\text{CC1}}$ max (CL = 2): 260 mA to 180 mA $I_{\text{CC1}}$ max (CL = 3): 280 mA to 200 mA $I_{\text{CC4}}$ max (CL = 2): 260 mA to 200 mA $I_{\text{CC4}}$ max (CL = 3): 320 mA to 250 mA $I_{\text{CC5}}$ max: 460 mA to 380 mA Capacitance $C_{11}$ max: 16 pF to 14 pF $C_{12}$ max: 20 pF to 14 pF $C_{\text{O}}$ min: 4 pF to 3 pF $C_{\text{O}}$ max: 6.5 pF to 5 pF Package dimension Change tolerance of height		